

Liquid Crystal Display Controller (LCDC) Documentation

The LCDC is an *Advanced Microcontroller Bus Architecture* (AMBA) master-slave module which connects to the *Advanced High-performance Bus* (AHB). The LCDC is an AMBA-compliant *System-on-a-Chip* (SoC) peripheral developed, tested and licensed by the Département Télécom of INPG.

Features

The LCDC provides all the necessary control signals to interface directly with a variety of monochrome LCD panels. The controller supports the following video parameters :

- 320 x 240 pixels resolution
- 8 bits depth (256 greyscale)

Inputs/Outputs

The LCDC provides the following inputs/outputs :

- AMBA compliant slave interface for configuration
- AMBA compliant master interface
- Display interrupt signal (`display_int`)
- LCD interface signals (pixel clock, control signals)

Figure 2 shows a simplified block diagram of the LCDC.

Operations

After reset, the LCDC is initially idle. Beginning of operation is triggered by writing into the `START_REG` register. The LCDC then performs read accesses to an external AMBA memory device holding the video buffer via its master interface. Addresses start at the value stored in the `ADDR_REG` register and increment until reaching the end of the buffer. Video data are supposed to be stored contiguously in memory, in big endian format (see figure 1). After reading the video buffer and sending appropriate signals on its LCD outputs, the controller asserts its `display_int` interrupt signal. The signal is supposed to be deasserted before next refresh (see `INT_REG` register reference).

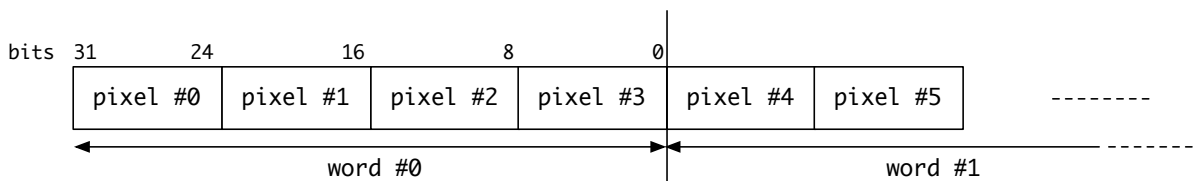


FIGURE 1 – Video data as expected in memory

