FM Demodulation Using PSoC® 3 and PSoC 5

AN59944

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Application Note Abstract

This application note explains two methods of demodulating a Frequency Modulation (FM) signal. One is the commonly used Slope Detection method; this is the conventional analog method. The second method uses a monostable multivibrator and is one of the best methods in terms of Signal to Noise Ratio (SNR) and Total Harmonic Distortion (THD). A sample project that implements the FM demodulator using the monostable multivibrator is attached with this application note.

Introduction

Frequency modulation is one of the most popular modulation techniques. It is used in many applications because it provides better fidelity and high noise immunity. There are various methods available for FM demodulation. The flexibility and resourcefulness of the PSoC® device allows adopting different methods to implement an FM demodulator.

Method 1: Slope Detection

An FM demodulator is a circuit that provides an output voltage proportional to the instantaneous frequency or frequency deviation of the input. Slope detection is a conventional analog FM demodulation method which revolves around this principle. In this method, an FM signal is converted to an AM signal and then decoded. The block diagram of the slope detection method is as follows.

Figure 1. Slope Detection Method Block Diagram

The final PSoC Creator™ schematic to implement an FM demodulator using slope detection method is as follows.

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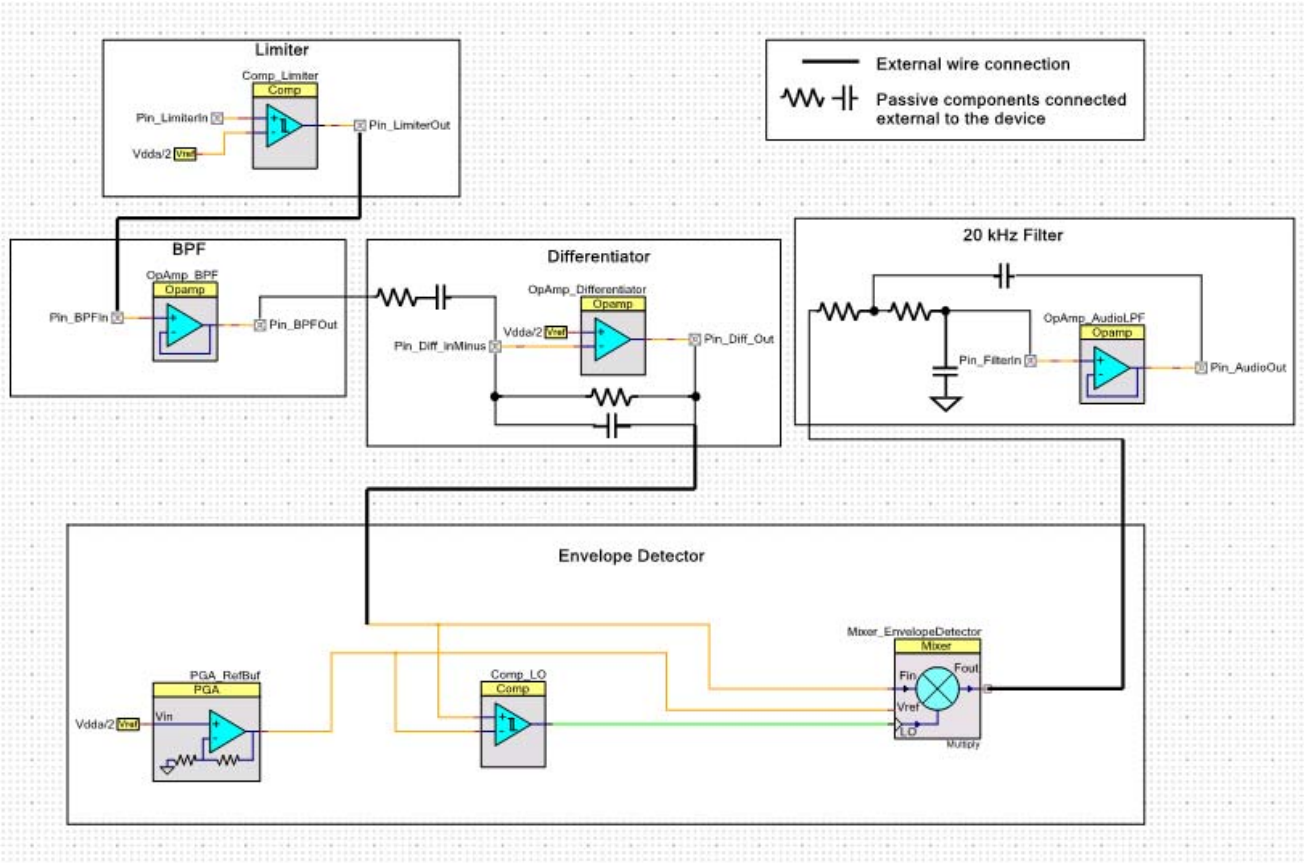
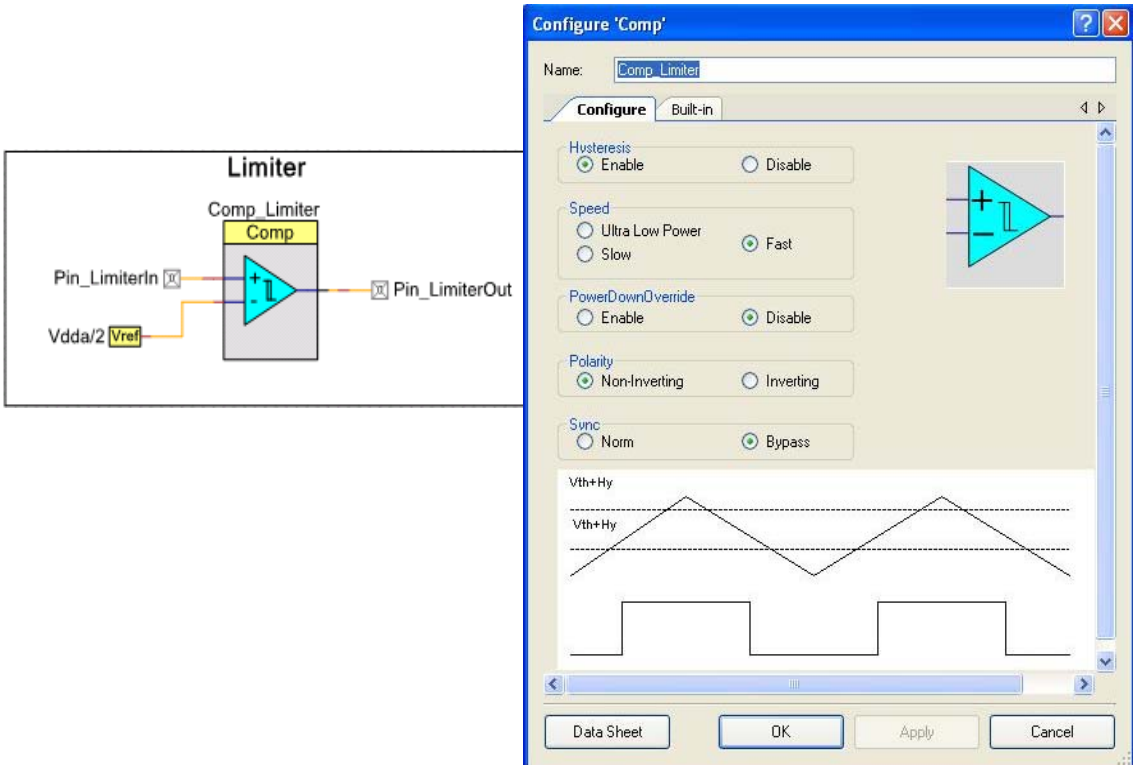
Figure 2. PSoC Creator Schematic for Slope Detection Method



The passive components to be connected, except the Band Pass Filter (BPF), are illustrated. You can design the BPF based on the application. The order of the BPF can be increased by using more opamps; an additional opamp and three SC/CT opamps are available.

A limiter circuit is the first stage of the FM demodulator. A limiter is used to eliminate the small noise present in the form of amplitude variations. The output of the limiter is a square wave of constant amplitude. A comparator can be used for this purpose by applying suitable threshold. The sample configuration of the comparator is shown in the following figure.

Figure 3. Comparator Configuration



Note that the comparator speed type determines the maximum frequency that it can convert. It also has an inverse relationship with the current consumed by the block. The hysteresis for the comparator is enabled to significantly improve the noise tolerance of the system.

The output of the limiter is sent through a BPF. The BPF filters out the square wave harmonics and provides a sine wave of constant amplitude. The BPF cut-off frequency should be designed at the carrier frequency. The bandwidth of the BPF is determined using Carson's rule. According to Carson's rule, the Required Bandwidth (RBW) is related to the deviation of FM input (Δf) and maximum modulating signal frequency (fm) as follows:

$$RBW = 2 \times (\Delta f + fm) \quad \text{Equation 1}$$

Active narrow band or wide band BPF can be constructed using the opamps inside the PSoC 3 / PSoC 5 device, together with external passives.

The differentiator circuit converts the FM signal to an AM signal. The AM signal amplitude is proportional to the instantaneous frequency of the FM signal, which is in turn proportional to the amplitude of the modulating signal.

An FM signal can be represented as,

$$S(t) = AcCos[\ 2\pi fct + \beta Sin(2\pi fmt)\ ] \quad \text{Equation 2}$$

Where,

Fc is the Carrier Frequency

fm is the Message Signal Frequency

Ac is the Carrier Amplitude

B, modulation index is Δf/fm where $\Delta f = k_f \times Am$

Am is the message signal amplitude and k_f is the frequency sensitivity measured in Hertz/Volt.

On differentiation it becomes,

$$S'(t) = (\ 2\pi fc + \beta \times 2\pi fmCos(2\pi fmt)) \times (AcSin[\ 2\pi fct + \beta Sin(2\pi fmt)\ ]) \quad \text{Equation 3}$$

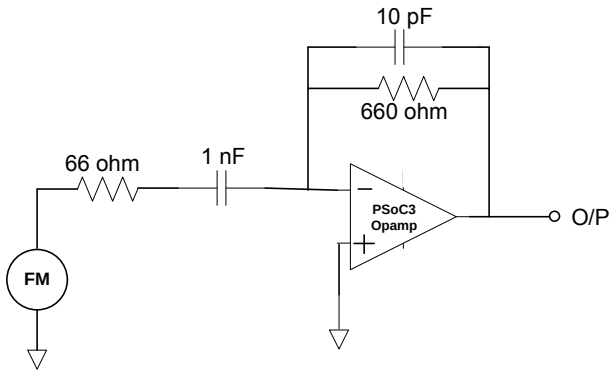
The amplitude of the resultant signal is given as,

$$Ac \times (2\pi fc + \beta \times 2\pi fmCos\ (2\pi fmt))$$

Equation 2 indicates that the amplitude of the differentiator output signal is directly proportional to the amplitude of the modulating signal.

A simple differentiator circuit with external components designed for an FM wave with a frequency range of 150 kHz to 350 kHz is shown in the following figure.

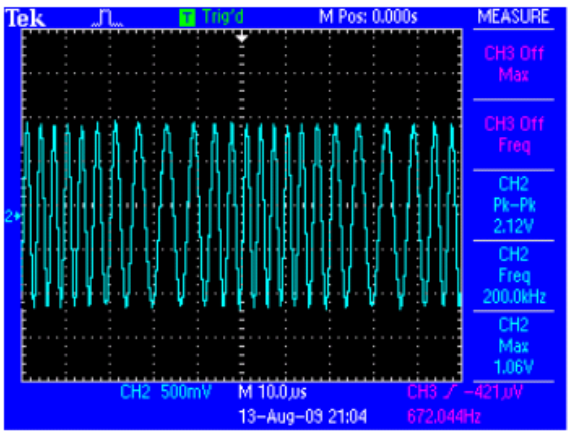
Figure 4. Simple Differentiator Circuit



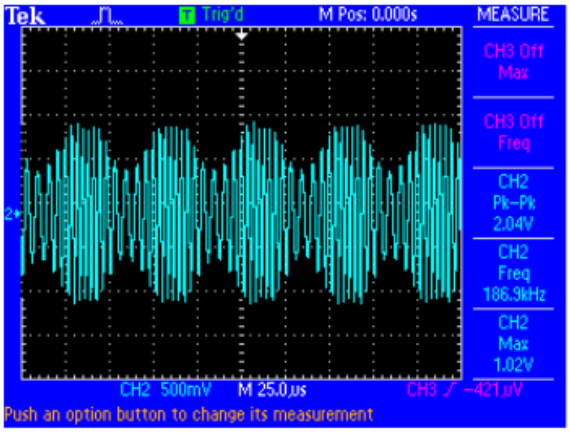
The differentiator circuit design is important because the total harmonic distortion of the FM demodulator depends on the linearity of the differentiator circuit. The section Important FM Specifications discusses the linearity of the differentiator circuit. Waveforms showing the FM modulated signal and the differentiated output are shown in the following figure.

Figure 5. FM Signal and Differentiator Output

FM SIGNAL

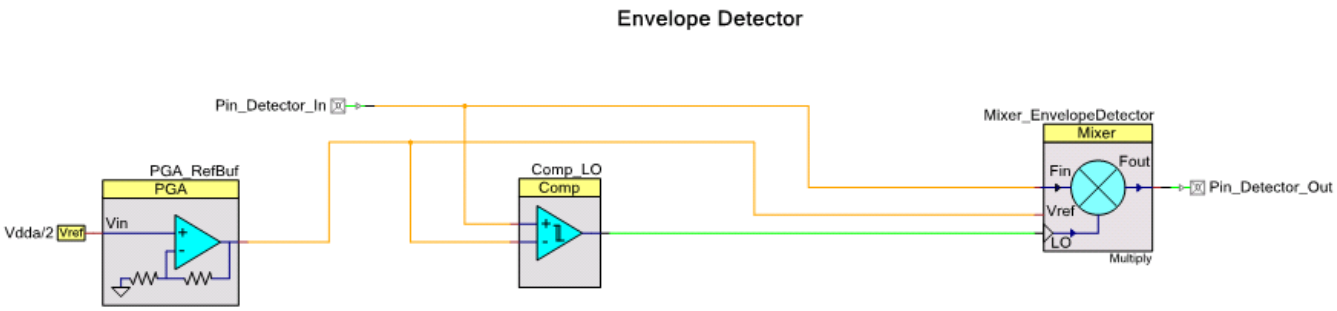


DIFFERENTIATOR O/P



The output of the differentiator has amplitude variations proportional to the message signal. Therefore, it is passed through an envelope detector or amplitude demodulator to retrieve the original signal. There are different methods of implementing an envelope detector; the most common design is the one with a diode, resistor, and a capacitor. In a PSoC 3 / PSoC 5 device, an envelope detector can be built without using any external components. The schematic of an envelope detector biased at Vdda/2 is as follows.

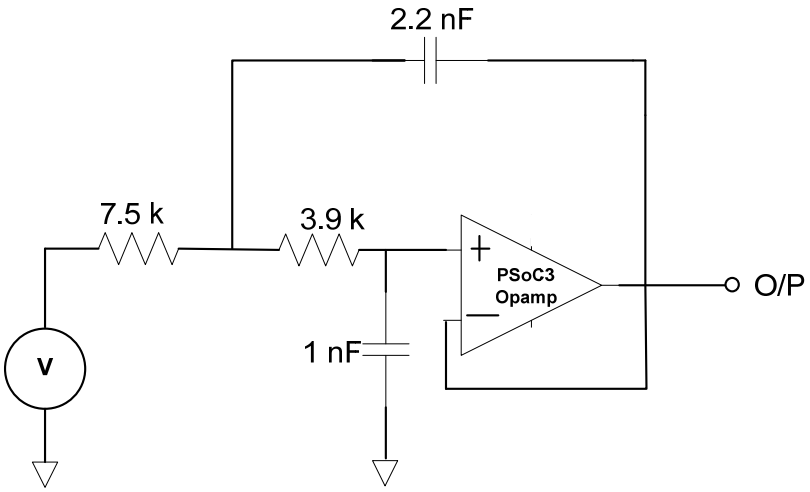
Figure 6. Envelope Detector Schematic



In the figure, note that a PGA is used as a buffer for the reference voltage. For PGA to act as a buffer, the gain of the PGA should be set to ‘1’.

The output of the envelope detector contains the modulating signal including other harmonics. The higher frequency can be eliminated and modulating signal can be retrieved using a low-pass filter. A simple low-pass filter designed to pass the full audio signal range is shown in the following figure.

Figure 7. Low-Pass Filter Circuit Diagram



Important FM Specifications

Many specifications exist for FM demodulator circuits. The output of the FM demodulator circuit mentioned previously is used to determine important specifications such as THD and SNR. The test setup is as follows.

A frequency modulated signal is generated using a function generator. The output of the function generator is given as an input to the FM demodulator circuit. The demodulated signal is given to a spectrum analyzer to determine the THD and SNR of the output. The THD and SNR of the FM demodulator circuit for a modulating signal of frequency 1 kHz and amplitude 1 V peak to peak is as follows.

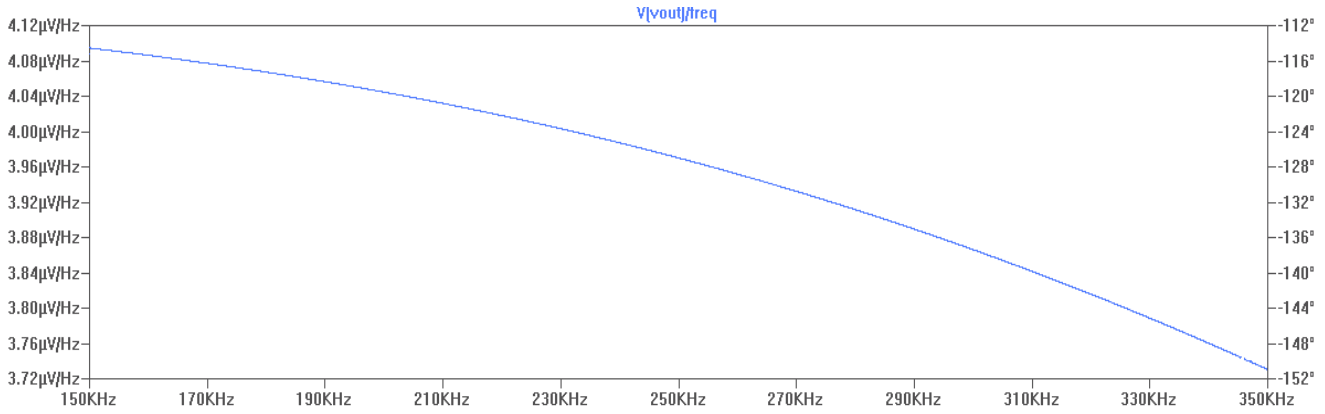
- THD: < 5%
- SNR: 60 dB

The sensitivity of the FM demodulator circuitry is determined by the hysteresis of the input comparator used as limiter. The sensitivity of the FM demodulator using slope detection method is 10 mV.

THD is sometimes an important parameter in FM demodulation circuits. With the slope detection method, it is possible to achieve THD less than or equal to 5%. The main reason for a bad THD is circuit non linearity. Some suggestions to improve the THD for the slope detection method are as follows.

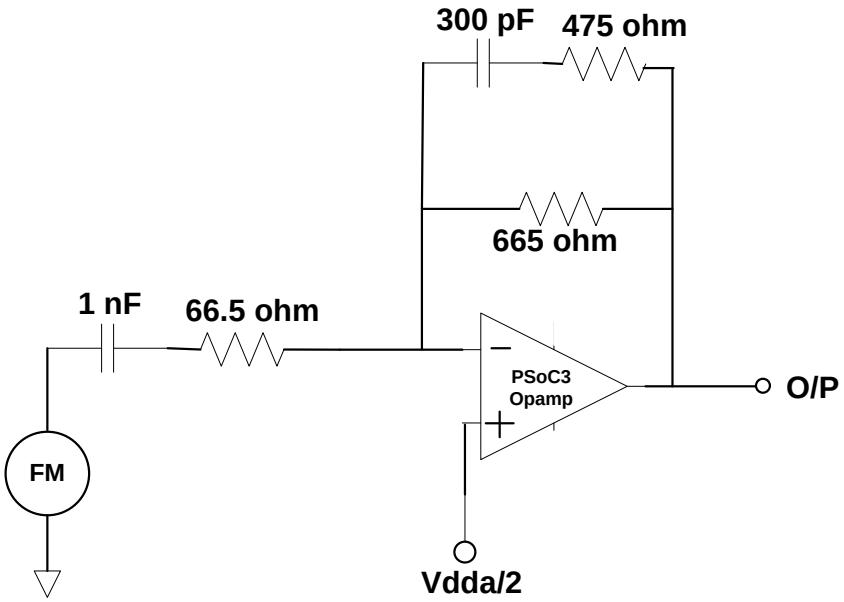
- Design the BPF such that the pass band characteristics are linear.
- The differentiator circuit design is a major contributor to harmonic distortion. Optimize the design values such that the output amplitude is proportional to the frequency in working range. Consider the following graph.

Figure 8. Differentiator Output Characteristics



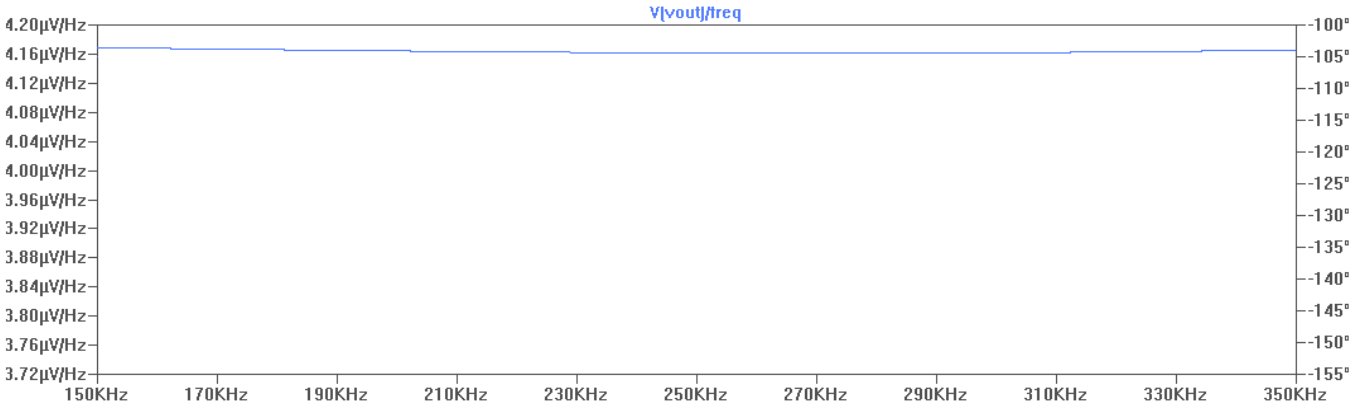
This graph shows the output voltage/frequency versus frequency of the simple differentiator circuit mentioned in the previous section. This differentiator circuit is designed for an FM with a frequency range of 150 kHz to 350 kHz. For a linear system, the response is a straight line. As seen, the response of the simple differentiator circuit is not linear for frequencies in the working range. This is a potential problem resulting in a bad THD figure. Therefore, the differentiator circuit should be designed accordingly to meet the ideal response. An improved differentiator design is shown in the following figure.

Figure 9. Modified Differentiator Circuit Diagram



The plot showing the output characteristics of the modified differentiator circuit is as follows.

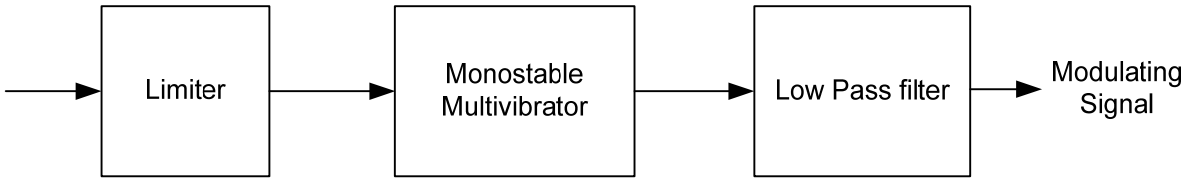
Figure 10. Output Characteristics of Improved Differentiator Design



Method 2: FM Demodulation Using Monostable Multivibrator

FM demodulation can be implemented in a better way by using a monostable multivibrator. The theory behind this method is that when the square output of comparator (limiter) is applied as the trigger input to a monostable multivibrator of fixed pulse width, the average value of the output pulse stream is proportional to the instantaneous frequency of the FM signal. This, in turn, is proportional to the modulating signal. Hence, if the output of the monostable multivibrator is passed through a low-pass filter, the modulating signal can be retrieved. The block diagram of this method is shown as follows.

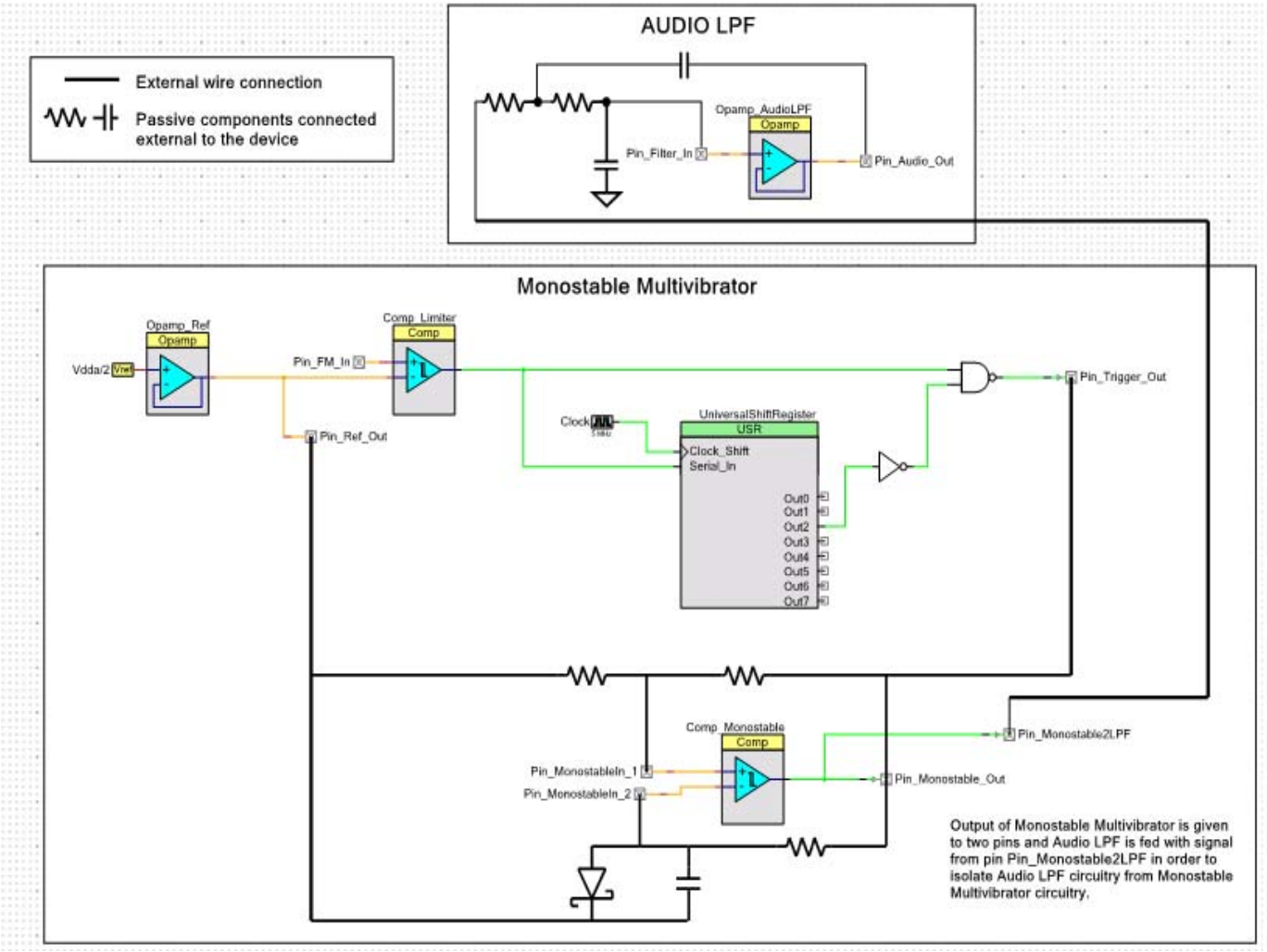
Figure 11. FM Demodulation Block Diagram Using Monostable Multivibrator



PSoC 3 / PSoC 5 Implementation

The PSoC Creator schematic to implement the FM demodulator using the monostable method is shown in the following figure.

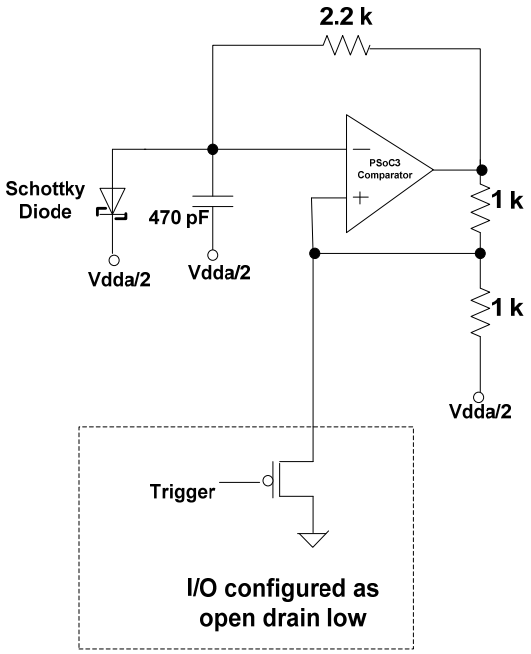
Figure 12. PSoC Creator Schematic for Monostable Method



Monostable Multivibrator

A monostable multivibrator circuit built using a PSoC 3 / PSoC 5 comparator and few passive components is shown in the following figure.

Figure 13. Monostable Multivibrator Circuit Diagram



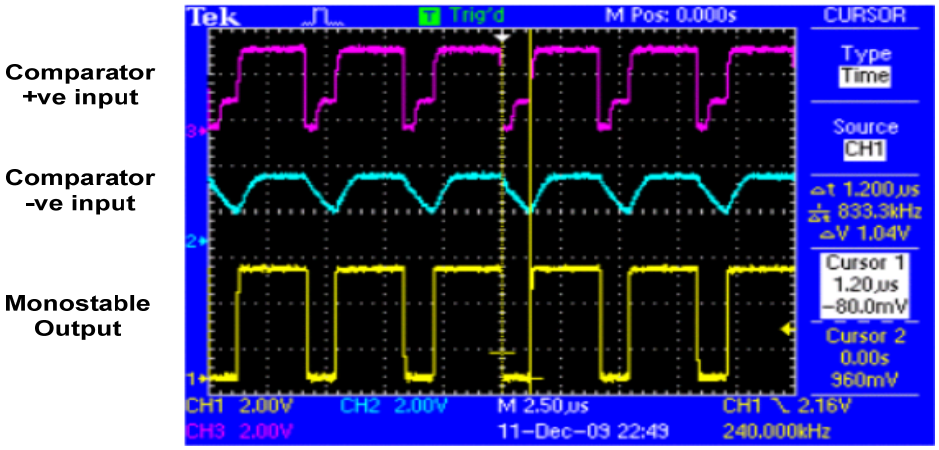
The circuit shown is similar to a conventional monostable multivibrator circuit using dual supply opamps. Here, the whole circuit is biased at Vdda/2, so that the output of the monostable multivibrator switches between GND and V_{DD}. The PSoC device does not accept negative voltages.

The steady state of the monostable circuit is Logic High (V_{DD}). The capacitor is charged to a voltage equal to Vdda/2 + knee voltage of diode. The positive input of the comparator has a voltage equal to 3 Vdda/4. This is greater than the voltage at negative terminal because the Schottky diode has a low knee voltage.

When the trigger input goes low, the open drain I/O pulls down the comparator positive input to ground. Hence the comparator output goes Low (quasi stable state). Now, the capacitor discharges. The trigger should be a low going pulse with very low pulse width. After the trigger is removed, the voltage at the positive input becomes Vdda/4 (because the output is low). Hence, the capacitor discharges until the voltage across the capacitor reaches Vdda/4. When the capacitor voltage becomes slightly less than Vdda/4, the comparator output goes high and the monostable returns to its stable state.

The following figure shows a screenshot of the waveforms at comparator output and both the inputs.

Figure 14. Monostable Multivibrator Waveforms



The monostable multivibrator circuit is designed for a pulse width of 1.2 uS. The trigger applied has a low going pulse width of 600 nS.

The conventional monostable multivibrator circuit has a differentiator circuit, which converts the square wave into spikes of very low pulse width before applying it as the trigger. However, in a PSoC 3 / PSoC 5 device, this differentiator functionality can be implemented digitally using UDB. A custom component named Universal Shift Register created as a PSoC Creator library project is used for this purpose.

The symbol and the configuration options for Universal Shift Register are shown as follows.

Figure 15. Universal Shift Register Component Symbol

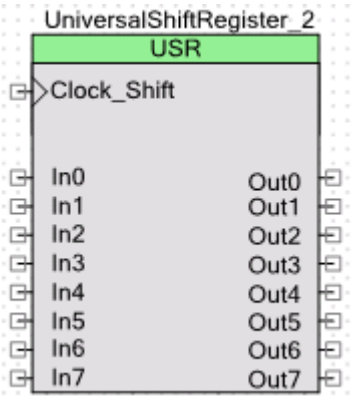
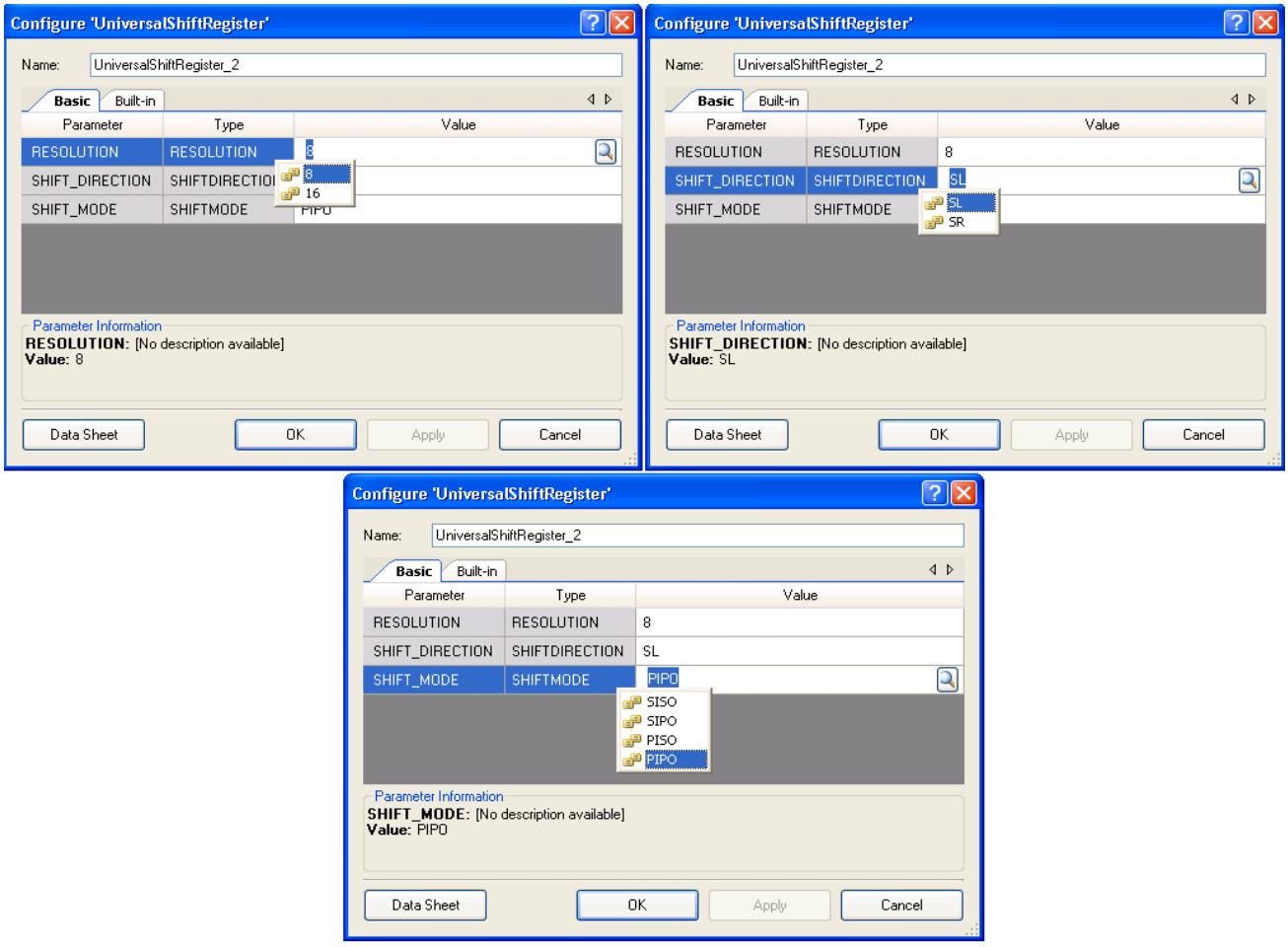


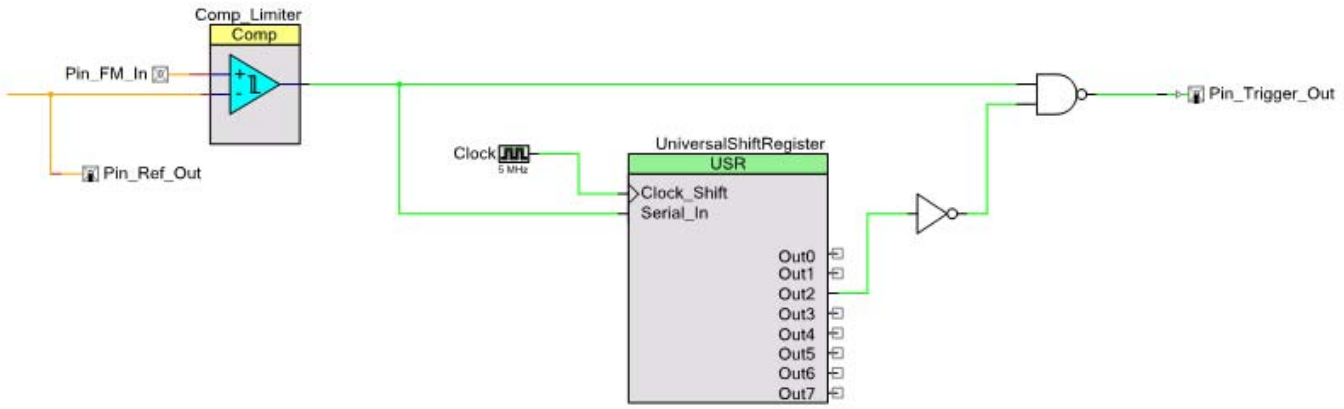
Figure 16. Configuration Options for Universal Shift Register Component



As shown, the Universal Shift Register can be configured for resolution of 8 bits or 16 bits. The component supports left shift and right shift in all four shift modes including serial-in serial-out mode, serial-in parallel-out mode, parallel-in serial-out mode, and parallel-in parallel-out mode. The parallel outputs available in the component enable the component to be used as a highly programmable delay element.

The digital trigger circuitry used in the project is shown in the following figure.

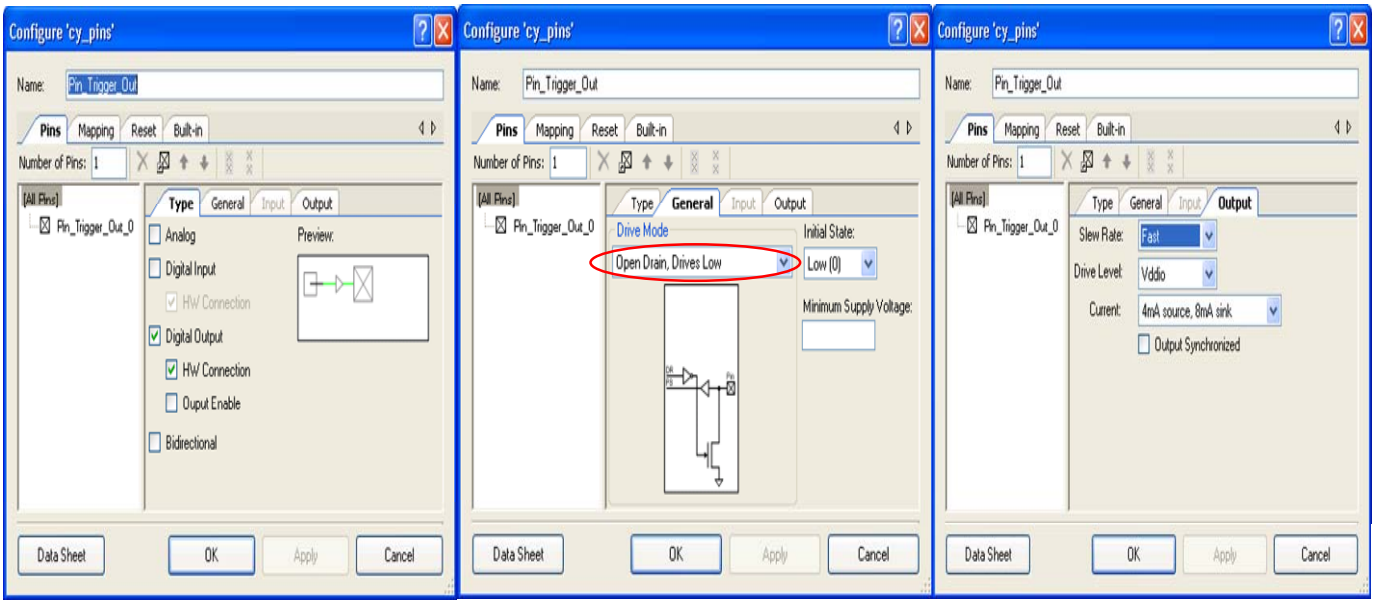
Figure 17. Trigger Circuitry Schematic



The Universal Shift Register is configured for serial-in parallel-out mode. The Universal Shift Register is used as a delay element. The pulse width required for the trigger pulse can be programmed by changing the shift register delay. In this case, to achieve a pulse width of 600 nanoseconds, the Universal Shift Register clock is chosen as 5 MHz and output is taken from the third tap (Out2). Hence, the delay is ((1/5 MHz = 200 ns)*3 = 600 ns).

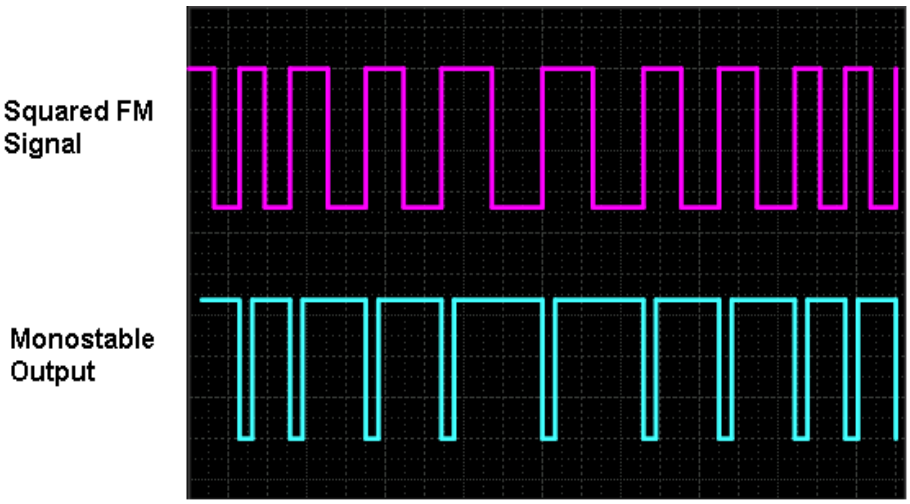
In the schematic, note that the output of the trigger circuitry is connected to a pin named ‘Pin_Trigger_Out’. The pin must be configured for open drain low drive mode for the monostable multivibrator circuit to work. The configurations for the pin are shown in the following figure.

Figure 18. Configuration for Pin_Trigger_Out



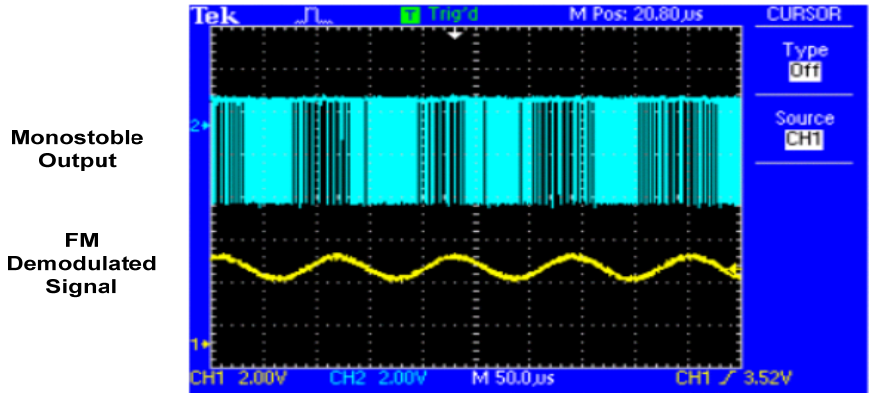
The output of monostable circuit when a squared FM signal is given as the trigger input is shown in the following figure.

Figure 19. Limiter Output and Monostable Output Waveforms



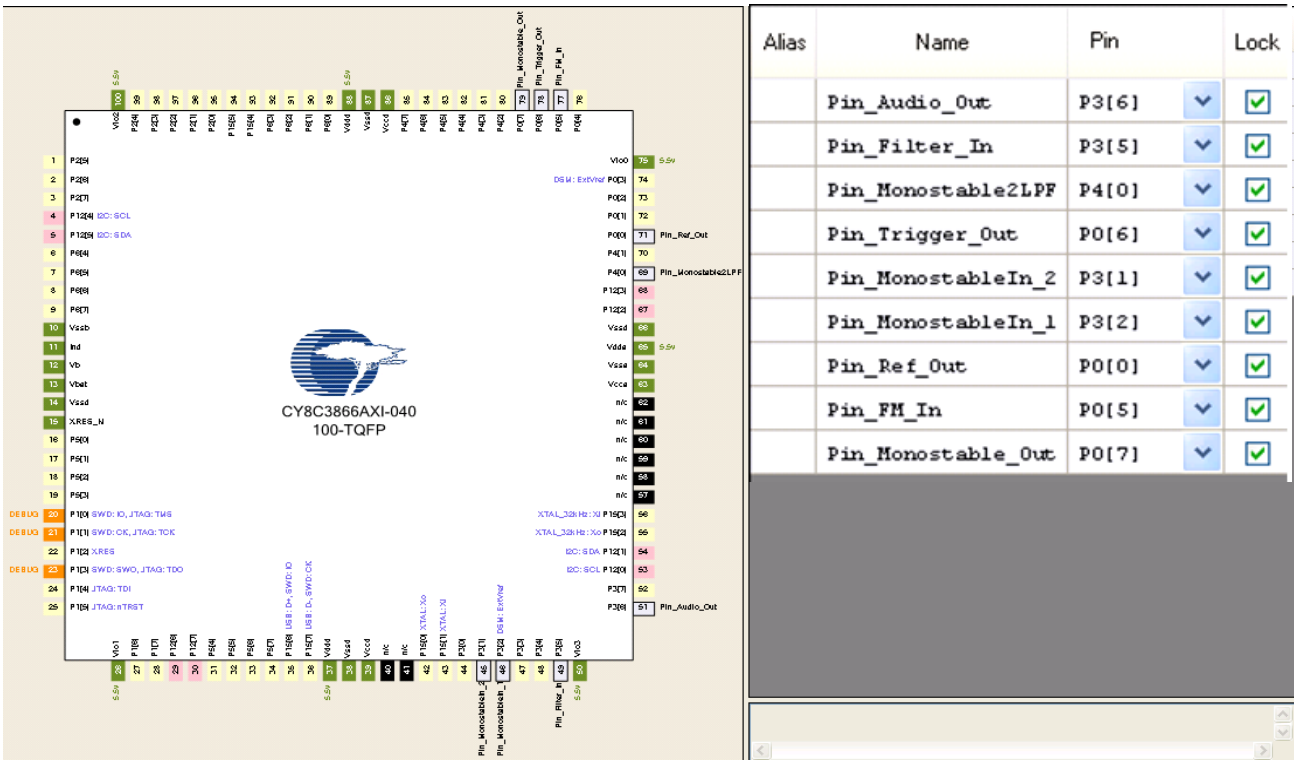
As shown in previous figure, when the monostable output is passed through a low pass filter, the original modulating signal is retrieved. The waveforms are as follows.

Figure 20. Monostable Output and Low Pass Filter Output Waveforms



The pinout information for the attached project is included in the following figure.

Figure 21. Pinout Diagram

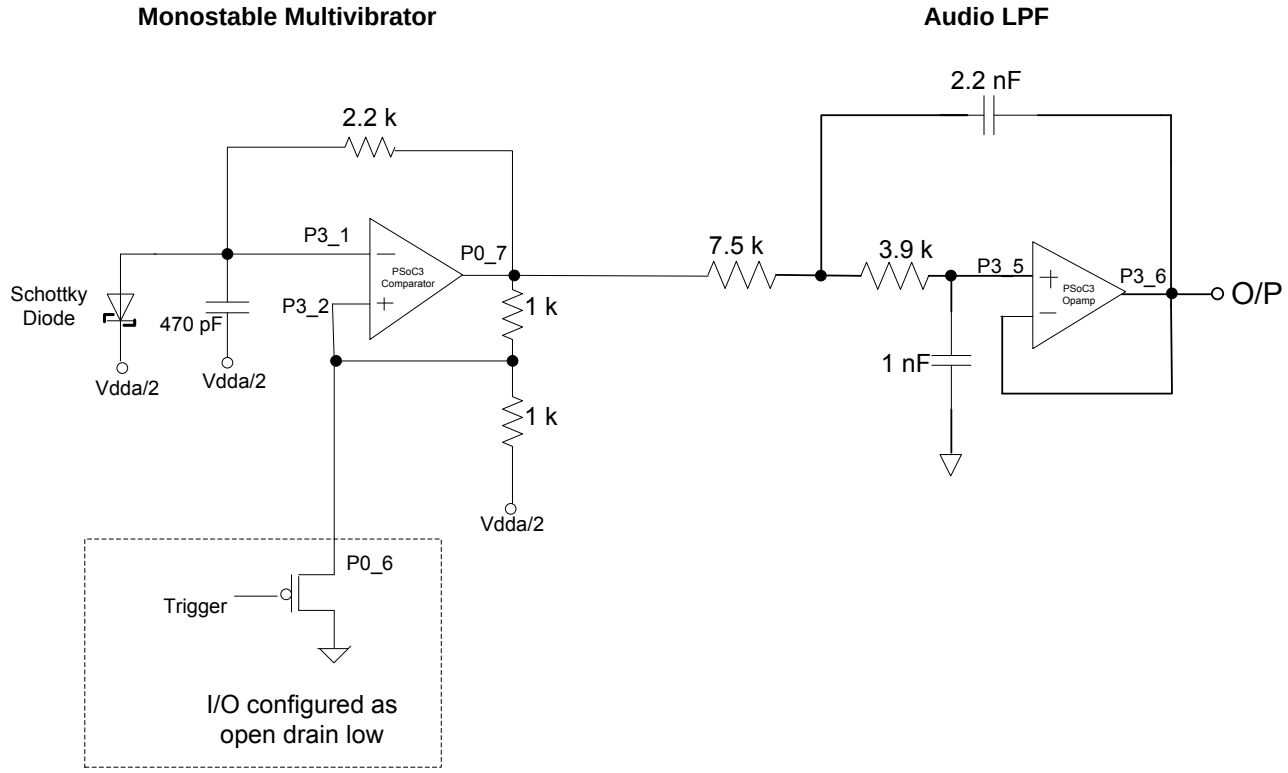


You can change the pin placement accordingly. For best results, route the opamp input and output pins to the direct connection pins.

Circuit Diagram

The final circuit diagram to implement the FM demodulator with a frequency range of 150 kHz to 350 kHz using the monostable multivibrator method is shown in the following figure.

Figure 22. Circuit Diagram of FM Demodulator using Monostable Multivibrator



The low-pass filter is designed to pass the full audio range. The pinouts shown in the circuit diagram are with respect to the pin placement of the attached project.

Important FM Specifications

This method exhibits great performance in terms of THD and SNR. Some of the important parameters measured using the previously mentioned circuit elements for a modulating signal of frequency 1 kHz and amplitude 1 V peak to peak are as follows.

- THD: 0.01%
- Sensitivity: 10 mV (hysteresis of comparator used as limiter)
- SNR: 80 dB

The improvement in THD is mainly because THD is no longer determined by the linearity of the differentiator circuit. It depends on the linear relationship between modulating signal frequency and output voltage. The output voltage is determined by the width of the monostable multivibrator output, which in turn is inversely proportional to the frequency of the modulating signal. Hence, the output voltage becomes proportional to the modulating signal frequency and thus reduces total harmonic distortion.

Comparison of Methods

The following table summarizes the comparison between the two FM demodulation methods.

Table 1. Comparison of FM Demodulation Methods

Method	THD	SNR	Sensitivity	Pins	Opamps	Comparators	SC/CT Blocks	External Component Count
Slope Detection	< 5%	60 dB	10 mV	8	3	2	2	8[1]
Monostable Multivibrator	0.01%	80 dB	10 mV	9	2	2	-	9

1. The external component count for slope detection method does not include the external components that are used to implement the band pass filter.

Frequency Range Limitations

Both of the FM demodulator implementations explained in this application note can be used in applications where the maximum frequency of the FM is less than 10 MHz. To demodulate high frequency FM signals, for example, in the range of 88 MHz to 108 MHz, use suitable down convertors to the PSoC 3 / PSoC 5 device externally.

Summary

The flexibility of PSoC 3 / PSoC 5, along with its analog and digital capabilities, makes it possible to implement an FM demodulator using different methods. This application note discusses the implementation of an FM demodulator using slope detection and monostable multivibrator.

A project that implements FM demodulator using monostable multivibrator is attached with this application note. The project workspace is named *FM_Demodulation.cywrk*. The library project for the Universal Shift Register component is also available with this document.

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**	2886337	ANUP	04/05/2010	New application note.
*A	2940939	ANUP	06/01/2010	Updated to PSoC Creator Beta 4.1. Updated content and projects to be compatible with PSoC 5
*B	3011406	ANUP	19/08/2010	Updated to PSoC Creator Beta 5.
*C	3155622	LRDK	01/27/2011	Updated to PSoC Creator 1.0.
*D	3194288	ANUP	03/12/2011	Changed section title for clarification.

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