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VANIER COLLEGE - Computer Engineering Technology
247-205 Circuit Analysis and Simulation II

Lab 10 - Transistor Class A amplifier

Purpose:

a) Drawing the complete load line and the selected Q point.
b) Analyze the ac response of this type A amplifier.
c) Observe the cutoff regions.
d) Observe an Off-centered Q point.

To be submitted:

1. **Deadline**: In 1 week to be submitted via Lea, MIO not accepted.
2. **NO formal report is required**.
    a. **Answer all the questions** in the lab in the blank space provided. (this is where you get your marks)
    b. If calculations are involved, clearly show all the working steps involved. (you can do it on a paper take a **GOOD** picture and add it to the word document in the proper place.)
    c. Attach table/plot, screen shots clearly labelled, whenever applicable to word document.
    d. Include a final discussion and conclusion session.
3. **TO HAND IN:**
    a. This word document filled in properly.
    b. Your Proteus files.
    c. Please do not Zip the file, instead hand in two files one after the other.

Theory:

A transistor can be represented internally by 2 diode junctions. Hence, a multimeter/ohmmeter can be used to check each diode junction with simple test for open or shorted diode junctions. Then it is possible to determine if a given transistor is NPN or PNP.

Voltage-divider bias is often used because the based current is made small compared to the currents through the two base resistors. Consequently, the base voltage and collector current are stabilized against changes in the circuit.

Lab Work:

Part 1: Drawing the complete load line and the selected Q point.
To be done before going to Proteus.

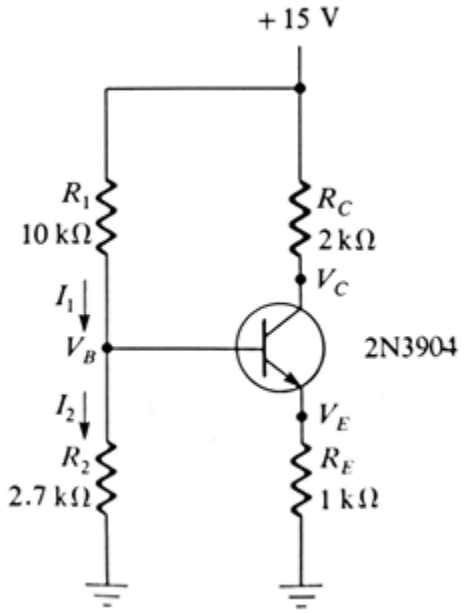


Figure 1-class A amplifier circuits

1. Calculate the $I_{C(sat)}$ and $V_{CE(cutoff)}$.
   Calculations and work under question 3.

Parameter	Value
$I_{C(sat)}$	***5 mA***
$V_{CE(cutoff)}$	***15 V***

Table 1 Saturation and cutoff values

2. Draw a new LOAD LINE graph using the values in Table 1 Saturation and cutoff values . Compare with last week's Load Line.

   Between this load line and the load line that was done last week, the results are pretty much the same, with a few minor differences, otherwise they are identical. Also, this is the same voltage-divider bias circuit that was used to construct the load line last week, so the two load lines should be pretty much the same.

   Calculations and work under question 3.

3. Calculate the Q point and add it to the graph.

   Calculations and work…

Question 1:

$V_{CE(cutoff)} \cong V_{CC}$

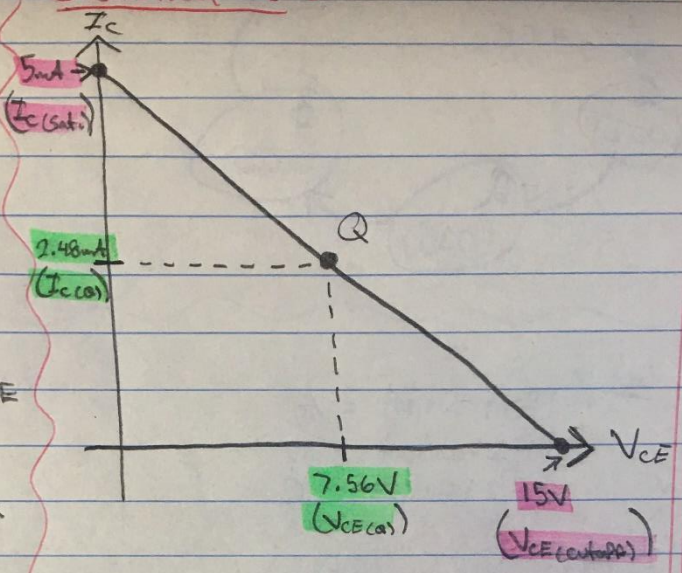
$= 15V$

$I_{C(saturation)} = \frac{V_{CC}}{R_C + R_E}$

$= \frac{15V}{2k + 1k}$

$= 5mA$

Question 2:



Question 3:

① $V_{B(Q)} \cong \left(\frac{R_2}{R_1 + R_2}\right) \cdot V_{CC}$

$= \left(\frac{2.7k}{10k + 2.7k}\right) \cdot 15V$

$= 3.18V$

② $I_{E(Q)} = \frac{V_{B(Q)} - 0.7}{R_E}$

$= \frac{3.18V - 0.7V}{1k}$

$= 2.48mA$

③ *β_{DC} is not available:

$I_{C(Q)} \cong I_{E(Q)}$

$= 2.48mA$

④ $V_{C(Q)} \cong V_{CC} - (I_{C(Q)} \cdot R_C)$

$= 15V - (2.48mA \cdot 2k)$

$= 10.04V$

⑤ $V_{CE(Q)} = V_{C(Q)} - (I_{E(Q)} \cdot R_E)$

$= 10.04V - (2.48mA \cdot 1k)$

$= 7.56V$

Part 2: Class A amplifier

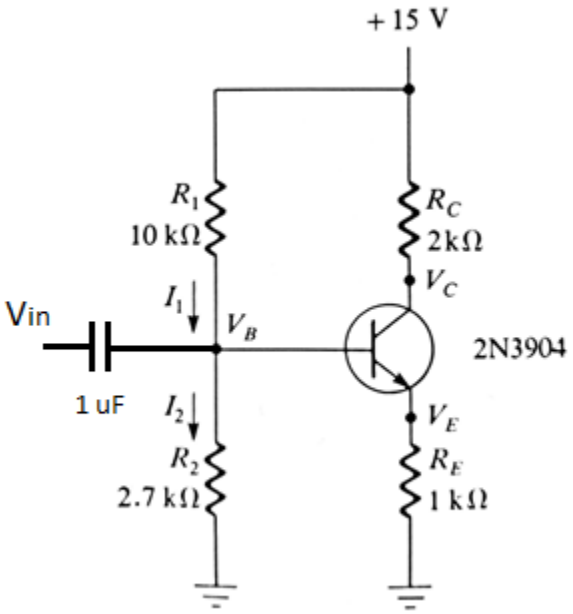
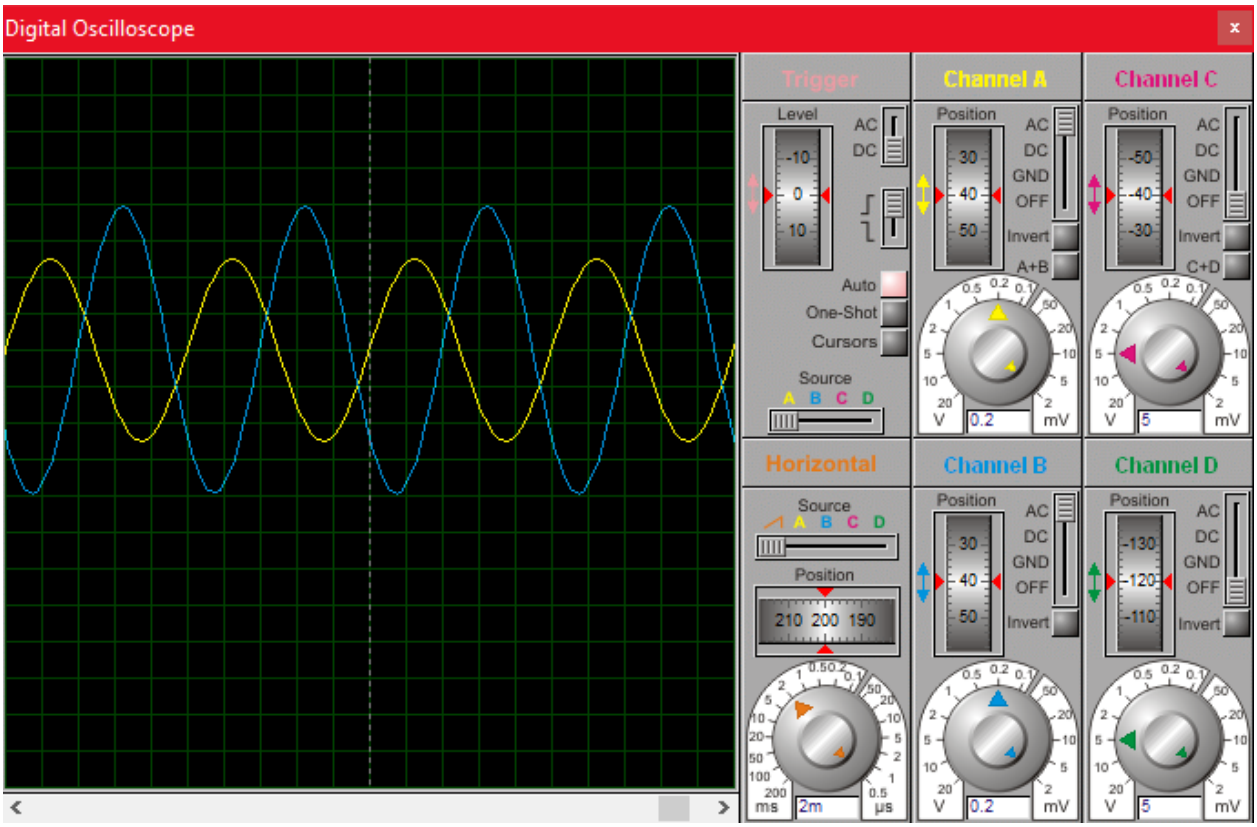
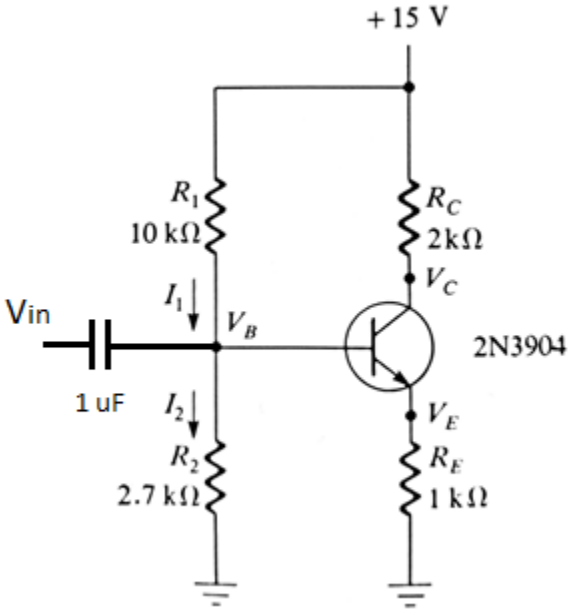


Figure 2

4. Watch the following YouTube video: https://youtu.be/YhzcXgxBGpU

Put a 1 V (peak to peak) 100 Hz sine wave on V_{IN}, through a 1 µF capacitor as shown in





5. Figure 2. Visualize the Vout and Vin on the oscilloscope, take a screen shot and explain the input and output waveforms.

These are the typical results one should see when dealing with a class A amplifier circuit. In the screenshot above, the yellow graph represents V_{IN} (signal going into the circuit) and the blue graph represents V_{OUT} (signal going out of the circuit). Since this is a class A amplifier, the output waveform (V_{OUT}: blue) is directly inversed to the input waveform (V_{IN}: yellow). Also, the output waveform (V_{OUT}: blue) has an amplified signal compared to the input waveform (signal is bigger). This is shown in the screenshot above.

6. Calculate Av from the measurements in step 4. Compare with the theoretical values based on R_C and R_E

   Theoretical:

   $$A_V = \frac{R_C}{R_E}$$

   $$= \frac{2k\Omega}{1k\Omega}$$

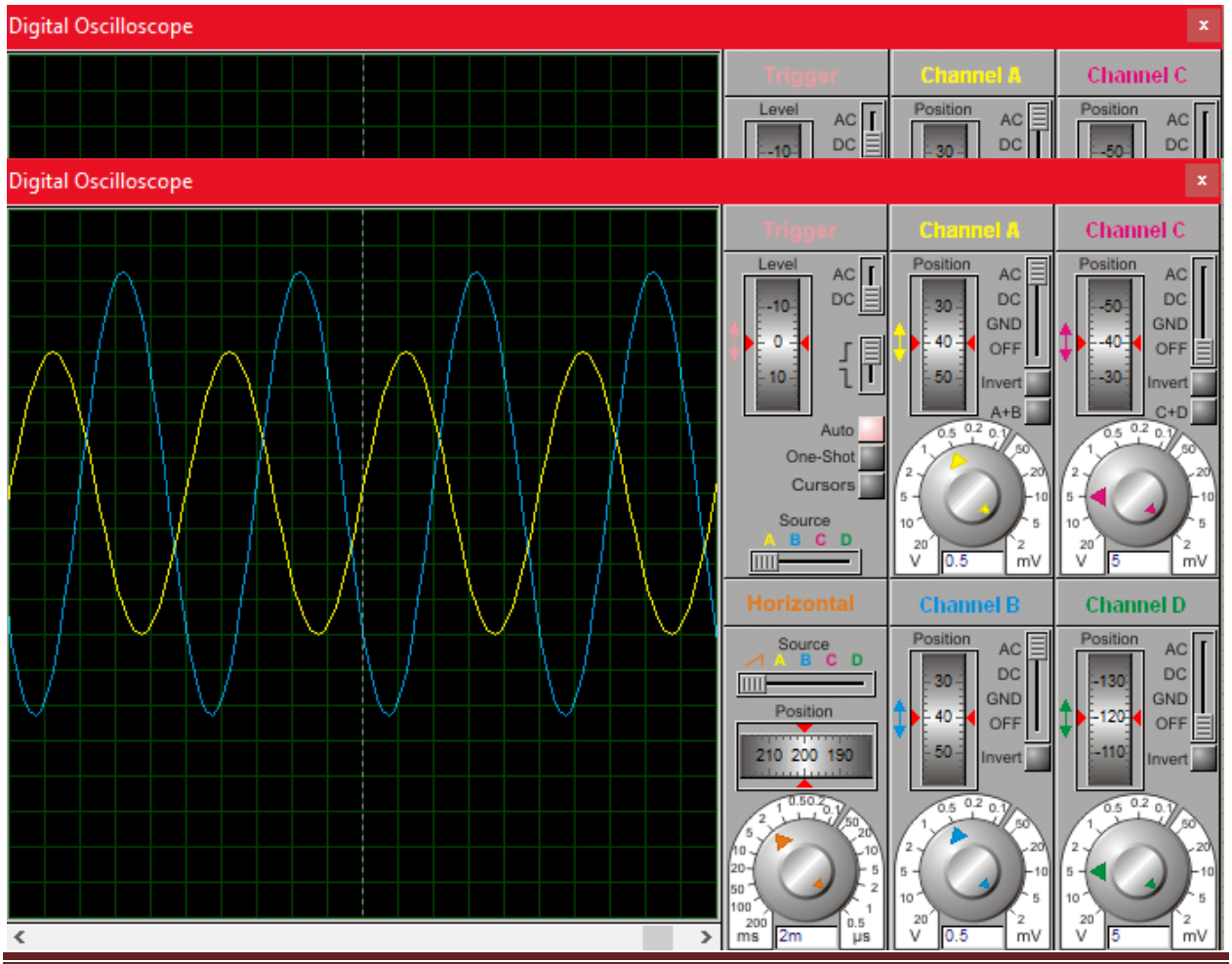
   $$A_V = 2$$

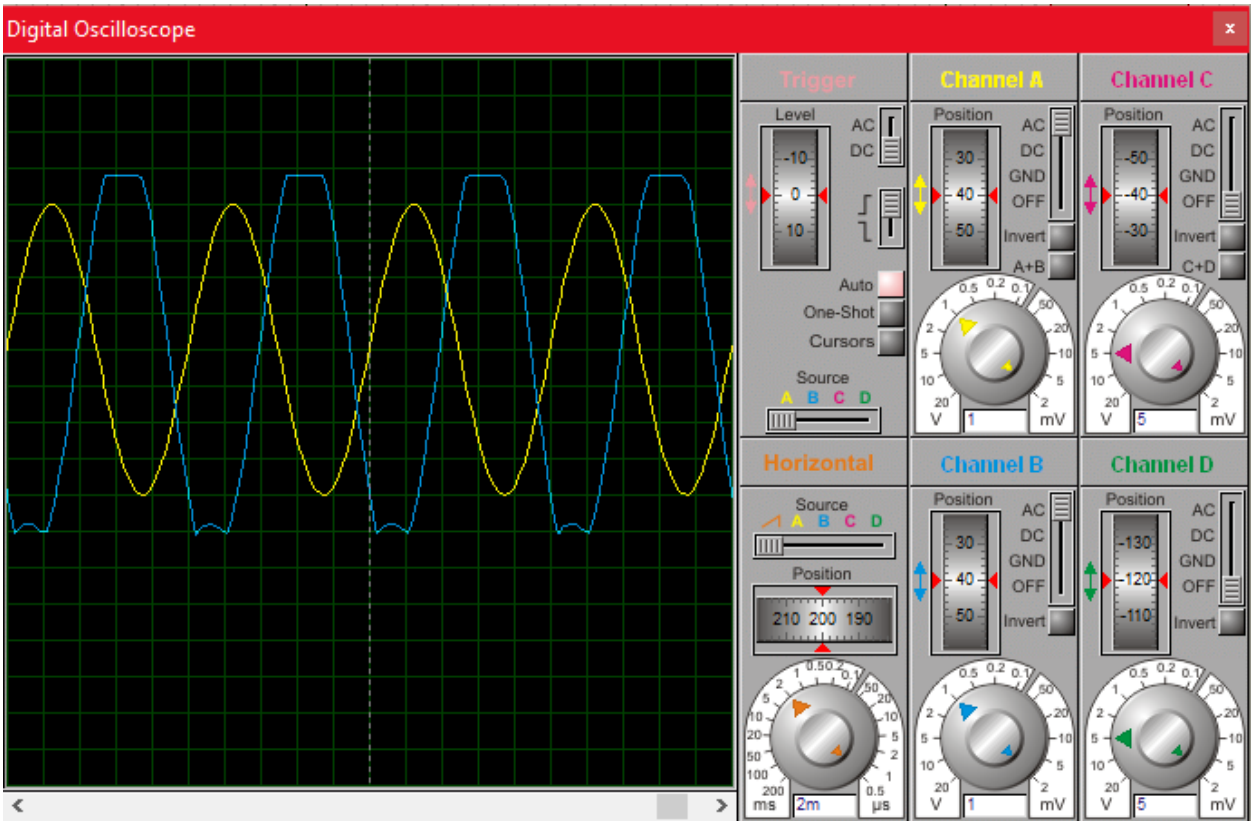
   Looking at the screenshot above:

   When looking at the screenshot in question 5, the output waveform peak (V_{OUT}: blue graph), is about 4 divisions high. The input waveform peak (V_{IN}: yellow graph) is about 2 divisions high. So, doing some basic mental math, one could say that the output waveform is about 2 times bigger then the input waveform. This checks out with the theoretical value that was calculated above.

Part 3: exploring the limits

7. Increase the amplitude of the waveform until the output is distorted. Take a capture and explain what you see.



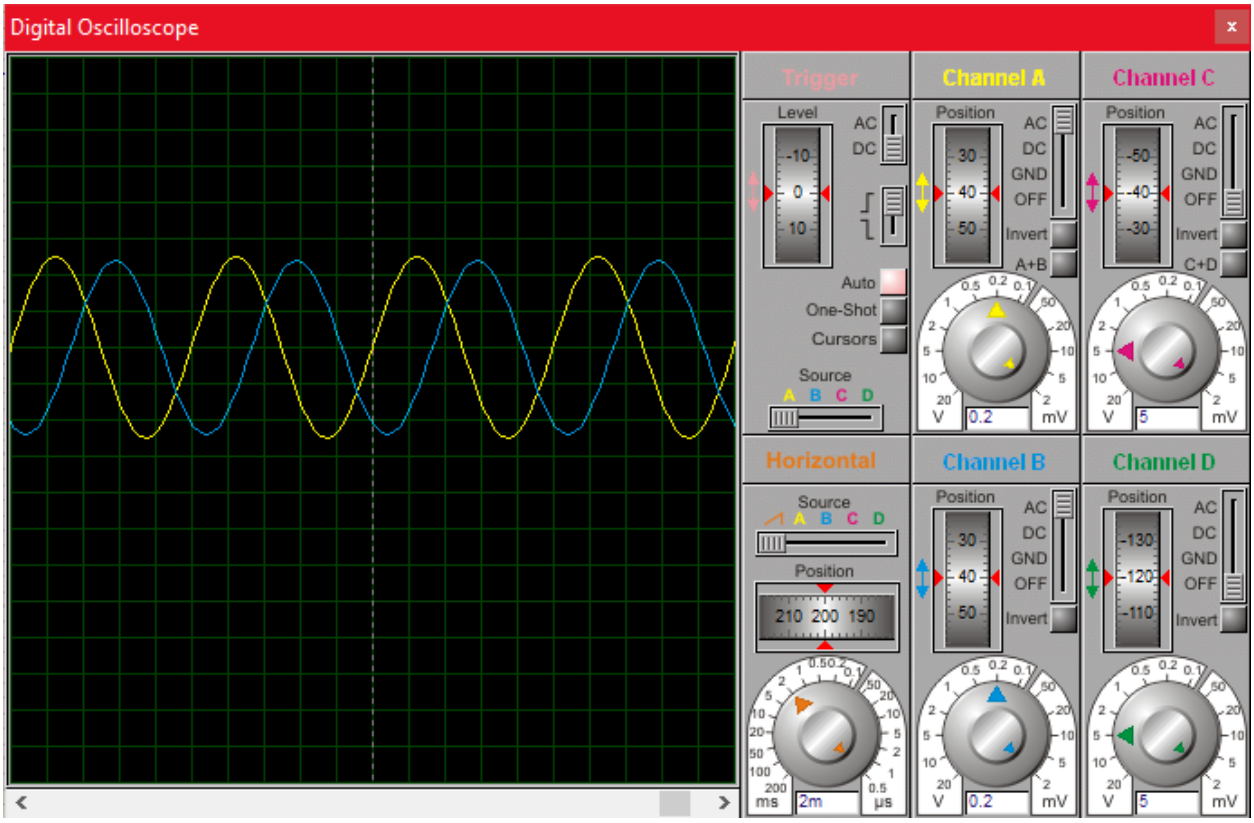


This is a good example of a distorted class A amplifier. (In the last screenshot:) as one could see, when the amplifier reaches the point of distortion, the output waveform (V_{OUT}: blue graph) the top and bottom portions of the waveform are slightly cutoff. If the amplifier is driven into greater distortion (when the input signal is very high), then the output waveform (V_{OUT}: blue graph) will go into further distortion and the clipping of both top and bottom portions of the output waveform. Looking at the screenshots above, the first screenshot represents a good working-class A amplifier (no distortion) and through the screenshots (the other two are incremental from the previous one) the last screenshot represents the output waveform (V_{OUT}: blue) in the beginning stage of distortion. In other words, when the amplifier is distorted, the output waveform is clipped at cutoff and saturation because the amplifier is overdriven (too large an input signal).

8. Replace R2 with a 1 KΩ and return to the previous Vin. What changes in your setup and in your Load Line?

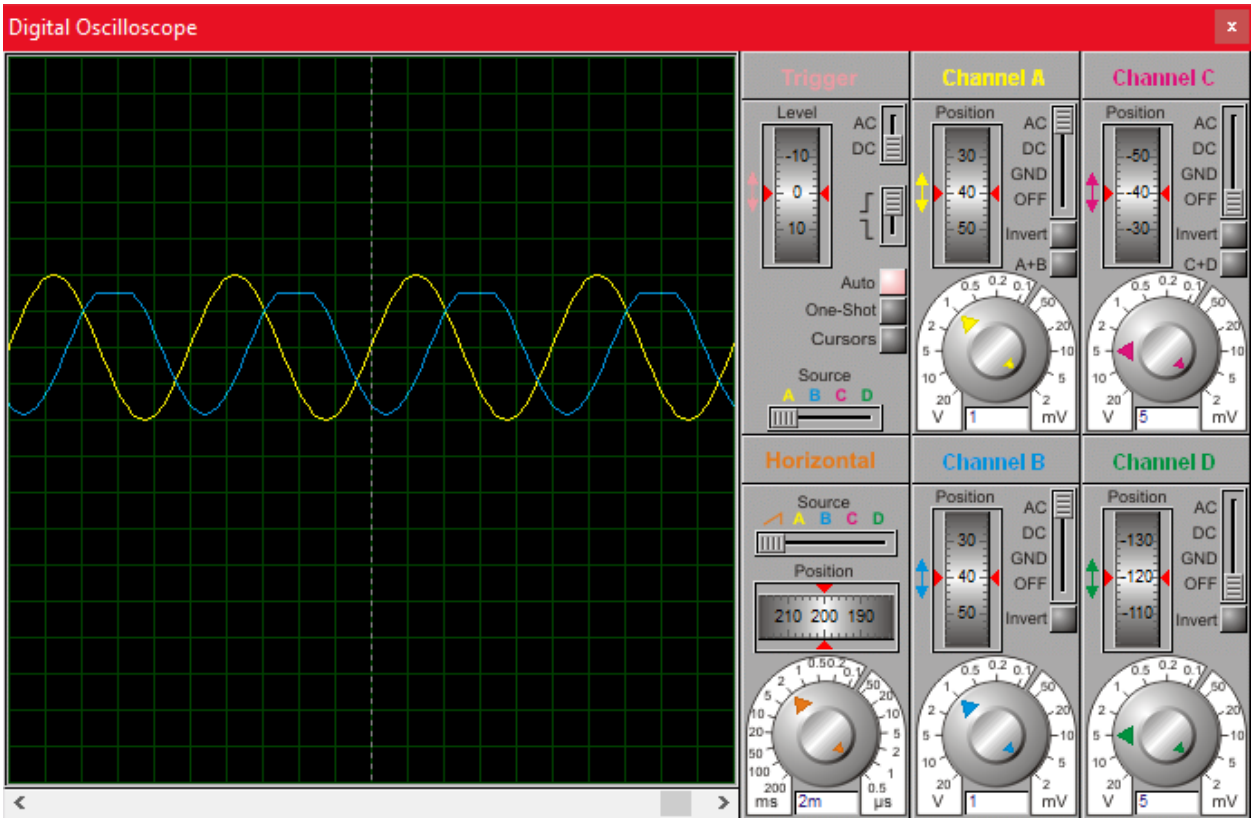
   The change in setup is that now instead of R2 being 2.7kΩ, it now became 1kΩ. This changes the load line, where the Q-point is no longer at the center position, causing other significant problems in the operation of the amplifier.

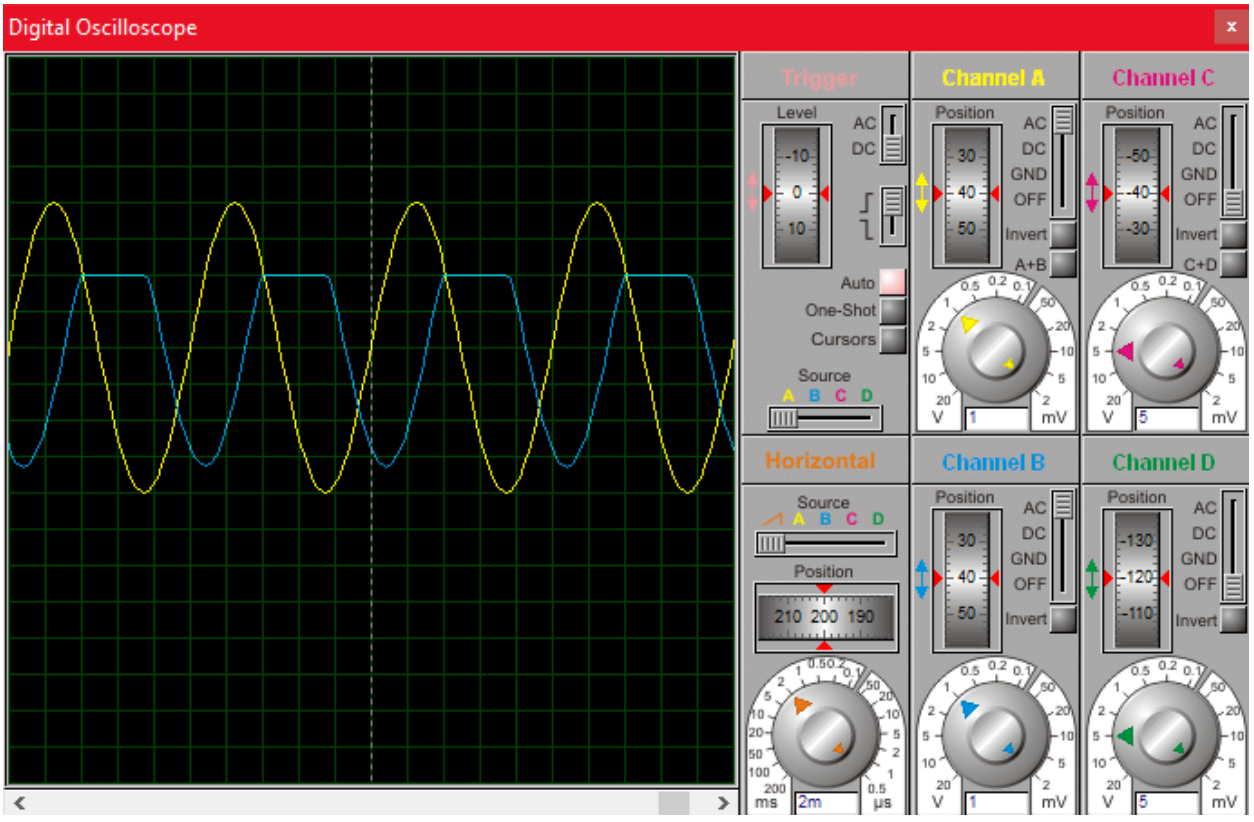
9. What are the impacts of this change on your output waveform? Screen shot. Explain.

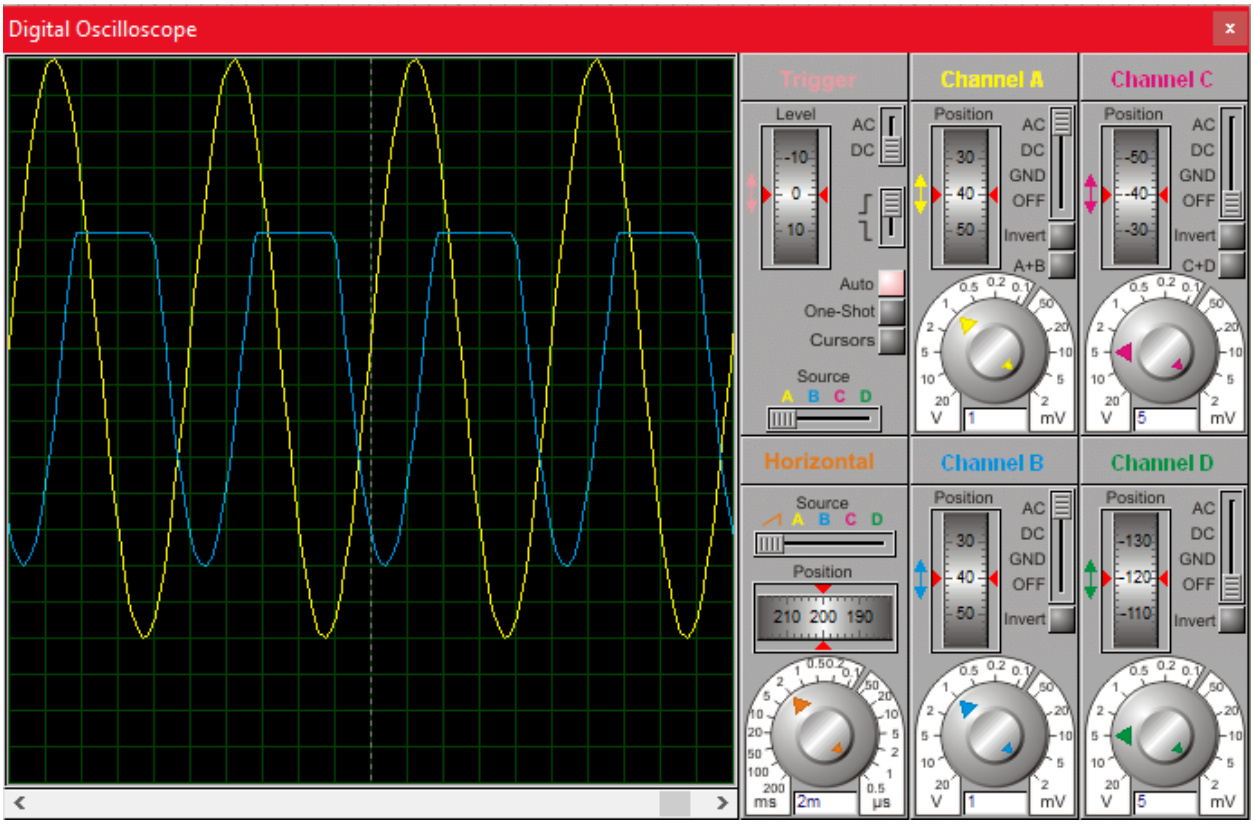


Looking to the screenshot above, when R2 is set to 1kΩ, the input waveform (V_{IN}: yellow graph) is almost identical to the to the output waveform (V_{OUT}: blue graph). The difference: the two waveforms are not "lined up" against each other. In other words, there is an offset between the two graphs (the output waveform is shifted to the right from the input waveform).

10. Slowly increase your input waveform. Explain what is happening. Screen shot. Compare with question 7. (keep R2 1k)







Looking back to question 7, the two scenarios are almost similar. In question 7, we observed what would happen when the amplifier was overdriven (when distortion occurred), where the top and bottom portions of the graphs were clipped. In this scenario, the amplifier is not distorted, but the amplifier's Q-point is not properly centered and the top portion of the output waveform (V_{OUT}: blue graph) is getting clipped (as seen in the last screenshot). Looking at the first screenshot above, the amplifier appears to be operating normally, but when the input signal gets bigger, the transistor goes into cutoff (as seen in the last screenshot). Essentially, what is happening here, is that the Q-point is limiting the output waveform (V_{OUT}: blue graph). If the input signal is to get bigger, then the amplifier will go deeper into cutoff.

Discussion/Conclusion:

This lab was a continuation from the last lab (lab 9), where in this lab, we dived deeper into class A amplifiers and voltage-divider bias circuits. During the beginning of the lab, we essentially completed a whole load line of a voltage-divider bias circuit by doing the appropriate calculations. Furthermore, we observed the behavior of the class A amplifier under certain situations. For example, we observed the behavior of the amplifier when the Q-point was off center. To observe the behaviors, we used Proteus to create BJT class A amplifier simulations by replicating the circuits given to us and using the appropriate steps (i.e. using virtual scope) to observe the behaviors.