Course Outline

FACULTY:	**Faculty of Science and Technology**
PROGRAM(S):	243.A0
DEPARTMENT:	Computer Engineering Technology
COURSE TITLE:	Digital Systems Design using HDL
COURSE NUMBER:	247-512-VA
COURSE SECTION(S):	00001
PONDERATION:	2-4-2
NUMBER OF CREDITS:	2.66 credits
PREREQUISITE(S):	
SEMESTER/YEAR:	Fifth semester Autumn 2021
TEACHER (THEORY):	Manijeh Khataie Office: K309 Tel: 514-744-7500 Ex. E-mail: khataiem@vaniercollege.qc.ca
AVAILABILITY:	Office Hours: Wednesday 11:30am to 12:30pm or by prior appointment.
TEACHER (LAB):	Manijeh Khataie Office: K309 Tel:
AVAILABILITY:	

Course Description:

In this course, student will learn to design, simulate, and build combinational logic and sequential circuits. They will learn how to use relevant CAD tools and design technologies used in industry today. They will design projects by implementing a representative collection of combinational and sequential circuits using the same tools as are prevalent in industry.

They will learn the timing problems encountered by fast digital signals. Students will program using HDL (Hardware Description Language). Students will implement hierarchical design; simulate waveforms, prepare pin assignments and different circuit components on a PLD chip using vendor-specific IDEs. They will design on a specific FPGA or CPLD board and know the difference between the two technologies.

Statement of Competency

037V To perform activities related to designing a computerized system.

Competency

1. Focus on the desired objectives.
2. Look for information
3. Develop the design.
4. Validate the design.
5. Document the project.

Bibliography (required according to MEES)

- Digital Fundamentals, A Systems Approach. Thomas L. Floyd.
- Digital Design Using Digilent FPGA Boards, Verilog. Richard E. Haskell.

Week	**Theory topics** (Sequence subject to change)	**Tentative lab activities** (Sequence subject to change)
1	Course Outline. Review basis of digital logic.	Lab1: Introduction to Digilent Basys2 board
2	Review SOP and POS. Introduction to programmable logic devices (PLD). Verilog test bench	Lab1
3	Introduction to Verilog HDL	Lab2: Behavioral logic design and Verilog test bench and simulation
4	Introduction to Field Programmable Gate Array (FPGA) architecture.	Lab3: 7-seg hierarchy design
5	Combinational Logic, Verilog test bench and top module	Lab4: Sequential logics in Verilog
6	Dataflow Modeling	Lab4
7	***Test ***	Lab5: Sequential counter in Verilog
8	Behavioral Modeling	Lab5
9	Behavioral Modeling	Lab5
10	Sequential logic design in Verilog • Register • Counters	Lab6: Combinational lock using FSM
11	Finite State Machine	Lab6
12	Finite State Machine	Lab7: Timed triggered event using FSM
13	Advanced finite state machine design in HDL design.	Lab7
14	*review*	Lab8 FSMD
15	***Final exam***	Lab catch-up

Course Structure		
THEORY:	2 hours/week:	Quiz, lecture, demonstration, problem solving, and discussion with student participation.
LABORATORY:	4 hours/week:	The student will perform typical tasks in programming an embedded system.
HOMEWORK:	2 hours/week:	The student will be expected to devote at least 2 hours per week to homework, reading datasheets and other documents.

ATTENDANCE	
THEORY:	Consistent attendance is strongly recommended. **Students are responsible for obtaining all material covered during any absence.**
LABORATORY:	Laboratory sessions are part of assessment activities. Failure to complete lab activities assigned in the designated lab class without just cause may result in a failure of the lab session and any results and/or lab report derived from the session. In order to meet and be evaluated on the course competencies lab attendance is required. Note that there is both a separate and an integrated **professionalism** mark associated with the course (see below). During the lab periods, you are expected to work on your assignments. It is not permitted to use the internet during lab periods outside the scope of the lab.
TESTS:	Absence will result in failure of the missed test (mark of 0). Students with a just cause for absence are encouraged to seek alternative arrangements with the instructor – beforehand if possible.

EVALUATION		
The final mark will be weighted:	65% theory:	15% Homework and Quizzes 25% Midterm Test 25% Final Test
	35% lab work:	30% laboratory practice and report 5% English proficiency/Professionalism
	Total:	**100%**

The following general rules apply:

- A minimum mark of 60% is required to pass the course **AND** at least 50% in the Theory portion **AND** at least 50% in the Lab portion. If the mark is less than 50% for either the Theory o**r** Lab portion, the total mark will not exceed 55%.
- At least one week's notice will be given for test dates or changes in test dates.
- Tests questions will not be re-graded after 24 hours of returning and any altered material will not be re--graded
- Quizzes may be given without prior notice – there are no make-ups for quizzes.
- Students are expected to attend all their schedule classes.
  - Absence from any lab class where specific skills are being assessed will result in a failure of that skill.
- **Students are expected to conduct themselves in a professional manner at all times.** This includes but is not limited to:
  - Arriving to class (theory and laboratory) on time and prepared to do the required work;
  - Conducting themselves in an appropriate manner at all times (including being respectful to the teacher, classmates, and any guests);
  - Using professional language (no cursing and/or swearing and using appropriate vocabulary);
  - Arriving to class/lab with all necessary supplies (logbook, notebook, textbook, manual, paper, writing implements, calculator, etc.);
  - Turning off all personal communication/music/video electronics (removing headphones, earphones, ear buds etc.); and
  - Having all assigned work completed.

  Remember that developing professional behaviours and habits now is an important aspect of preparation for entering a professional work environment in the future.
- Students are expected to take their own notes during classes.
- Calculators with memory for equations (for example graphing calculators) will not be allowed when writing tests.
- Reports must be typed and computer generated according to the guidelines provided by the teacher.
- When requested, Lab preparations and Lab Results/logbooks are to be handed in during the lab session. Late Lab Preparations/Lab Results may not be accepted, and a zero mark will be recorded.
- Reports are due two weeks after they are assigned unless the instructor provides a specific due date.
- Any assigned work submitted beyond 1 week late may not be accepted, and a zero mark may be recorded. Assigned work up to and including one week late may be reduced by up to 25% of the maximum mark.
- In-class assignments will only be accepted in the class in which they are assigned.
- Students who are consistently late for class (lab and/or theory) may be refused entry.
- All grades are reported on a numeric scale from 0% to 100%. The following categories briefly describe the relative value of these grades.

range	mean	Description
90 - 100	**95**	Excellent, mastery of the objectives
80 - 89	**85**	Very Good mastery of the objectives
65 - 79	**72**	Good, mastery of objectives
60 - 64	**62**	Fair mastery of objectives

0 - 59	n/a	Poor mastery of objectives

Academic and other Resources

If at any point in the semester, you are concerned about the course or you realise that you are having academic difficulties; your first resource should be to talk to me, your teacher. Academic difficulties include problems with the understanding of the theory, to the development of the practical skills required by the course. The earlier you look for help, the greater your chances of succeeding in the course. If I don't feel I can provide you with the help you need then I may recommend one of the College resources below.

For other problems or difficulties, you may encounter while at Vanier there are a number of Services available to help you within the college. They are there for you to use. These include:

Student Services (C203): Some areas where they provide services and/or information are:

Services for students with disabilities	Counselling (personal and other problems)
Student Advocate	Financial Aid (including aid and scholarships)
Health Services (Nurse on staff)	Student Employment
Academic and Behaviour Policies	Lockers
Housing	Volunteering

Student Services is a great resource for questions about college life and any problems you encounter while at Vanier. If they do not have the answer, they can direct you to the right place to find it.

Tutoring and Academic Success Center - TASC (F-300): Student-orientated centre dedicated to promoting and aiding students' development and success in academics and in society.

Admissions and placement tests	S.T.A.R. Program
English Exit Exam	English conversation and pronunciation clubs
English Peer Tutoring	Scholarship information
Vanier Native Program	Diversity support

TASC is the main college resource for students with learning difficulties and for students with weak English language skills.

Science, Technology, Engineering and Mathematics - STEM (D-301): This Centre aims to promote student success in mathematics and science. The large interactive study space includes a hackerspace for hands-on applied projects such as robotics, and a study hub for collaborative group work. Teacher help, computers, and a large collection of math and science textbooks are equally available. We offer a number of activities, services and resources including:

Free drop-in peer tutoring	Drop-in help from teachers
Free private tutoring	Teacher-led review sessions
Computer access	Laptop borrowing

Mediation and Grades Review

There are two committees available to the student for resolution of academic complaints.

1. The *Grades Review Committee* to review complaints concerning the grading of students' work.
2. The *Faculty Mediation Committee* to review academic complaints other than those dealing with student grades – see *Student Academic Complaints* below.

Information on College Policies

It is the student's responsibility to be familiar with and adhere to Vanier College Academic Policies. A summary of the course-level academic policies that apply in this and all other Vanier courses can be found in Omnivox under Important Vanier Links, or by following this link

http://www.vaniercollege.qc.ca/psi/course-level-policies/

Complete policies can also be found on the Vanier College website, under Policies.