Computational Logic Circuits (Lab 6)

zyBooks & MUX/3-to-8 decoder

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OBJECTIVES

- To understand the topics covered in zyBooks for this week's lab.
- To understand the functions of a 4-to-1 MUX and MUXs in general.
- Understand 74180 and 74280 chips.

DESIGN

Experiment

- There were two parts in this lab. First, we asked to read from chapter 6.1 to 6.5 in our zyBooks. Then, we had to build two separate circuits. The first circuit was a 4-to-1 multiplexer. The second, was a 3-to-8 decoder. The multiplexer had 4 inputs and 1 output. The decoder had 3 inputs and 8 separate outputs. An expression was given: $F = A'B'C' + A'BC' + A'BC + AB'C$ to implement into our circuits. The instructor verified the operation of the circuits. Below outlines my work from the lab.

SCHEMATICS

Schematics from the Experiment

The schematic for the 9-bit parity checker is on the attached paper of this report.

QUESTIONS

Questions from the Experiment

What is a parity bit?

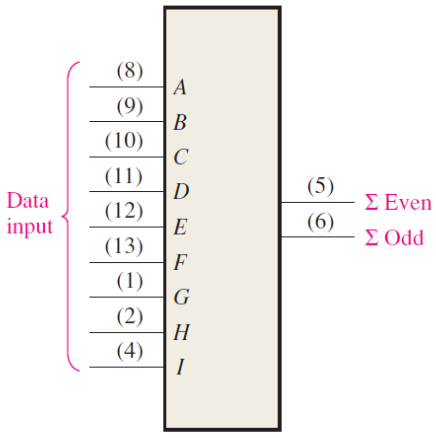
- A parity bit indicates if the number of 1s in a code is even or odd for the purpose of error detection.

What is a parity checker?

- A parity checker is the process that ensures accurate data transmission between nodes during communication.

What are the functions of the 74280 chips?

- This particular device can be used to check for odd or even parity on a 9-bit code (eight data bits and one parity bit), or it can be used to generate a parity bit for a binary code with up to nine bits. The inputs are *A* through *I*; when there is an even number of 1s on the inputs, the ∑ Even output is HIGH and the ∑ Odd output is LOW.



(a) Traditional logic symbol

Number of Inputs *A–I* that Are High	Outputs Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

(b) Function table

Source: Digital Fundamentals, Eleventh Edition, Thomas L. Floyd, 2015.