Pianodo Project Update Report

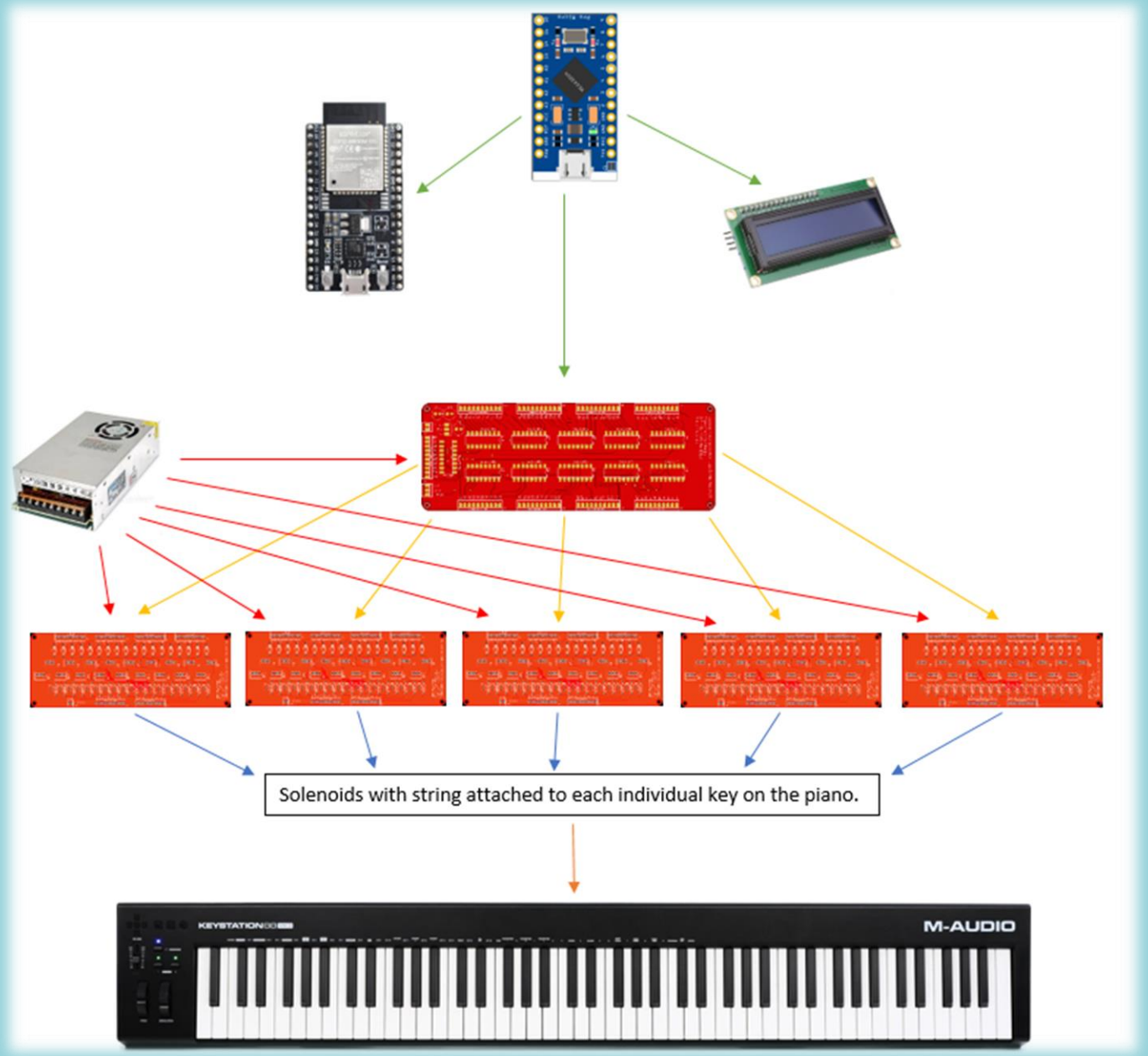
Presentation by Leonardo Fusser
Project Planning & Design
Mohamed Tavakoli

Outline

- Recap of Pianodo (re-visit)
- Arduino pro micro board overview
- ESP32 development board overview
- 16x2 with I2C module overview
- Solenoid control and control board overview
- Logic control and control board overview
- Next steps...

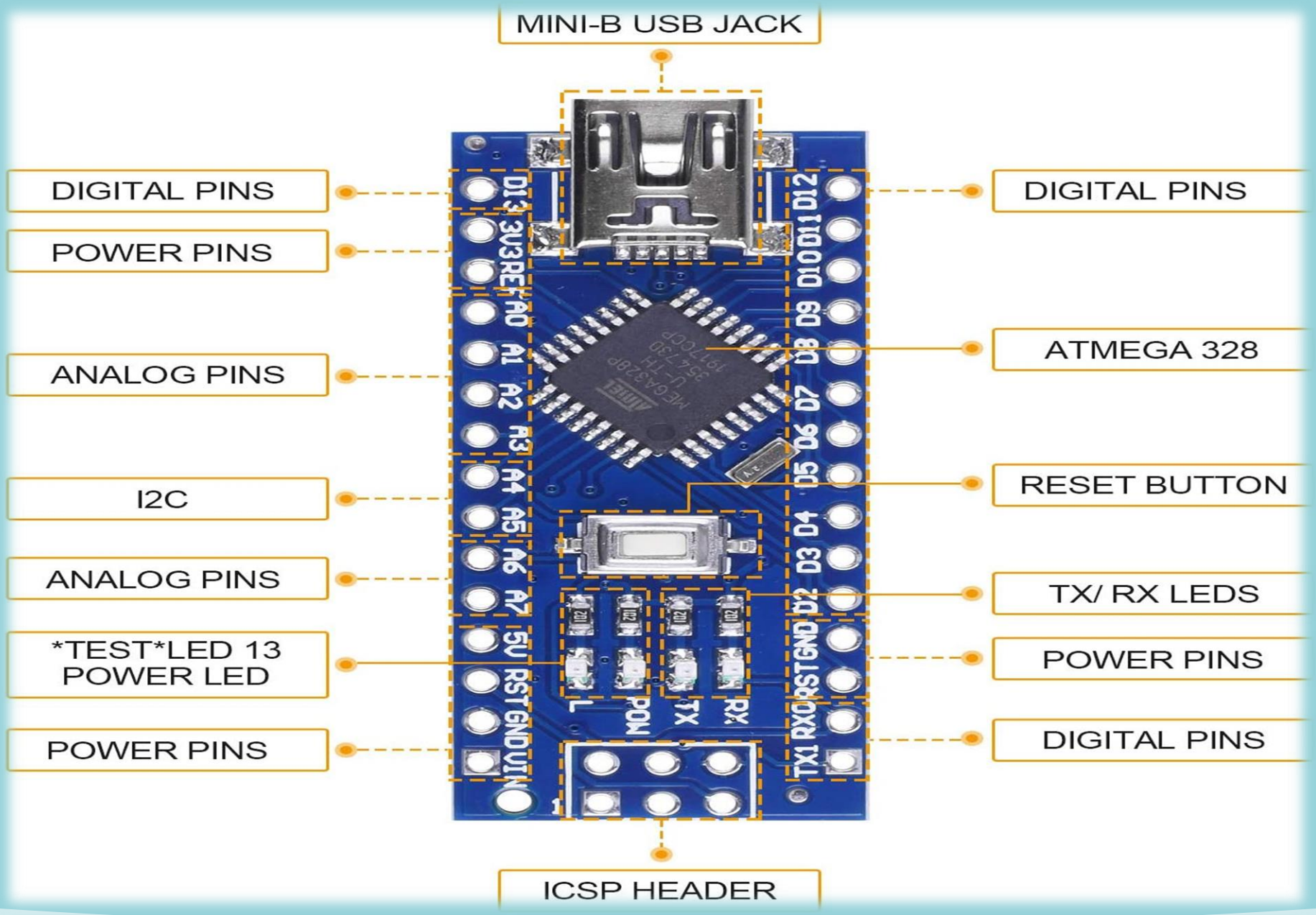
Basic overview of Pianodo

A quick look at what it is again…


Solenoids with string attached to each individual key on the piano.
KEYSTATION
M-AUDIO

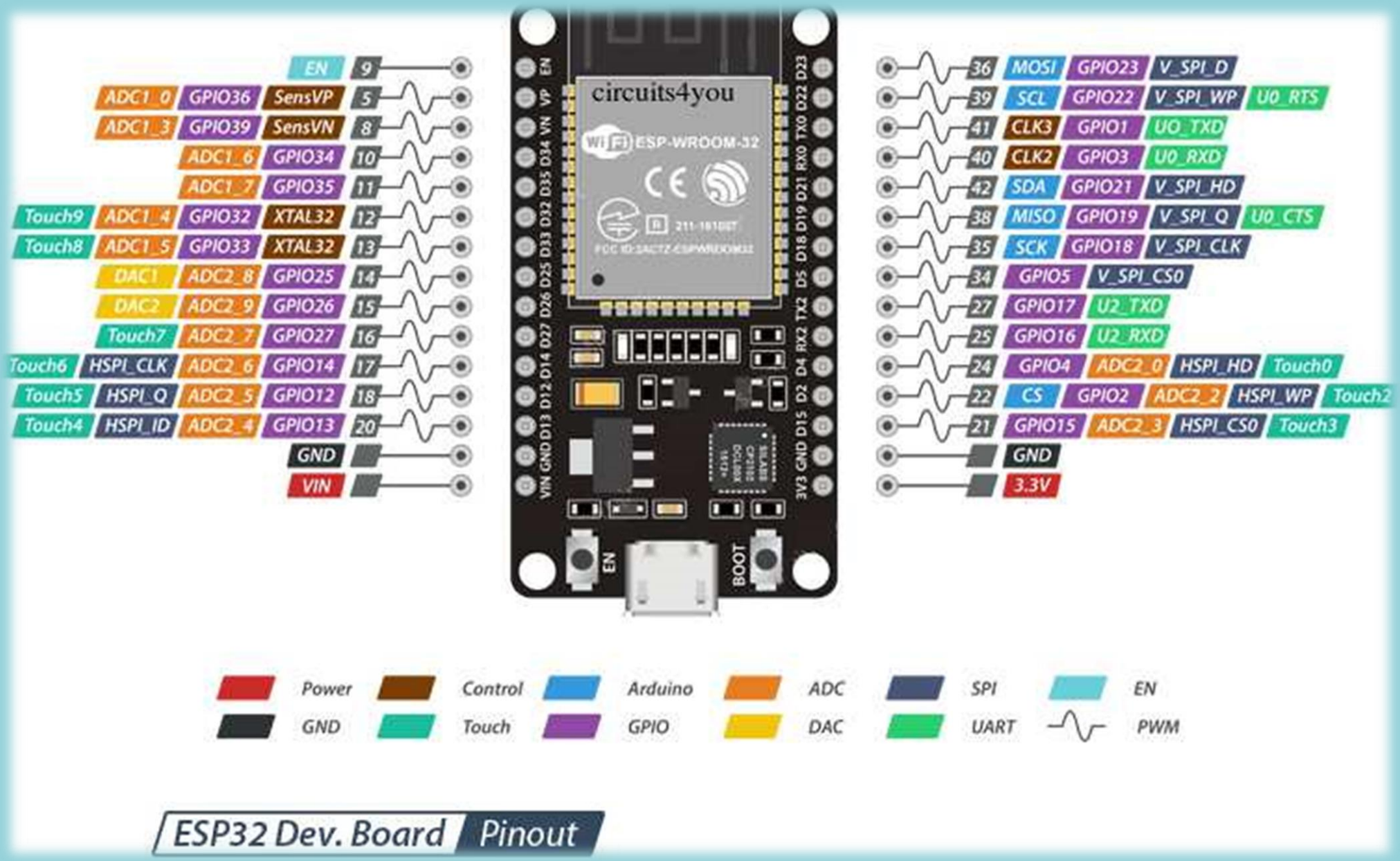
Arduino pro micro board

A quick overview of the board…


MINI-B USB JACK
DIGITAL PINS
POWER PINS
ANALOG PINS
I2C
ANALOG PINS
*TEST*LED 13
POWER LED
POWER PINS
ICSP HEADER
DIGITAL PINS
ATMEGA 328
RESET BUTTON
TX/ RX LEDS
POWER PINS
DIGITAL PINS

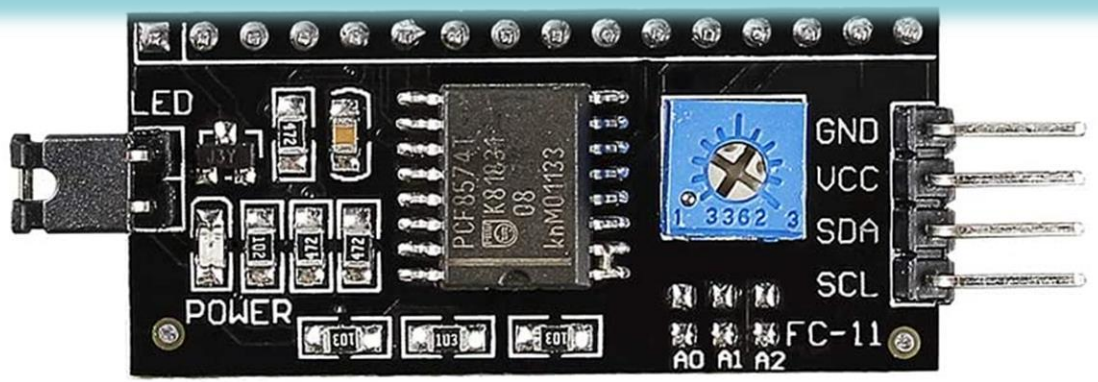
ESP32 development board

A quick overview of the board…


EN 9
ADC1_0 GPIO36 SensVP 5
ADC1_3 GPIO39 SensVN 8
ADC1_6 GPIO34 10
ADC1_7 GPIO35 11
Touch9 ADC1_4 GPIO32 XTAL32 12
Touch8 ADC1_5 GPIO33 XTAL32 13
DAC1 ADC2_8 GPIO25 14
DAC2 ADC2_9 GPIO26 15
Touch7 ADC2_7 GPIO27 16
Touch6 HSPI_CLK ADC2_6 GPIO14 17
Touch5 HSPI_Q ADC2_5 GPIO12 18
Touch4 HSPI_ID ADC2_4 GPIO13 20
GND
VIN
circuits4you
ESP-WROOM-32
EN
BOOT
36 MOSI GPIO23 V_SPI_D
39 SCL GPIO22 V_SPI_WP U0_RTS
41 CLK3 GPIO1 U0_TXD
40 CLK2 GPIO3 U0_RXD
42 SDA GPIO21 V_SPI_HD
38 MISO GPIO19 V_SPI_Q U0_CTS
35 SCK GPIO18 V_SPI_CLK
34 GPIO5 V_SPI_CS0
27 GPIO17 U2_TXD
25 GPIO16 U2_RXD
24 GPIO4 ADC2_0 HSPI_HD Touch0
22 CS GPIO2 ADC2_2 HSPI_WP Touch2
21 GPIO15 ADC2_3 HSPI_CS0 Touch3
GND
3.3V
Power
Control
Arduino
ADC
SPI
EN
GND
Touch
GPIO
DAC
UART
PWM
ESP32 Dev. Board Pinout

16x2 LCD with I2C module

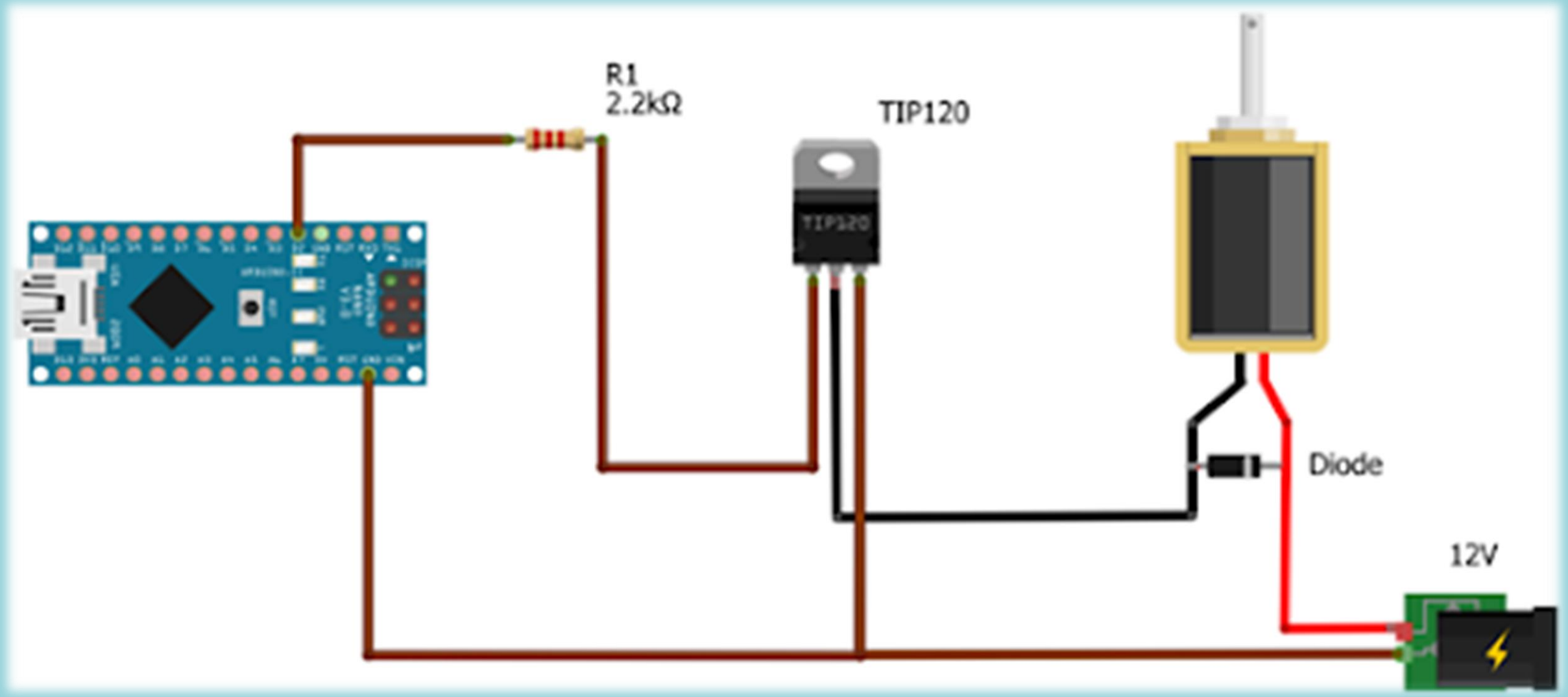
A quick overview of the LCD display...


LED
POWER
PCF8574T
GND
VCC
SDA
SCL
FC-11
A0 A1 A2


1
16
VSS VDD VO RS RW E D0 D1 D2 D3 D4 D5 D6 D7 A K
Hello,world!
SunFounder

Solenoid control & control board overview

A quick look at how the solenoids are controlled and the PCB that holds the circuitry…


R1
2.2kΩ
TIP120
TIP120
Diode
12V

TIP120, TIP121, TIP122 (NPN); TIP125, TIP126, TIP127 (PNP)

Plastic Medium-Power Complementary Silicon Transistors

Designed for general−purpose amplifier and low−speed switching applications.

Features

- High DC Current Gain −
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage − @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) − TIP120, TIP125
  = 80 Vdc (Min) − TIP121, TIP126
  = 100 Vdc (Min) − TIP122, TIP127
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- Pb−Free Packages are Available*

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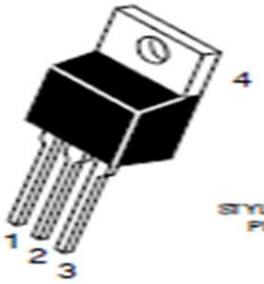
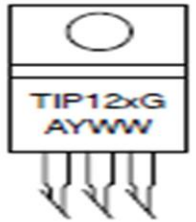
DARLINGTON
5 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60−80−100 VOLTS, 65 WATTS



TO−220AB
CASE 221A
STYLE 1

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

MARKING DIAGRAM



TIP12x	= Device Code
x	= 0, 1, 2, 5, 6, or 7
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

TIP120, TIP121, TIP122 (NPN); TIP125, TIP126, TIP127 (PNP)

MAXIMUM RATINGS

Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}		5.0		Vdc
Collector Current – Continuous – Peak	I_C		5.0 8.0		Adc
Base Current	I_B		120		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		65 0.52		W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D		2.0 0.016		W W/°C
Unclamped Inductive Load Energy (Note 1)	E		50		mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}		−65 to +150		°C

THERMAL CHARACTERISTICS

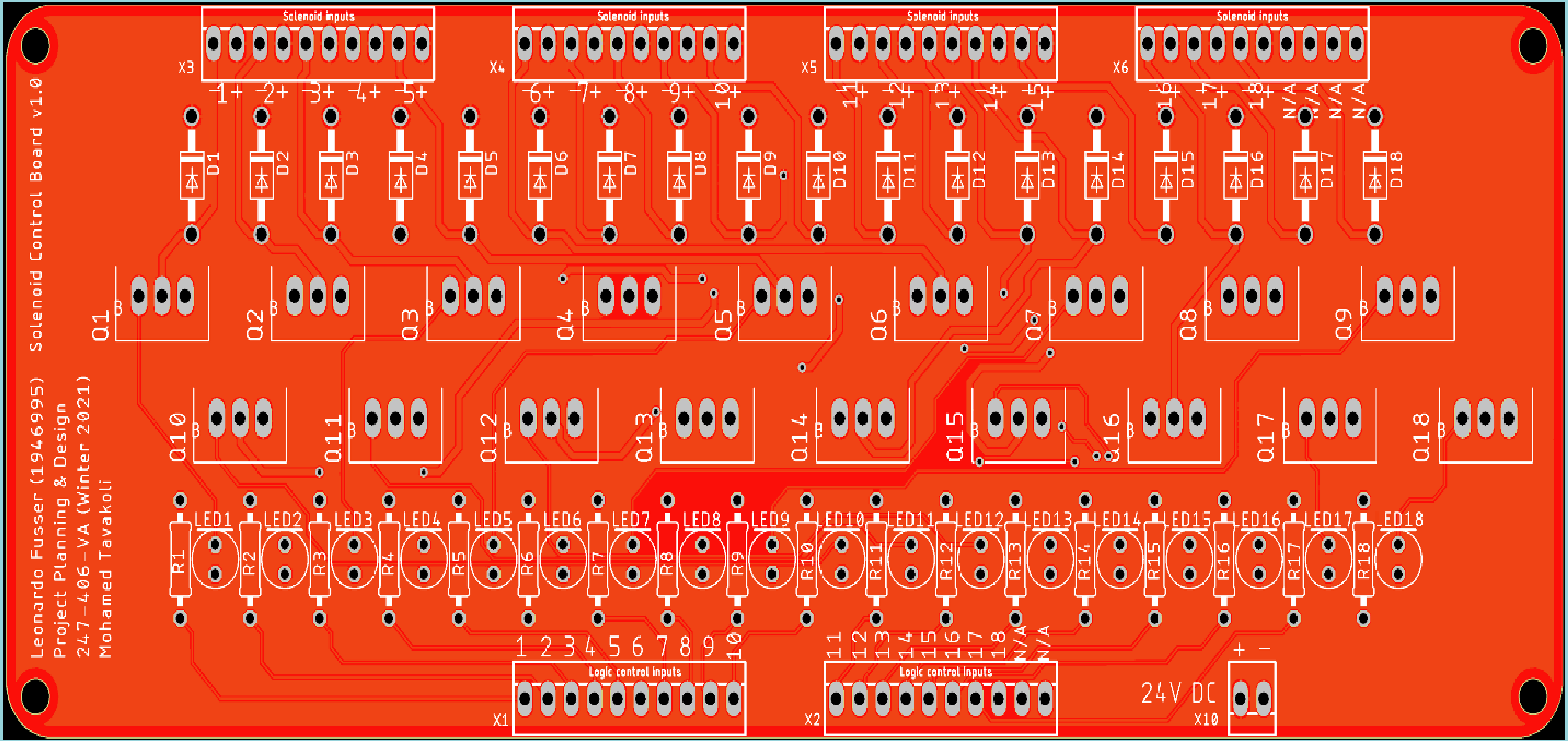
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	62.5	°C/W

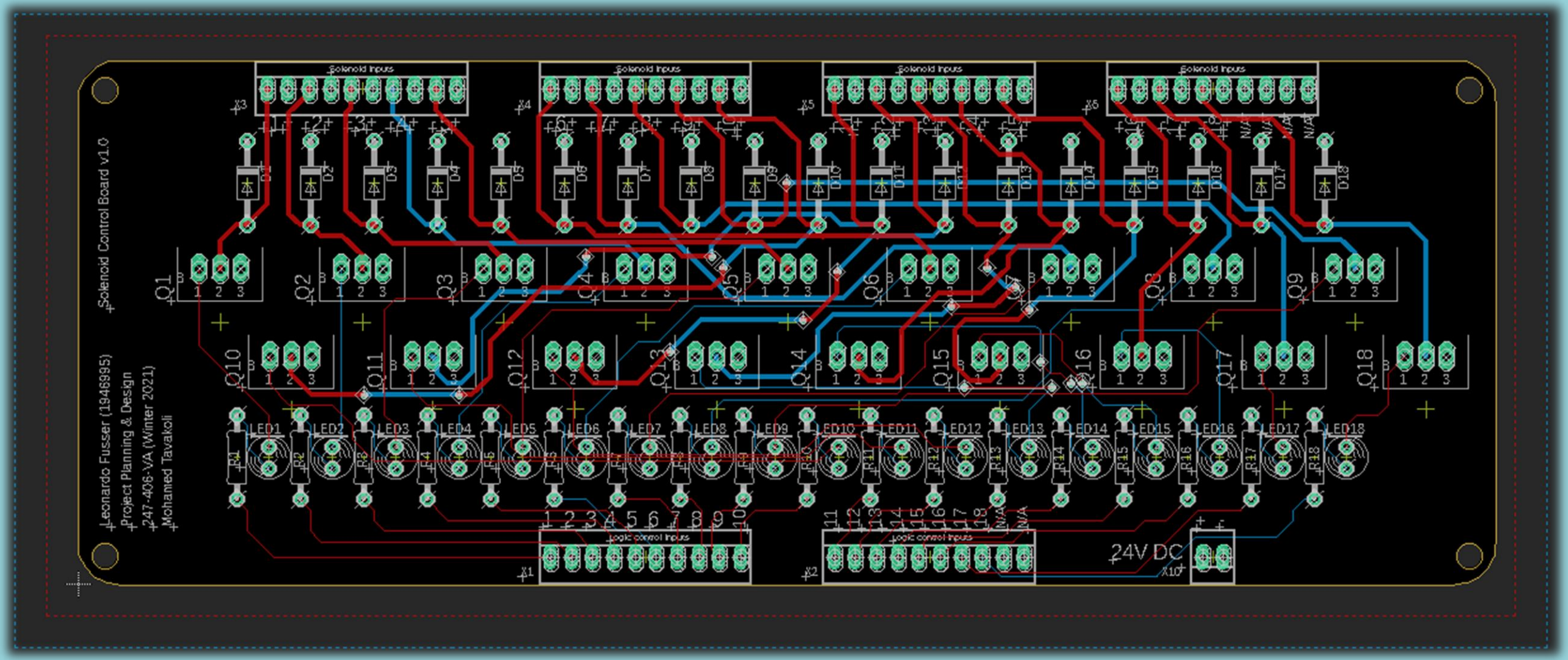
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_C = 1 A, L = 100 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

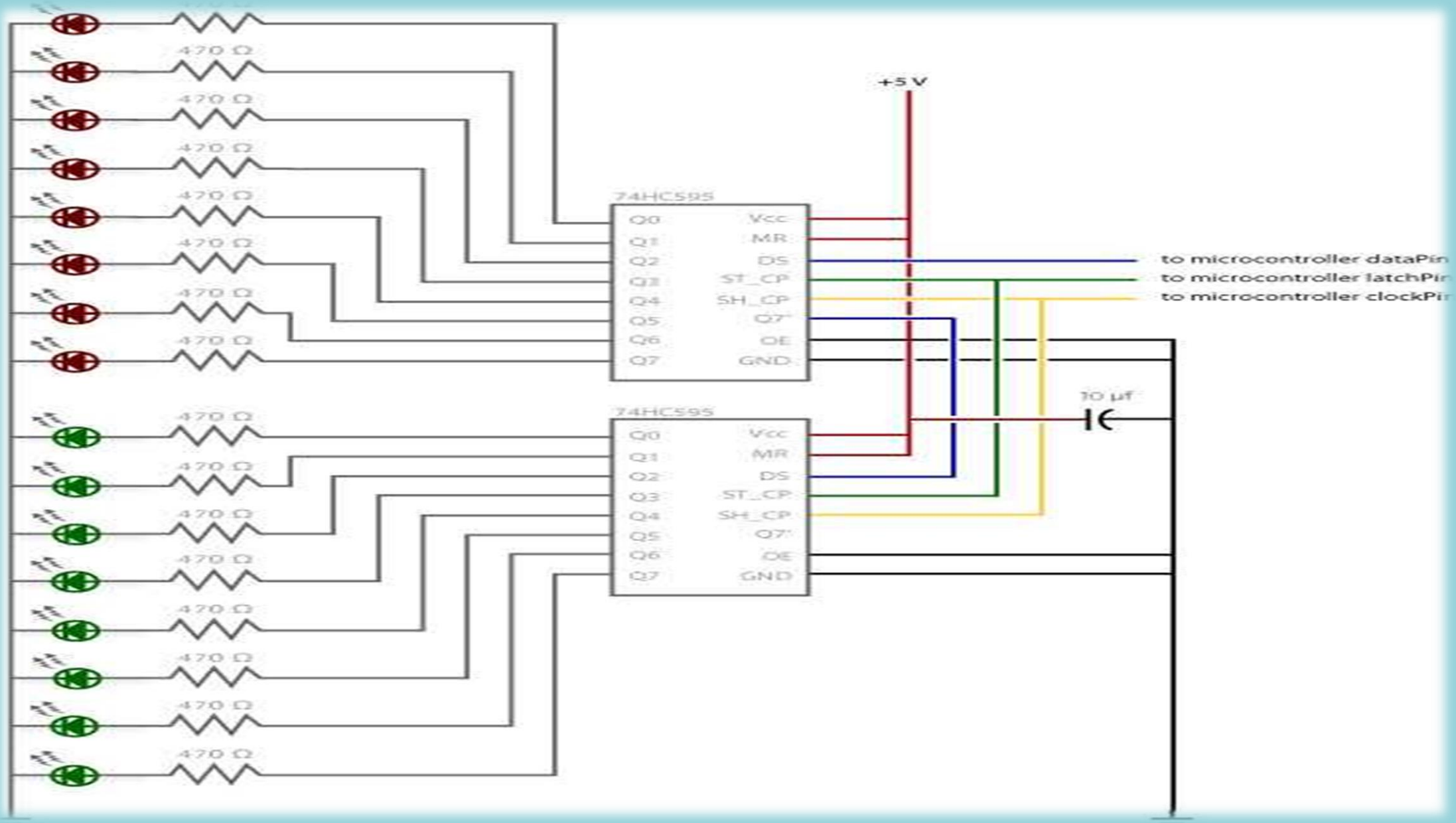
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 2) (I_C = 100 mAdc, I_B = 0)	TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	$V_{CEO(sus)}$	 60 80 100	 – – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	I_{CEO}	 – – –	 0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	I_{CBO}	 – – –	 0.2 0.2 0.2	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (Note 2)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000 1000	– –	–
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 5.0 Adc, I_B = 20 mAdc)		$V_{CE(sat)}$	 – –	 2.0 4.0	Vdc
Base–Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		h_{fe}	4.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz	TIP125, TIP126, TIP127 TIP120, TIP121, TIP122	C_{ob}	– –	300 200	pF


Solenoid inputs
Solenoid inputs
Solenoid inputs
Solenoid inputs
X3
X4
X5
X6
Solenoid Control Board v1.0
Leonardo Fusser (1946995)
Project Planning & Design
247-406-VA (Winter 2021)
Mohamed Tavakoli
Logic control inputs
Logic control inputs
X1
X2
24V DC
X10

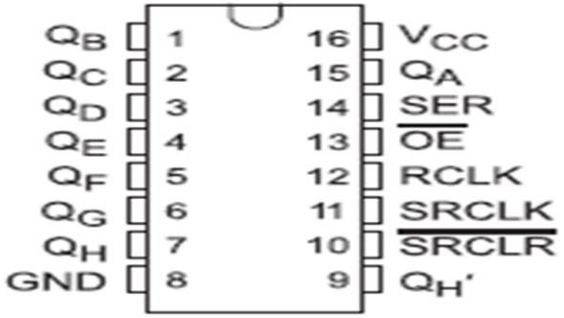

Solenoid Control Board v1.0
Leonardo Fusser (1946995)
Project Planning & Design
247-406-VA (Winter 2021)
Mohamed Tavakoli
Solenoid Inputs
Logic control Inputs
24V DC

Logic control & control board overview

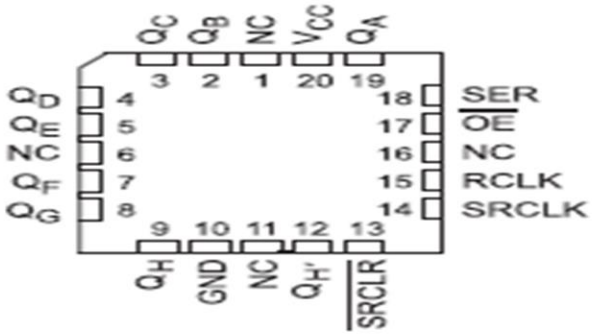
A quick look at how the digital logic works and the PCB that holds the circuitry…


470 Ω
74HC595
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Vcc
MR
DS
ST_CP
SH_CP
Q7'
OE
GND
+5 V
10 µF
to microcontroller dataPin
to microcontroller latchPin
to microcontroller clockPin

D, N, NS, J, DB, or PW Package
16-Pin SOIC, PDIP, SO, CDIP, SSOP, or TSSOP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, PDIP, SO, CDIP, SSOP, or TSSOP	LCCC		
GND	8	10	—	Ground Pin
$\overline{OE}$	13	17	I	Output Enable
Q_A	15	19	O	Q_A Output
Q_B	1	2	O	Q_B Output
Q_C	2	3	O	Q_C Output
Q_D	3	4	O	Q_D Output
Q_E	4	5	O	Q_E Output
Q_F	5	7	O	Q_F Output
Q_G	6	8	O	Q_G Output
Q_H	7	9	O	Q_H Output
$Q_{H'}$	9	12	O	$Q_{H'}$ Output
RCLK	12	14	I	RCLK Input
SER	14	18	I	SER Input
SRCLK	11	14	I	SRCLK Input
$\overline{SRCLR}$	10	13	I	$\overline{SRCLR}$ Input
NC	—	1 16 11 16	—	No Connection
V_{CC}	—	20	—	Power Pin

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current (2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

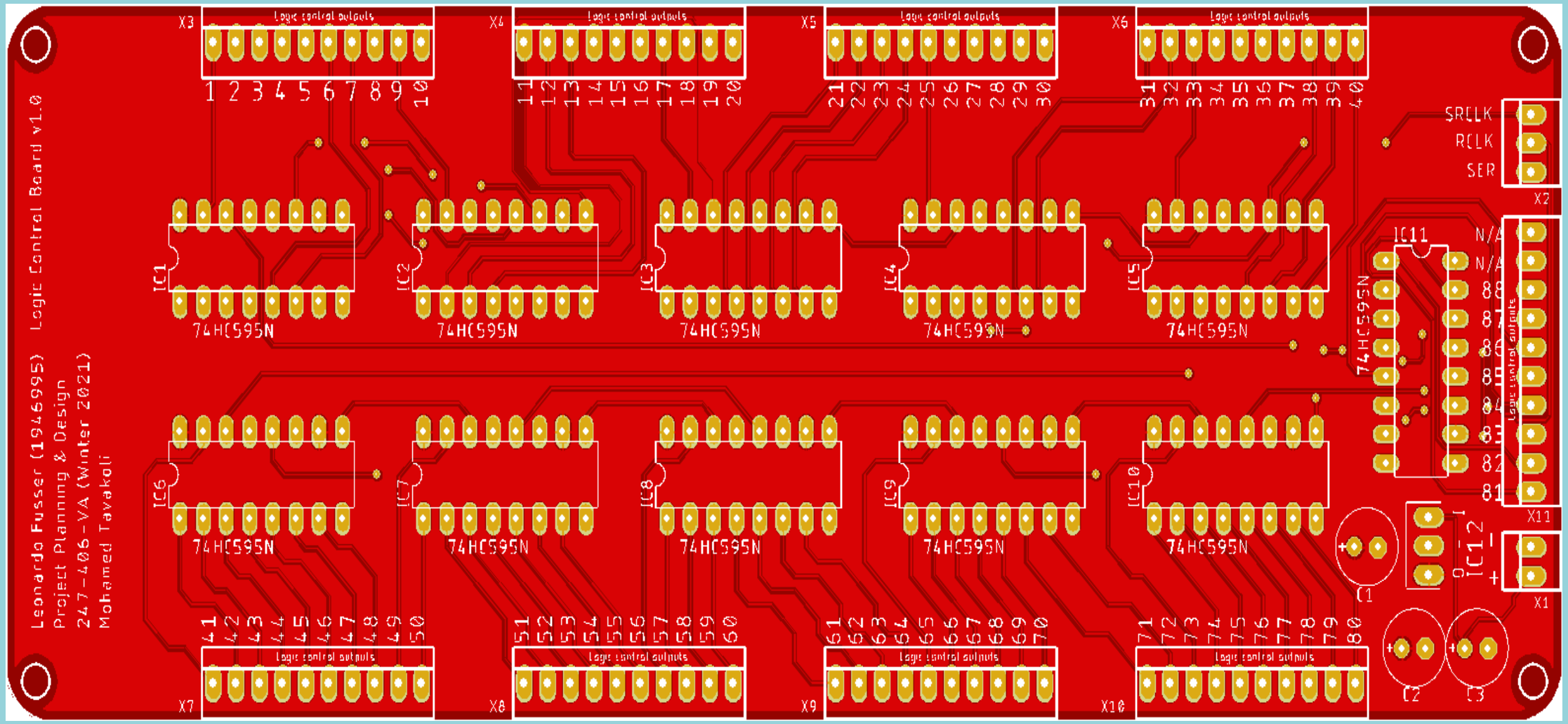
			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

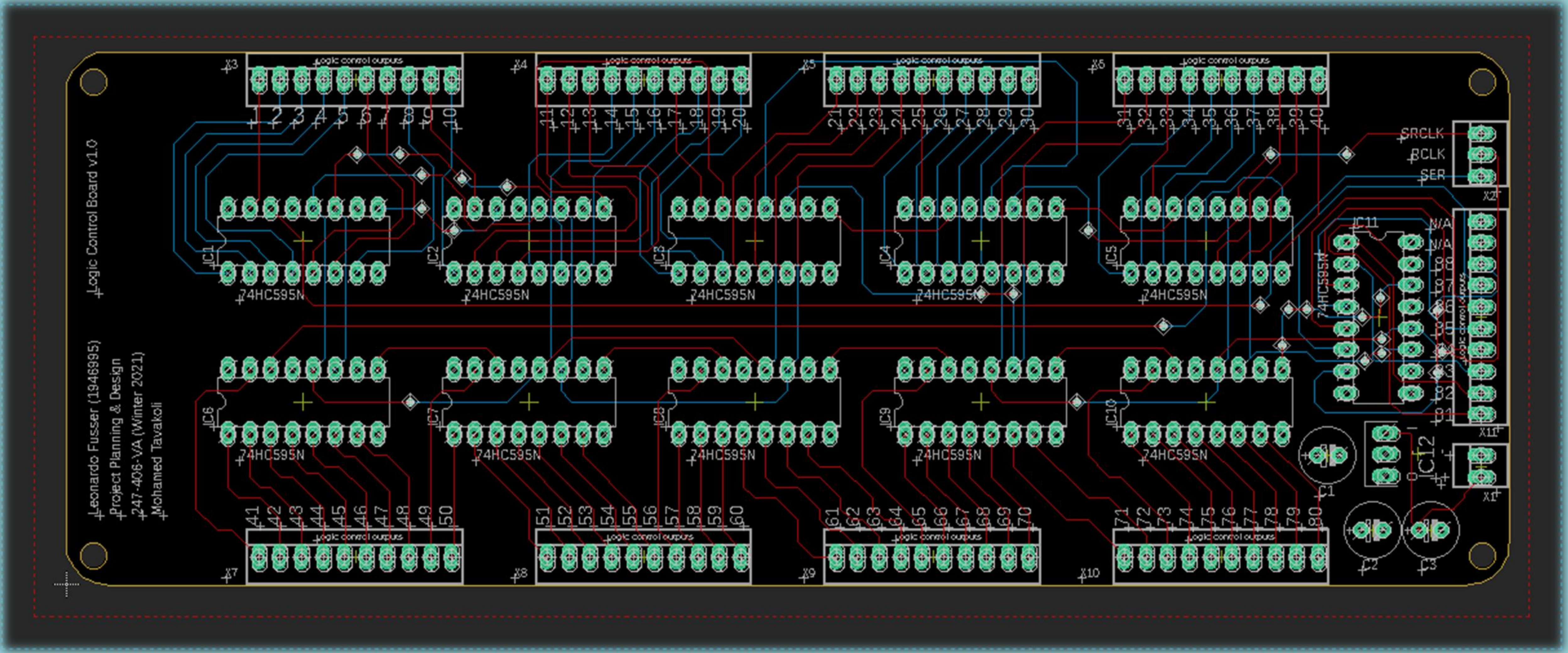
(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54HC595			SN74HC595			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall time(2)	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C


Leonardo Fusser (1946995) Logic Control Board v1.0
Project Planning & Design
247-406-VA (Winter 2021)
Mohamed Tavakoli
X3
X4
X5
X6
X7
X8
X9
X10
X11
X12
Logic control outputs
1 2 3 4 5 6 7 8 9 10
11 12 13 14 15 16 17 18 19 20
21 22 23 24 25 26 27 28 29 30
31 32 33 34 35 36 37 38 39 40
41 42 43 44 45 46 47 48 49 50
51 52 53 54 55 56 57 58 59 60
61 62 63 64 65 66 67 68 69 70
71 72 73 74 75 76 77 78 79 80
SRCLK
RCLK
SER
X2
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
IC11
74HC595N
N/A
N/A
88
87
86
85
84
83
82
81
C1
C2
C3


Logic Control Board v1.0
Leonardo Fusser (1946995)
Project Planning & Design
247-406-VA (Winter 2021)
Mohamed Tavakoli
logic control outputs
74HC595N
SRCLK
RCLK
SER

Next steps

What's next for Pianodo...

Next steps

- Waiting for final electrical components to arrive.
- Assembly of all electrical components to PCBs.
- Assembly of project with electricals.
- Programming the boards.
- Esthetics and final touch-ups.