# **247 Computer Engineering Technology**

AUTUMN 2017 Digital Circuits I (247-107)

# **Lab 3**Logic Gates

# NOTE:

To be completed during the lab session This exercise is to be done **individually** except where specified in the procedure. **Each** student must submit a lab report by the end of the lab.

- 1. **Watch YouTube** (Digital Electronics: Logic Gates Integrated Circuits Part 1) at <a href="https://www.youtube.com/watch?v=cdMJvFT-Afc">https://www.youtube.com/watch?v=cdMJvFT-Afc</a>
- 2. Watch YouTube at <a href="https://www.youtube.com/watch?v=Ax230XQof1I">https://www.youtube.com/watch?v=Ax230XQof1I</a>

#### **LOGIC GATES**

AIM: To study and verify the truth table of logic gates LEARNING OBJECTIVE:

• Identify various ICs and their specification.

**COMPONENTS REQUIRED:** 

- Logic gates (IC) trainer kit.
- Wires.
- IC 7400, IC 7408, IC 7432, IC 7406, IC 7402, IC 7404

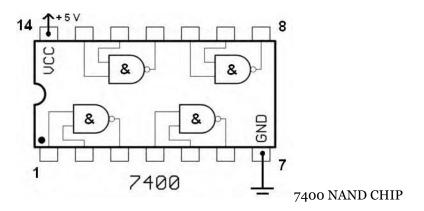
#### THEORY:

Digital logic devices are the circuits that electronically perform logic operations on binary variables. The binary information is represented by high and low voltage levels, which the device processes electronically. The devices that perform the simplest of the logic operations (such as AND, OR, NAND, etc.) are called gates. For example, an AND gate electronically computes the AND of the voltage encoded binary signals appearing at its inputs and presents the voltage encoded result at its output.

The digital logic circuits used in this laboratory are contained in integrated circuit (IC) packages, with generally 14 or 16 pins for electrical connections. Each IC is labeled (usually with a 74LSxx number) to identify the logic it performs. The logic diagrams and pin connections for these IC's are described in the TTL Data Book by Texas Instruments.

The transistor-transistor logic (TTL) IC's used in this laboratory require a 5.0 volt power supply for operation. TTL inputs require a voltage greater than 2 volts to represent a binary 1 and a voltage less than 0.8 volts to represent a binary 0.

Pin numbering is standard on IC's. Figure 1-1 illustrates the pin numbering for a 14-pin dual in-line package (DIP). With the IC oriented as shown, the numbering starts at the top left and proceeds counterclockwise around the chip:



## PROCEDURE:

- 1. Check the components for their working.
- 2. Insert the appropriate IC into the IC base.
- 3. Make connections as shown in the circuit diagram.
- 4. Provide the input data via the input switches and observe the output on output LEDs.

## **Logic Gates and their Properties**

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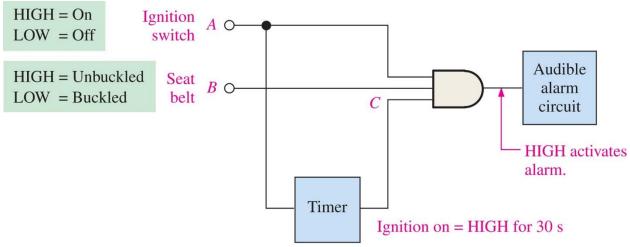
Gate	Description			1 Table	Logic Symbol	Pin Diagram
OR	The output is active high if any one of the input is in active high state, Mathematically, $Q = A + B$	0	<b>B</b> 0 1 0 1	Output 0 1 1	A OR	7-292 1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-
AND	The output is active high only if both the inputs are in active high state, Mathematically, Q = A.B	0	<b>B</b> 0 1 0 1	Output 0 0 0 1	A B AND AS	7408 1
NOT	In this gate the output is opposite to the input state, Mathematically, $Q = (A)$ '	<b>A</b> 0 1		Output 1 0	A NOT	7404 1 VOC 14 2 VOC 14 2 VOC 14 12 4 VOC 14 12 4 VOC 14 12 4 VOC 14 12 4 VOC 14 12 4 VOC 16 10 8 VOC 16 8 VOC 1
NOR	The output is active high only if both the inputs are in active low state, Mathematically, $Q = (A+B)$ '	A 0 0 1 1 1	0 1 0 1	Output 1 0 0 0	A B NOR	7402 14 2 4 4 5 7 6ND 8
NAND	The output is active high only if any one of the input is in active low state, Mathematically, Q = (A.B)'	A 0 0 1 1 1	<b>B</b> 0 1 0 1	Output 1 1 1 0	A B NAND	7400 14 2 4 11 12 4 10 8

- 1. Complete the table using the circuit symbol, Boolean function, and truth table using a Breadboard.
- a. Assemble one single NAND gate from a 7400 chip and verify its operation.
- b. Assemble one single NOR gate from a 7402 chip and verify its operation.

TYPE OF GATE	SYMBOLIC LOGIC	INPUTS		OUTPUT
		A	В	С
NAND IC 7400	$a - b$ $C=(\overline{AB})$	0 0 1 1	0 1 0 1	1 1 1 0
NOR IC 7402	$\bigcap_{B} \bigcap_{C=(\overline{A+B})}$	0 0 1 1	0 1 0 1	1 0 0 0

## 2. A seat belt Alarm System:

Given the following diagram (system)



a. Every time the ignition switch is turned on in the above circuit, the alarm comes on for thirty seconds, even when the seat is buckled. What is the most likely problem? What is the most probable cause of this malfunction?

*Answer:* The three-input AND gate most likely has malfunctioned causing the alarm to ring. A probable cause could be that the three-input AND gate could have been electrically shorted/burned due to external causes.

b. The seat belt alarm circuit has malfunctioned. You find that when the ignition switch is turned on and the seat belt is unbuckled the alarm comes on and will not go off. What is the most likely problem? How do you troubleshoot it?

Answer: The timer most likely has malfunctioned causing the alarm to ring continuously.

The proper way of diagnosing is trying to disconnect the timer then test to see if the alarm stays continuously on with the seat belt buckled.

#### ANSWER THE FOLLOWING QUESTIONS (Using the internet):

1. Why NAND & NOR gates are called universal gates?

*Answer:* NAND and NOR are called universal gates because all the other gates like AND, OR, NOT, XOR and XNOR can be derived from it.

2. Attain the EX – OR gates using minimum number of NAND gates.

Answer: It would take a minimum of 4 NAND gates to represent an XNOR gate.

3. Give the truth table for EX-NOR and attain using NAND gates?

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Answer: a b out
0 0 0
0 1 1
1 0 1
1 1 0
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4. What are the logic low and High levels of TTL IC's and CMOS IC's?

Answer: For TTL gates, the low-level noise margin is the difference between 0.8 volts and 0.5 volts (0.3 volts), while the high-level noise margin is the difference between 2.7 volts and 2 volts (0.7 volts). CMOS noise margins widen even further with higher operating voltages.

5. Compare TTL logic family with CMOS family?

Answer: A single logic gate in a CMOS chip can consist of as little as two FETs while a logic gate in a TTL chip can consist of a substantial number of parts as extra components like resistors are needed.

6. Which logic family is fastest and which has low power dissipation?

Answer: In Emitter Coupled Logic (ECL), the storage time is eliminated as the transistors are used in difference amplifier mode and are never driven into saturation. Is the fastest logic family and has the lowest propagation delay.