Lab No. 8:

Improved FSMD

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Note: *This lab is a bonus mark, and it has to be finished during the lab session.*

Objective:

- Improve a FMSD design .

Hardware:

- See previous lab.

To hand in:

- Commented Verilog source files - module and top module.
- Explain detailed modification in the header of each module.

Lab work:

- Again, for a second time, you must improve your lock design.

Improvement:

- After reset, the user must wait 4 seconds before she can start entering the secret code. Also, whenever the user enters a wrong code, she must wait the same 4 second delay.
- You must modify the existing delay counter. You don't create a new counter. The countdown for wait must be displayed on one digit (the same digit as the 9 second delay).

Test Bench:

Test bench is optional.

Test on the target:

Download the code on the target and test it. Final result to be approved.

[Verilog code for Lab 8]

- Refer to "PulseGen" module in "PulseGen.txt" attached to this report submission.
- Refer to "Down_counter" module in "Down_counter.txt" attached to this report submission.
- Refer to "Lock" module in "Lock.txt" attached to this report submission.
- Refer to "Lab8_TOP" module in "Lab8_TOP.txt" attached to this report submission.

[Verilog constraints file for Lab 8]

- Refer to "Lab8_constraints" file in "Lab8_constraints.txt" attached to this report submission.