Computational Logic Circuits (Online Lab 4)

Shift Registers

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OBJECTIVES

- To understand the function of shift registers.
- To understand how to design a shift register.
- To verify and simulate the function of a shift register.

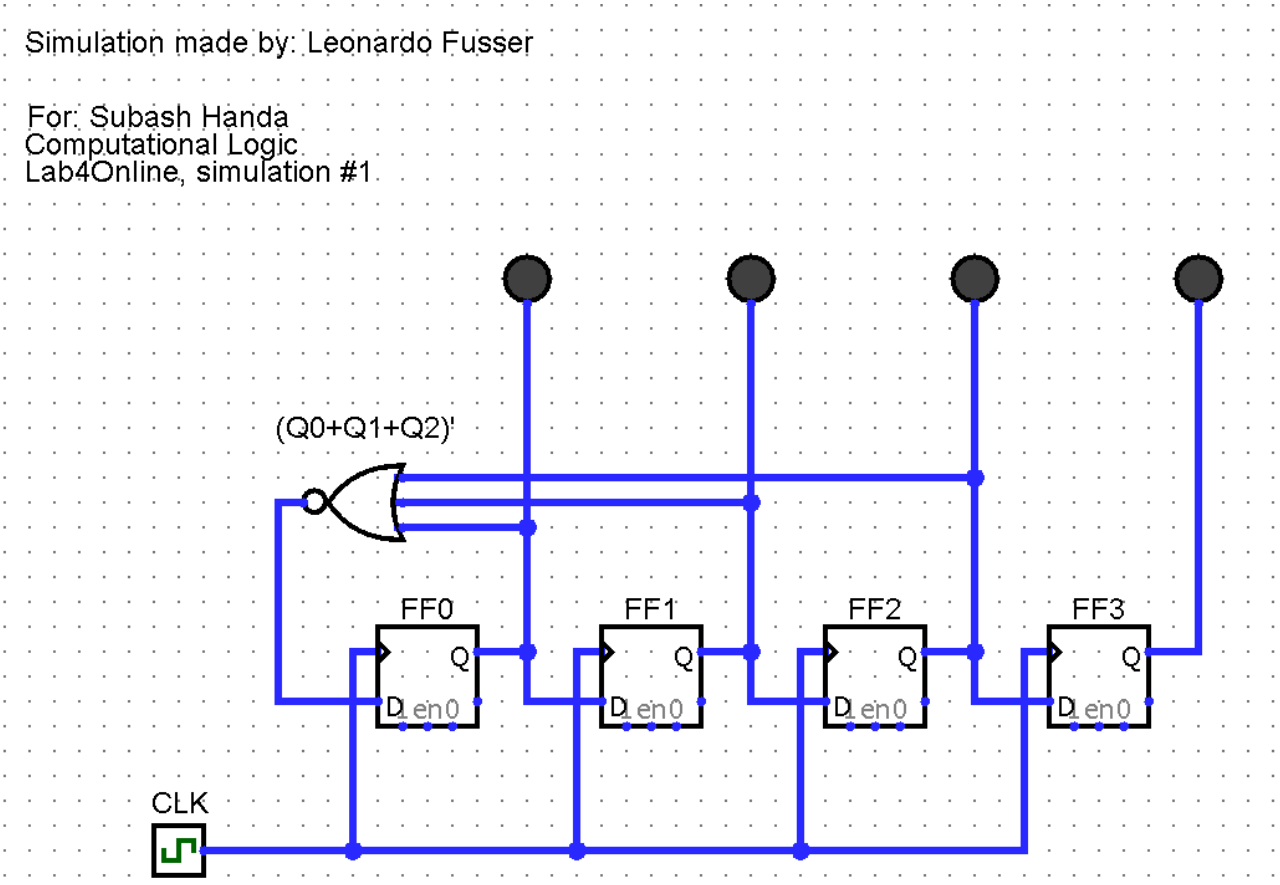
DESIGN

Experiment

- There was one simulation done in this lab. We were asked to create a shift register using D Flip-Flops. For better visualization of the concept of a shift register, a serial in / parallel out right shift register was used in this lab. The sequence was a shift to the right after each clock pulse (1 would shift one place to the right after each clock pulse). Prior research on shift registers was done and proper design and testing were done as well. The simulations were done in "Logisim". Below outlines the work done in the lab.

SIMULATIONS

Simulations from the Experiment



Serial In / Parallel Out shift register using D Flip-Flops (above)

Results

CLK	FF0(Q_0)	FF1(Q_1)	FF2(Q_2)	FF(Q_3)
Initial	*0*	*0*	*0*	*0*
1	***1***	*0*	*0*	*0*
2	*0*	***1***	*0*	*0*
3	*0*	*0*	***1***	*0*
4	*0*	*0*	*0*	***1***

***Note: look at the position of 1 after each clock pulse *(shifting)*.**

QUESTIONS

Questions from the experiment

➢ **What are shift registers?**

- Shift registers are a type of sequential logic circuit used primarily for the storage of digital data and movement of digital data. Shift registers also (typically) do not possess a characteristic internal sequence of sates (with exceptions). There are 4 types of shift registers. 1) Serial In/Serial Out, 2) Serial In/Parallel Out, 3) Parallel In/Serial Out and 4) Parallel In/Parallel Out shift registers are common types today.

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➢ **Applications of shift registers?**

- Time-delay device:

Time Delay

A serial in/serial out shift register can be used to provide a time delay from input to output that is a function of both the number of stages (n) in the register and the clock frequency.

When a data pulse is applied to the serial input as shown in Figure 8–26, it enters the first stage on the triggering edge of the clock pulse. It is then shifted from stage to stage on each successive clock pulse until it appears on the serial output n clock periods later. This time-delay operation is illustrated in Figure 8–26, in which an 8-bit serial in/serial out shift register is used with a clock frequency of 1 MHz to achieve a time delay (t_d) of 8 μs (8 $\times$ 1 μs). This time can be adjusted up or down by changing the clock frequency. The time delay can also be increased by cascading shift registers and decreased by taking the outputs from successively lower stages in the register if the outputs are available, as illustrated in Example 8–6.

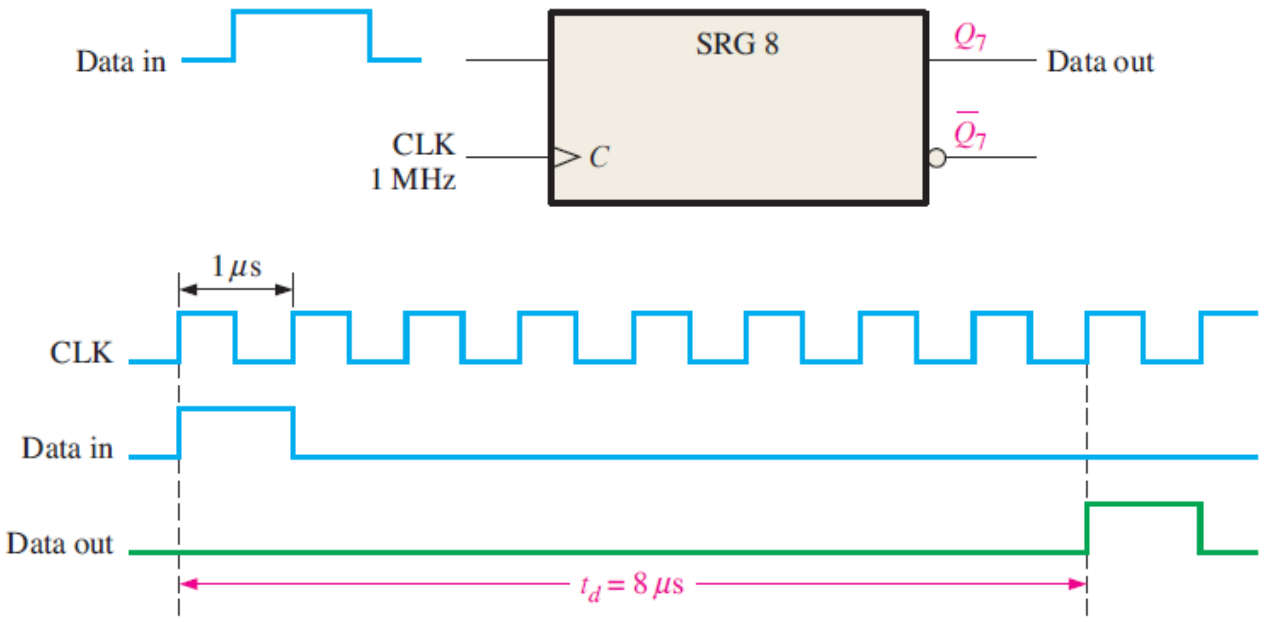

FIGURE 8–26 The shift register as a time-delay device.

Source: *Digital Fundamentals, Eleventh Edition, Thomas L. Floyd, 2015.*