

Course Outline

FACULTY: Faculty of Science and Technology PROGRAM(S): 243.A0 Computer Engineering Technology DEPARTMENT: 247 Computer Engineering Technology COURSE TITLE: PRODUCT DEVELOPMENT II COURSE NUMBER: 247-606-VA COURSE SECTION(S): 00001, 00002 PONDERATION: 2h - 4h - 3hLecture – Lab work – Homework 3h – 5h – 4.5h ⇒ Adjusted for a 10 week semester. NUMBER OF CREDITS: 3 credits 3 credits PREREQUISITE(S): 247-606-VA SEMESTER/YEAR: Semester 6, Winter 2022 TEACHER (THEORY): John F. N. Salik, Eng. Office: D-366 Tel: 514-744-7500 Ex. 7034 E-mail: salikj@vaniercollege.qc.ca Office Hours: Tuesday 10:30am to 11:30pm or by prior appointment. The AVAILABILITY: instructor will be in his office or in one of the CET laboratories. TEACHER (LAB): John F. N. Salik, Eng. Office: D-366 Tel: 514-744-7500 Ex. 7034 E-mail: salikj@vaniercollege.qc.ca AVAILABILITY: Office Hours: Same as above. Introduction



In this course, students will design and integrate and test a complete product that can be commerically deployed. Students will work independently to collect and interpret the product's specifications and form a continuous action plan that will require them to produce deliverables on time including the final, operational product. They will document, manage, and resolve problems in a logbook that should clearly demonstrate their organization as a professional. By the end of the course, students will demonstrate the results of their effort with a working product. During the semester, they will independently produce a multi-layer PCB from a specification. They will be responsible for component sourcing, creating libraries, and schematics. They will validate their board by prototyping it first. They are responsible for all embedded and host software (if connected to a computer). All wiring, harnesses and plugs must be professionally done in a manner that allows for the finished product to be maintainable by the customer that receives the product. The student will also be responsible for acquiring all external components so that they fit inside an enclosure.

Summary:

In the project portion of this course, students will autonomously produce a unique, consumer-grade product refining the principles first acquired in **Product Development I**. They will produce all necessary documents to support the product and produce prototypes in hardware and/or software as necessary. The major goal of the project is to produce a useful, cost-effective and production-ready printed circuit board that is fully planned and managed. Lectures will consist of various topics that center on embedded software engineering and data structures.

Statement of Competency

Competency 037N: To design printed circuits.

Competency 037V: To perform activities related to designing a computerized system.

Student Personal Resources Required

- Essential materials will be provided by the College.
- Project materials are purchased by the student for projects to a maximum value of \$250. Students will be required to provide proof of all purchases at the end of the semester.

Bibliography (required according to MEES)

- Class Notes & Slides 2020, John Salik
- To be provided through the online resource.



Week Date		Laboratory Exercise	Deliverables	
1	Jan. 17	Project Initiation: Discussion of project boundaries. Feasibility study (purchase plan, draft requirements, diagrams). Business Requirements Document.	Formal Memo: Feasibility study. Business Requirements Document	
2	Jan. 24	<u>Planning</u> : Functional Requirements Document. Scheduling and budgeting. Prototyping purchasing list (1).	Project Planning Document Prototyping Purchasing List (1) Functional Requirements Document	
3	Jan. 31	<u>Execution</u> : Exploratory prototyping. Progress report. Prototyping purchasing list (2).	Lab demonstration of progress. Prototyping Purchasing List (2) Formal Memo: Detailed progress report (technical)	
4	Feb. 7	<u>Execution</u> : Component selection, sourcing and ordering. Complete schematic entry.	Purchasing invoices. Complete schematics (with libraries).	
5	Feb. 14	Execution: Essential subsystem prototyping. Progress report. Revision of the Functional Requirements Document Preparation of project presentation.	Lab demonstration of progress. Formal Memo: Detailed progress report (technical) Revised Functional Requirements Document Project presentation.	
6	Feb. 21	Execution: Full prototype assembly. Schematic design review. PRESENTATION 1.	Revised schematics. Formal Memo: Progress report on technical issues and how they will be resolved.	
7	Feb. 28	Execution: Mechanical prototyping (measurements and enclosure fitting). Mechanical CAD. Component and parts ordering.	2D mechanical drawings: PCB geometry, the complete assembly and all other important mechanical parts.	
8	Mar. 7	Execution: Prototype functional testing. Complete device testing. PCB design.	PCB mock-up (transparent PCB, all layers). Formal Memo: Progress on mechanical and electronic aspects (technical).	
9	Mar. 14	Spring Break		
10	Mar. 21	<u>Execution</u> : PCB design and budget review. Component and PCB ordering.	Invoice collection and organization. Formal Memo: Progress report and budget.	
11	Mar. 28	Monitoring & Control: Project review: logistic, budgetary or scheduling problems/issues. Preparation of final project presentation.	Formal Memo: Progress report (non-technical).	
12	Apr. 4	Execution: PCB assembly and testing.	Lab demonstration of PCB function. Formal Memo: Progress report (non-technical).	
13	Apr. 11	Closure: Device assembly and testing.	Lab demonstration of device function. Final project presentation (COMPLETED).	
14	Apr. 18	Stage Week 1	No work scheduled.	
15	Apr. 25	Stage Week 2	No work scheduled.	
16	May 2	Stage Week 3	No work scheduled.	
17	May 9	PRESENTATION 2	Formal demonstration of project to the Department and General Audience. This will be a public demonstration.	



- *Note 1: This is a new course, dates and content may vary.
- *Note 2: Students are expected to submit work for grading every week to provide incremental feedback on progress.
- *Note 3: Documents submitted for grading is due <u>start</u> of theory class, 8:00am on Wednesdays.
- *Note 4: Laboratory sessions are scheduled from 8am to 1pm with a mandatory scheduled break from 10:30am to
- 11:00am. Students may leave the class at 12:50pm.

Lectures (see *Note 1, 2, 3 and 4 above)

Content is tentative and will vary to support the competencies directly with an emphasis on artificial intelligence. Deliverables from the laboratory sessions are due at the start of class (8am) and are considered late after 5 minutes. Only printed submissions are marked although an online submission as well. Dates are tentative. The instructor reserves the right to add or remove material as time permits (this is a new course).

Laboratory Sessions (see *Note 1, 2, 3 and 4)								
Week	Date	Theory Topic	Overview					
1	Jan. 19	Partitioning Algorithms	Introduction to Classifiers					
2	Jan. 26	Clustering Part 1	K-Means and K-Nearest Neighbors					
3	Feb. 2	Clustering Part 2	DBSCAN and Hierarchical Clustering					
4	Feb. 9	Tree-Based Methods	Decision Trees and Random Forests					
5	Feb. 16	Dimensional Analysis	PCA, SVD, and LDA					
6	Feb. 23	Midterm						
7	Mar. 2	Metaheuristic Optimization	Cost Function Optimization					
8	Mar. 7	Probabilistic Search	Simulated Annealing					
9	Mar. 14	Sprint Break						
10	Mar. 21	Metaheuristic Optimization Part 3	Genetic Algorithms					
11	Mar. 28	Multi-Agent Optimization Part 4	Particle Swarm Optimization					
12	Apr. 4 Review		Cumulative Review					
13	Apr. 11	Final Exam						
14	Apr. 18	Stage Week 1	No work scheduled.					
15	Apr. 25	Stage Week 2	No work scheduled.					
16	May 2	Stage Week 3	No work scheduled.					
17	Мау 9	Presentation						



Course Struc	cture					
THEORY:	2 hours/week:		course compression to 10 weeks (3-week stage), this is led as 2.5 hours/week .			
			ts must be present, taking their own notes and actively pating in classroom.			
sc to de			Due to course compression to 10 weeks (3-week stage), this is scheduled as 5 hours/week . Students are expected to devote this time to ensuring their project is on track for completion and that all deliverables are in on time. Their presence is required for the entire laboratory period with the exception of scheduled breaks.			
PERSONAL EFFORT:						
ATTENDANCE						
THEORY:	Consistent attendance is suggested to fully benefit from the course. In the event of absence, students are responsible for obtaining and assimilating all material covered. All laboratory deliverables are due at the start of the following theory class.					
LABORATORY:	Work assigned in the laboratory must be completed during the time allotted an adequate preparation by students. Unprepared students be able to practically demonstrate their preparedness will receive a grade penalty proportionate to t they are unable to do in the current laboratory activity. No students should be or leaving the classroom without permission and no work outside the context o session is allowed.					
TESTS:	Absence will result in failure of the missed test (mark of 0). Students with a just cause for absence are encouraged to seek alternative arrangements with the instructor – beforehand if possible.					
EVALUATION						
	Project 75%	10% 10% 50% 5%	Log Book (10 entries, 2 pages each) Laboratory Performance (10 Labs) Project (over 10 labs cumulative) Presentation (May 9)			
		Note:	To pass the course, a passing grade is needed <u>on all of the</u> <u>following</u> : Log Book, Project Presentation otherwise a maximun grade of 60% will apply.			
	Exams 25%	10% 15%	Midterm Exam (Feb. 23 th) Final Exam (April 11, Cumulative)			



Total: 100%



Learning Integration Assesment (LIA)

Each course includes a Learning Integration Assessment (LIA) that attests to students' achievement of the courselevel learning outcome that is the main knowledge, skills, and attitudes to be developed. The LIA for this course is the following:

Students will be evaluated on how they develop a complete, commercial grade product from a specification. They will be assessed on their product development and project management techniques. Using a professional log book, they must document their thoughts, measurements, and activities with the goal of producing actionable workplans.

This course forms a part of the Program Comprehensive Assessment (Epreuves Synthèse de Programme). To graduate from the CET program, all students must attempt and succeed the PCA. To do this, they must demonstrate the knowledge they acquired over the entirety of the program in the production of a complex project. Only students that demontrate they fit the formal CET exit profile will be issued a passing grade for the PCA. Note that a report and presentation form part of the PCA as required by Vanier College's Policy on Comprehensive Assessments. The remaining parts will be covered in other courses at the Department's discretion.

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EVALUATION CRITERIA FOR THE LEARNING INTEGRATION ASSESSMENT

The project will consist of developing a product that includes the following comprehensive aspects:

- Product planning and designing methods
- Developing detailed schematic diagrams from manufactures data sheets of a complete system.
- Developing a PCB for a product
- Troubleshooting a product
- Prototyping a product
- Produce all documentation that pertains to the product development.
- Programming microprocessors and modifying microprocessor programs
- Integrate, diagnose, optimize, and write procedures on a computer engineering system
- Schematics interpretation

STUDENT PROFICIENCY IN THE LANGUAGE OF INSTRUCTION (SPLI)



Student proficiency in the language of instruction is the ability to write, read, speak, and listen in order to communicate effectively at the college level. SPLI may also require discipline-specific vocabulary, documentation, and communication skills; assessment of language skills must account for a minimum of 10% of any take-home written assignment or oral presentation in which English is the language of expression.

In this course, the SPLI is based on:

- 1. The log book.
- 2. Presentation.

The following general rules apply:



- If log books do not have at least one 200-word entry per laboratory session or if a prototype does not have at least 80% functionality or the final submitted device does not have 100% function or complete documentation is not submitted complete and in the manner requested or the student has demonstrably exceeded their budget, then student may not pass the course (a maximum final grade of 55%).
- At least one week's notice will be given for test dates or changes in test dates.
- Quizzes may be given without prior notice there are no make-ups for quizzes.
 - Students are expected to attend all of their scheduled theory classes. In-class assignments will only be accepted in the class in which they are assigned.
 - Students are expected to take notes and participate in any discussion or activities.
 - No unannounced or unexpected departures are allowed from the scheduled lecture period. In this case, a grade penalty will apply.
 - Work assigned in the laboratory session is due within the first 5 minutes of the theory class. Work handed in after this is considered late.
- Absence from any laboratory sessions without valid reason (official note required) may result in failure of the assignments given there. Any anticipated absences must be discussed with the instructor.
 - Absence from any laboratory sessions without valid reason (official note required) may result in failure of the assignments given there. Any anticipated absences must be arranged with the instructor including submission of assigned work. In-lab assignments will only be accepted in the lab in which they are assigned.
 - No unannounced or unexpected departures are allowed from the scheduled laboratory period. In this
 case, a grade penalty will apply. Complete attendance to laboratory sessions a required (no
 unannounced or unexpected departures for any reason).
- Students are expected to conduct themselves in a professional manner at all times. This includes but is not limited to:
 - Arriving to class (theory and laboratory) on time and prepared to do the required work;
 - Conducting themselves in an appropriate manner at all times (including being respectful to the teacher, classmates, and any guests);
 - Using professional language (no cursing and/or swearing and using appropriate vocabulary);
 - Arriving to class/lab with all necessary supplies (logbook, notebook, textbook, manual, paper, writing implements, calculator, etc.);
 - Turning off all personal communication/music/video electronics (removing headphones, earphones, ear buds etc.); and
 - Being prepared for laboratory sessions and theory class including having all assigned work completed.
- Reports must be typed and computer generated according to the guidelines provided by the teacher.
- When requested, Lab preparations and Lab Results/logbooks are to be handed in during the lab session.
 Late Lab Preparations/Lab Results may not be accepted, and a zero mark will be recorded.
- Any assigned work submitted beyond 1 week late may not be accepted, and a zero mark may be recorded.
 Assigned work up to and including one week late may be reduced by up to 25% of the maximum mark.
- Students who are consistently late for class (lab and/or theory) may be refused entry.
- All grades are reported on a numeric scale from 0% to 100%. The following categories briefly describe the relative value of these grades:

range mean Description

Rev. 1.0 20-JAN-2020 9 John F. N. Salik, Eng.



90 - 100	95	Excellent, mastery of the objectives
80 - 89	85	Very Good mastery of the objectives
65 - 79	72	Good, mastery of objectives
60 - 64	62	Fair mastery of objectives
0 - 59	n/a	Poor mastery of objectives

Academic and other Resources

If at any point in the semester, you are concerned about the course or you realise that you are having academic difficulties; your first resource should be to talk to me, your teacher. Academic difficulties include problems with the understanding of the theory, to the development of the practical skills required by the course. The earlier you look for help, the greater your chances of succeeding in the course. If I don't feel I can provide you with the help you need then I may recommend one of the College resources below.

For other problems or difficulties, you may encounter while at Vanier there are a number of Services available to help you within the college. They are there for you to use. These include:

Student Services (C203): Some areas where they provide services and/or information are:

Services for students with disabilities Counselling (personal and other problems)
Student Advocate Financial Aid (including aid and scholarships)

Health Services (Nurse on staff)

Student Employment

Academic and Behaviour Policies Lockers
Housing Volunteering

Student Services is a great resource for questions about college life and any problems you encounter while at Vanier. If they do not have the answer, they can direct you to the right place to find it.

<u>Tutoring and Academic Success Center - TASC (F-300)</u>: Student-orientated centre dedicated to promoting and aiding students' development and success in academics and in society.

Admissions and placement tests S.T.A.R. Program

English Exit Exam English conversation and pronunciation clubs

English Peer Tutoring Scholarship information
Vanier Native Program Diversity support

TASC is the main college resource for students with learning difficulties and for students with weak English language skills.

<u>Science, Technology, Engineering and Mathematics - STEM (D-301)</u>: This Centre aims to promote student success in mathematics and science. The large interactive study space includes a hackerspace for hands-on applied projects such as robotics, and a study hub for collaborative group work. Teacher help, computers, and a large collection of math and science textbooks are equally available. We offer a number of activities, services and resources including:

Free drop-in peer tutoring Drop-in help from teachers
Free private tutoring Teacher-led review sessions

Computer access Laptop borrowing



Mediation and Grades Review

There are two committees available to the student for resolution of academic complaints.

- 1. The *Grades Review Committee* to review complaints concerning the grading of students' work.
- 2. The *Faculty Mediation Committee* to review academic complaints other than those dealing with student grades see *Student Academic Complaints* below.

General College Academic Policies

It is the student's responsibility to be familiar with and adhere to all Vanier College Policies. A summary of the course-level policies that apply in this and all other Vanier courses can be found under "Course-Level Policies" in **Important Vanier Links** on **Omnivox**, or by following this link: http://www.vaniercollege.qc.ca/psi/course-level-policies/. Complete policies can be found on the Vanier College website, under Policies.