



MICROCHIP

Basic 32-Bit MCU Design and Troubleshooting Checklist

PIC32MZ, PIC32MX, PIC32MK, PIC32C, and SAM Devices



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1. Frequently Asked Questions (FAQs)

- Problem 1: Intermittent start-up issues during power up or some devices will not start-up at all.
- Problem 2: Intermittent start-up, wake from low power modes or analog repeatability issues.
- Problem 3: Intermittent start-up and/or lock up issues on power-up.
- Problem 4: Intermittent MCU POR, BOR, BOD reset issues during start-up resulting in exception errors or lock ups.
- Problem 5: Some PIC32MZxxEFxx devices are intermittently not starting up when using primary oscillator with crystal.
- Problem 6: A PIC32MZxxEFxx is running at 200Mhz and there are lockups or exceptions errors on some devices.
- Problem 7: An external clock is being used with the MCU in EC mode, a clock is being input to the MCU, but nothing is happening.
- Problem 8: Using a crystal with automatic gain control enabled, POSCAGC=1, and getting a clock fail detect.
- Problem 9: Using auto gain control but seeing intermittent start-up issues on some boards and/or over temperature.
- Problem 10: The MCU operating frequency is not as expected or no MCU code is executing.
- Problem 11: Trying to clock switch from FRC to FRC w/PLL, but the system clock is still only 8Mhz and/or the OSCCON.OSWEN bit indicates the clock switch never completed.
- Problem 12: Sometimes a reset happens on a wake from sleep, or during a clock switch.
- Problem 13: A lock-up sometimes occurs during a power anomaly or when power cycling the application.
- Problem 14: Sometimes after hours, a lock-up occurs.
- Problem 15: The device does not function. It is continuously stuck in a hard fault or a reset.
- Problem 16: The PC does not recognize ICD4 and/or PICKIT 4.
- Problem 17: In debug mode why are some PIC32MX/ PIC32MZ/ PIC32MK registers values not showing as expected?
- Problem 18: Unable to connect with ICD4 or Realice to target.
- Problem 19: Programming works, but not the debug.
- Problem 20: What needs to be done with the exposed pad on the MCU package for the PCB design?
- Problem 21: Some of I/O pins and/or alternate function pins are not working at all even though they are configured correctly.
- Problem 22: MPLAB does not connect to the PIC32 target device.
- Problem 23: Do bypass caps need to be used on the VBAT input pin?
- Problem 24: The external battery voltage cannot be measured correctly using the ADC.
- Problem 25: There is frequent to intermittent data corruption between the MCU and target IC.
- Problem 26: There is intermittent data corruption on communication links between remote PCB stations or equipment.
- Problem 27: Clock and data are present, but the target SPI device it is not responding.
- Problem 28: Why is the SPI data always shifted by one bit?
- Problem 29: Why is the SPI /SQI data corrupted?
- Problem 30: The SD Card will not write or erase, only read.
- Problem 31: The SD Card cannot be accessed.
- Problem 32: Why is the UART data corrupted?
- Problem 33: Why is the first UART byte always wrong after a power-up or wake from sleep?

Frequently Asked Questions (FAQs)

- Problem 34: Why does a USB data transfer take longer than expected?
- Problem 35: Why will the USB DEVICE not enumerate?
- Problem 36: USB connection has been lost.
- Problem 37: Why is the CAN sending message errors?
- Problem 38: Why will the CAN not connect?
- Problem 39: Why is the SAR ADC result 0v with input voltages up to 30mv or more?
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Equation 1: Crystal MFG $C_{LOAD} = \{([C_{IN} + C1] * [C_{OUT} + C2]) / [C_{IN} + C1 + C2 + C_{OUT}] \} + \text{oscillator PCB stray capacitance.}$

Equation 2: Simplified Crystal C_{LOAD} formula: $C1 = C2 = ((2 * \text{MFG } C_{LOAD} \text{ spec}) - C_{IN} - (2 * \text{PCB capacitance}))$.

Equation 3: PCB signal series termination resistor(s) value = $\{[(VDD-VOH(\min)) / IOH(\max)] - \text{Trace Impedance}\}$.

5. Introduction

The 32-bit MCU Design Checklist is a value-added service provided by Microchip to assist customers in the development process. This document provides comprehensive guidelines for good design practices, common troubleshooting issues and their cause, and possible corrections. It also covers the following:

- Typical design-related issues and troubleshooting
- Best design practices
- Reference design examples
- ESD, EMI, and EFT protection considerations
- Typical peripheral usage issues (ADC, SPI, Ethernet, CAN FD, LIN, SQI, SDHC, UART, USB, and so on)
- PCB layout guidelines

For additional help, contact Microchip 32-bit design check service to provide assistance. A qualified engineering team with expertise in 32-bit microcontrollers (PIC32 and SAM) will review and provide guidance on the design to expedite the design cycle and help release the products to market faster.

5.1 User Issue Submission Instructions

Follow these steps to submit issues:

1. Identify the key areas of concern and challenges in the application.
2. Use the [Design and Trouble Shooting Menu](#) to reference applicable sections of the interest.
3. Complete the information review noted in the “completed” column in the [Design and Trouble Shooting Menu](#) in Chapter 1, prior to submitting an issue.

5.2 Microchip Client Support Services

www.microchip.com/clientsupport

5.3 Microchip Technical Support Services

microchipsupport.force.com/s/

6. Basic 32-Bit MCU Design and Troubleshooting Menu Checklist

Table 6-1. 32-Bit MCU Troubleshooting Checklist Menu

Check List Item	Issue Category	Issue Type	Completed
1	Functional Anomalies	<ul style="list-style-type: none"> Before trouble shooting review the product errata sheet to ensure compliance with all known workarounds and to avoid using non-supported features or modes. The errata listing can be found by going to the target MCU product page and selecting the Documentation TAB. 	
2	CPU Start-up problems	<ul style="list-style-type: none"> VDD Ramp Rate Power Bypassing Power Sequencing I/O pin Current Injection Crystal oscillator(s) Clock Switching 	
3	Unexpected Resets	<ul style="list-style-type: none"> POR / BOR NMI (Non Maskable Interrupt - Exception errors) ESD / EMI / EFT Events 	
4	Debug Issues	<ul style="list-style-type: none"> ICD4 / REAL_ICE ICSP (PGDx / PGCx) JTAG / SWD 	
5	PCB MCU Connections	<ul style="list-style-type: none"> Exposed PAD PIC32MZ/ PIC32MK VUSB3V3 MCLR# / Reset# VBAT & Battery Monitoring 	
6	Serial Data Corruption / Errors	<ul style="list-style-type: none"> Impedance Matching Ground Loops SPI / SQI SD (SDHC) UART USB CAN FD 	
7	ADC	<ul style="list-style-type: none"> Typical SAM SAR ADC Total Unadjusted Error Sources ADC NOISE VREF ACCURACY Circuit IR drop Offsets 	
8	I ² S	<ul style="list-style-type: none"> I²S and PCB pushbutton protection and design example 	
9	I ² C	<ul style="list-style-type: none"> I²C protection and design example 	
10	Inlet Power Protection	<ul style="list-style-type: none"> EMI/EFT protection design example 	
11	Ethernet	<ul style="list-style-type: none"> Typical Ethernet Issues Special Ethernet 10/100 Base-T Design Guidelines Unused Ethernet Cable Pairs Considerations Ethernet RJ45 Connector Considerations Ethernet Magnetics Considerations Ethernet design example KEY ETHERNET PROTECTION DESIGN POINTS 	
12	PCB Layout Guidelines	<ul style="list-style-type: none"> Comprehensive PCB Layout Guidelines & Recommendations 	

Note:

STEP 1: Identify the key areas of concern and/or challenges in the application.

STEP 2: Use this checklist to reference applicable sections of interest.

STEP 3: Complete the information review noted in the "completed" column of this table, prior to submitting an issue.

7. MCU Start-up Problems

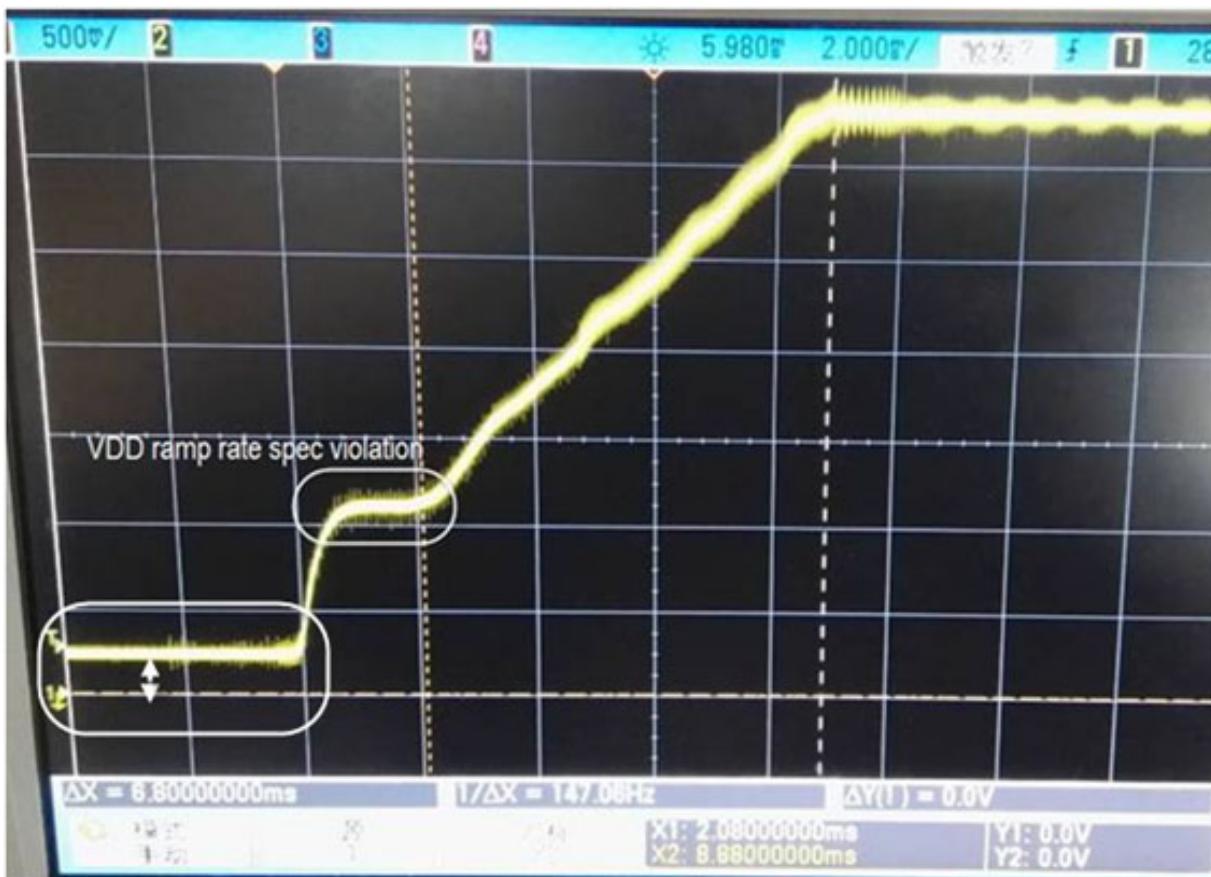
7.1 VDD Ramp Rate

Problem: 1: Intermittent start-up issues during power up or some devices will not start-up at all.

- Failing to meet the data sheet VDD ramp rate can cause lock-up issues or improper POR and BOR (i.e., BOD). VDD ramp rates are specified in volts per unit time, meaning that throughout the entire power-up process from 0V to nominal VDD, the VDD voltage must comply with the ramp rate specification.

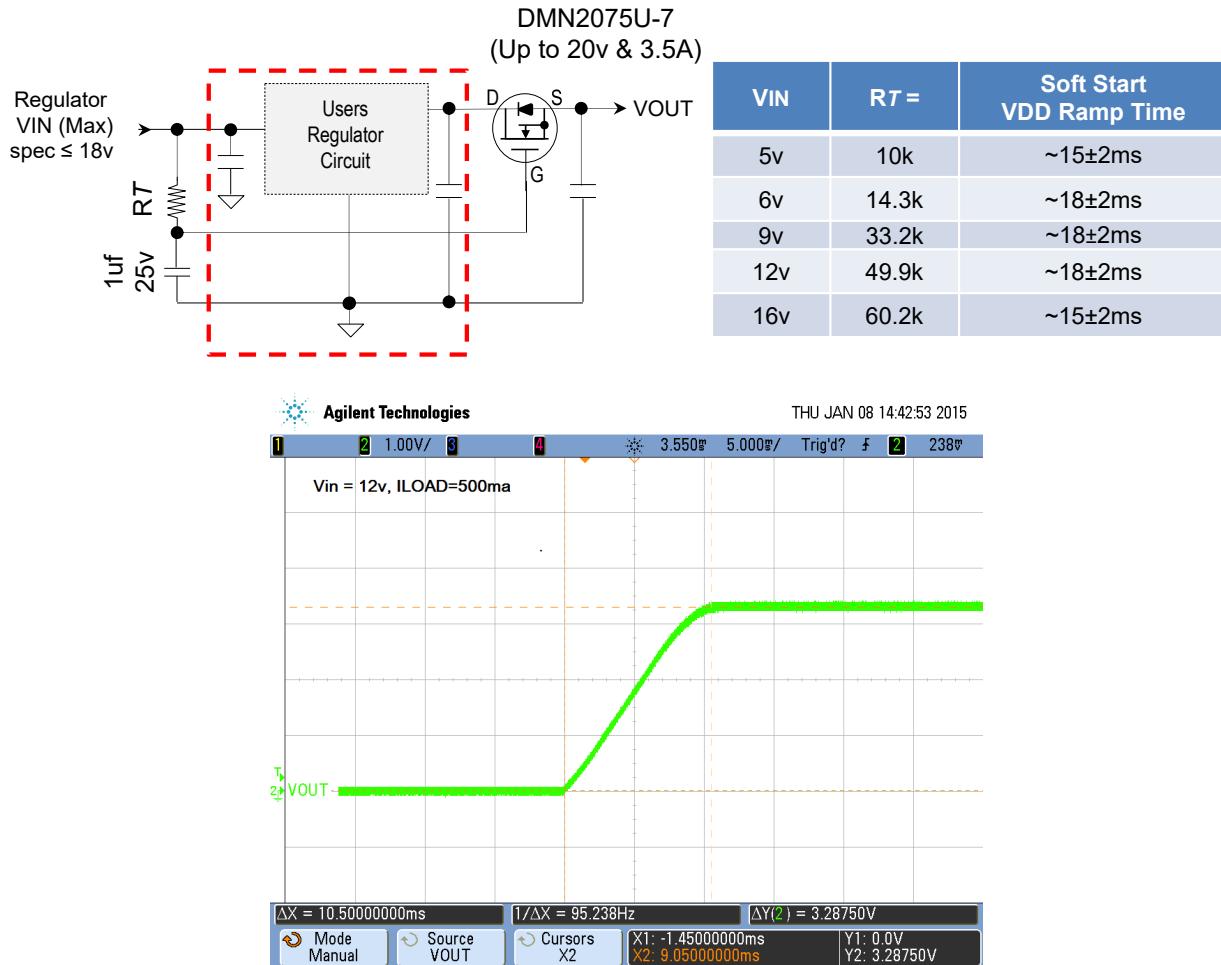
Note: The following VDD waveform contains (2) VDD ramp rate spec violations and can result in start-up issues. It is not correct to assume that as long as the VDD reaches its nominal threshold within the ramp time that they comply with the specification. This is an incorrect assumption and can be seen in the following VDD ramp rate figure below. During two periods of time where the VDD plateaus, the VDD ramp rate is essentially 0v/ms and therefore does not meet the ramp rate specification. This can cause issues because internal circuits have thresholds that when triggered start various time delays that assert either internal reset and/or "Not Ready" signals to the internal logic for a limited period of time. Some trigger logic is sensitive to rise times and therefore the noise riding on the VDD can also cause the trigger logic output to chatter. This chatter that gates the enable/disable signals and resets the logic and state machines, can cause logic metastability issues. The VDD does not start from 0V, and for some products may exceed the minimum VPOR specification to guarantee a proper Power-on-Reset (POR). Therefore all MCUs have VDD ramp rate specifications, sometimes including even ramp down rates to cover partial transitory power loss due to power grid fluctuations.

Figure 7-1. VDD Ramp Rate Violation Example



- A simple VDD soft start circuit can be applied to any existing application regulator design to ensure a smooth linear power-up. The ramp rate can be controlled by changing the resistor value RT.
- In LDO, the regulator bypass capacitor before and after the FET must be the same. The user must ensure that the bypass capacitor between the regulator and FET meets the regulator's minimum capacitive load as defined in the related data sheet.
- In BUCK regulator the feedback and inductor circuitry must be located on the regulator side between the regulator and FET. The capacitor before and after the FET must be the same and meet the regulator's recommended minimum capacitive load requirement specification.
- At a slightly higher cost, use a regulator with an externally programmable soft start capacitor pin

Figure 7-2. VDD Soft Start Circuit to Control VDD Ramp Rate



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7.2 Power Bypassing

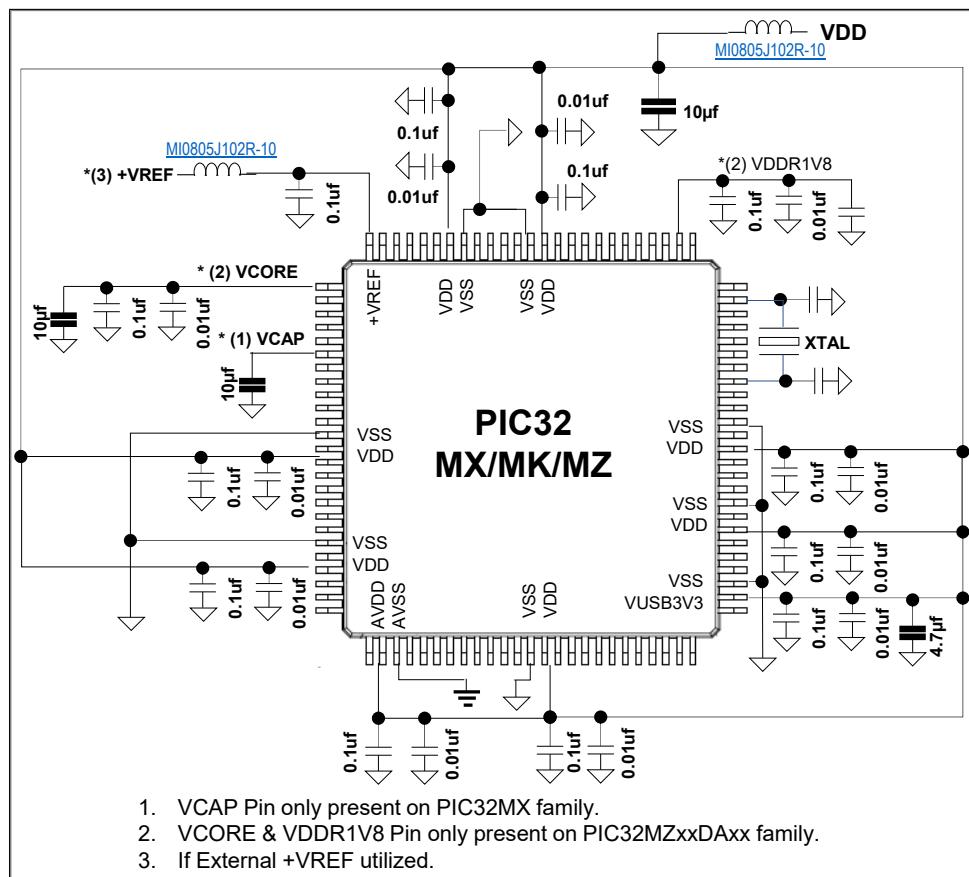
Problem 2: Intermittent start-up, wake from low-power modes or analog repeatability issues.

Note: Improper bypassing can affect the MCU during peak current demand periods during start-up, exit from low-power modes to Active mode, and clock switching between low-frequency operation to a higher clock operating frequency. It can also have an effect on timing jitter and pronounced analog peripheral performance impacts.

- All capacitors ceramic w/ESR ≤ 1 ohm ideally.
- All caps located on same side of the PCB as the MCU, except with packages, such as BGA where interior package pins are not accessible.

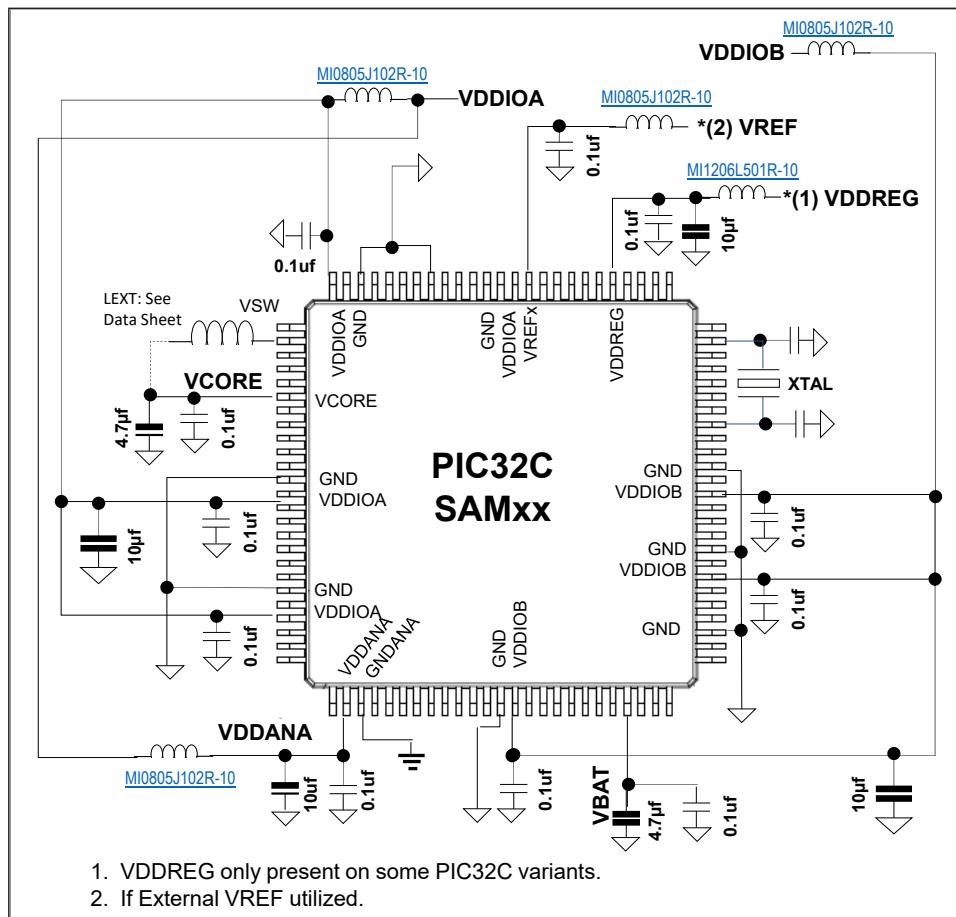
- High-frequency bypass caps located as close to the device power pins as possible.
 - BULK caps located close to the device, but in the case of multiple power pin groups that share the same PCB power bus, distributed evenly around device perimeter in close proximity to target power pin pair groups. For example, in some SAM families, VDDIOA and VDDIOB, call for separate 10 μ F caps, but most designs are connected together to the same PCB power bus. Do not connect both BULK caps side by side, instead distribute and center near the individual VDDIOA and VDDIOB groups.
 - All component leads to any power plane or ground plane must be as short as possible. The best solutions are plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections must be less than 5-10 mils in length. Trace connections must be as wide as possible to lower inductance. This will include any power ferrite beads feeding power planes, fuses feeding power planes, and so on.

Figure 7-3. PIC32MX/PIC32MZ/PIC32MK Recommended Minimum CPU Power Bypassing



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Figure 7-4. SAM/PIC32C Recommended Minimum CPU Power Bypassing

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7.3 Power Sequencing

Problem 3: The MCU is experiencing intermittent start-up and/or lock up issues on power-up.

- There are strict limits on voltage variations between different supplies on an MCU during power-up. In the PIC32MX/ PIC32MZ/PIC32MK, the VDD and AVDD must be no more than 0.3V apart during power-up. In the SAM/PIC32C it is VDDIO, VREG, and VDDANA. If using different regulators for different MCU supplies, it is critical that the designer consider how to manage this. This becomes even more critical in designs that use cascaded regulator designs (i.e., 5V > 3.3V > 1.8V regulators). This can create power sequencing issues, as well as voltage ramp differential synchronization specification violations.
- In the case of the PIC32MX, one result of the VDD and AVDD not tracking can be that the nominal VCORE of 1.8V will saturate at the nominal VDD voltage level. For short periods of time this may not harm the device, but will eventually induce reliability issues.
- To avoid unexpected current injection through the MCU, internal I/O high side protection diodes that can lead to MCU POR and start-up issues, ensure that signals originating from separately powered circuits be powered on after the MCU has been powered first. Failure to do so can cause an external logic high signal to power the MCU. If that is not possible consider using signal logic isolators, such as opto, capacitive, or inductive coupling components, see figures 7-1, 7-5B, and 7-6).

Note: Even the same regulator part number will ramp up at different rates depending on the load and bulk capacitance of the power bus.

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7.4

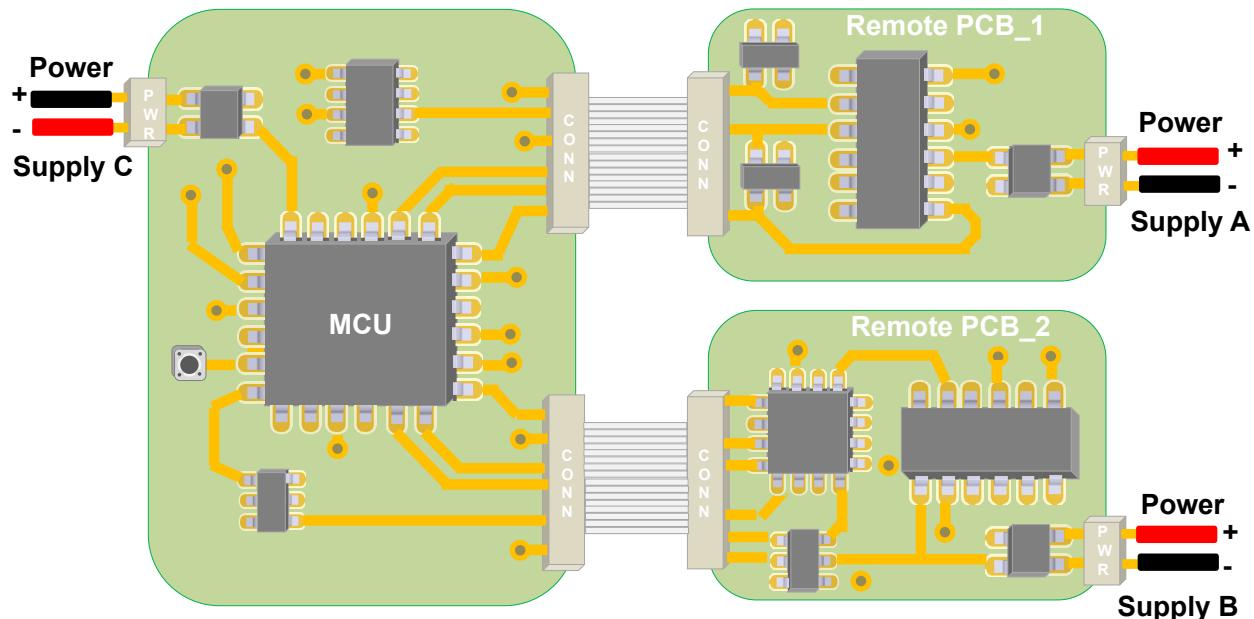
I/O Pin Current Injection from Remote Circuits

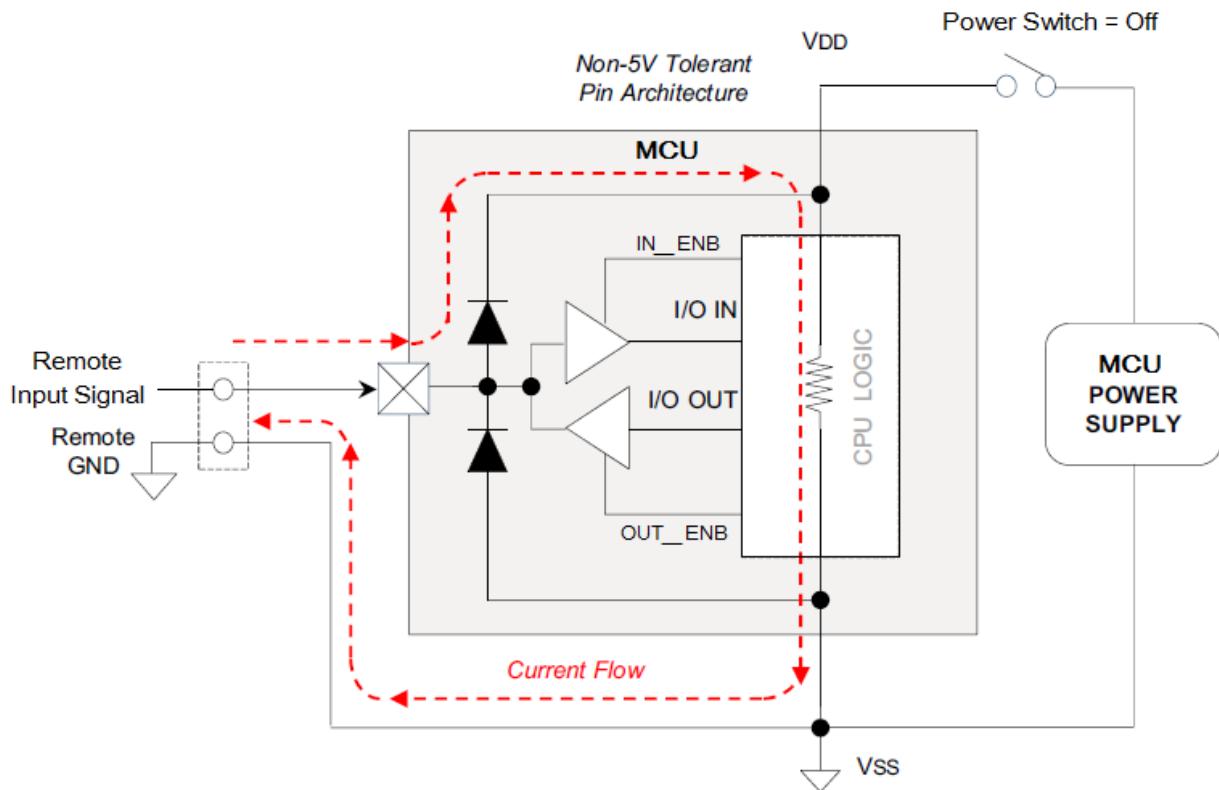
Problem 4: Intermittent MCU POR, BOR, BOD reset issues occur during start-up, resulting in exception errors or lock ups.

In interconnected designs, (i.e., cable connected PCB's as depicted in the following figure to the left side of the image), where remote interface circuits have independent power supply sources, injection current is a constant concern that can cause intermittent start up related issues due to POR, BOR, and BOD anomalies because the MCU can be powered through the I/O pins internal high side pin protection diodes (i.e., image on the right) rather than the VDD when MCU power is switched off from the remote still active circuits. In those cases, the VDD never actually goes to a voltage low enough to enable the MCU internal Power-on-Reset circuits properly. This can usually be detected if that is the case by taking a scope plot during the power up and power off period and inspect for any VDD anomalies where the VDD does not start from 0v volts as expected when it is turned off or the VDD appears to power up to between 0.6v to 1.2v, plateaus for a brief time, then continues upward to its expected nominal value, similar to the [VDD Ramp Rate Violation example](#). Designs like these are very susceptible to the following:

- Power sequencing in the interconnected PCB network
- [Ground loops](#) which are covered later

Figure 7-5. I/O Pin Current Injection





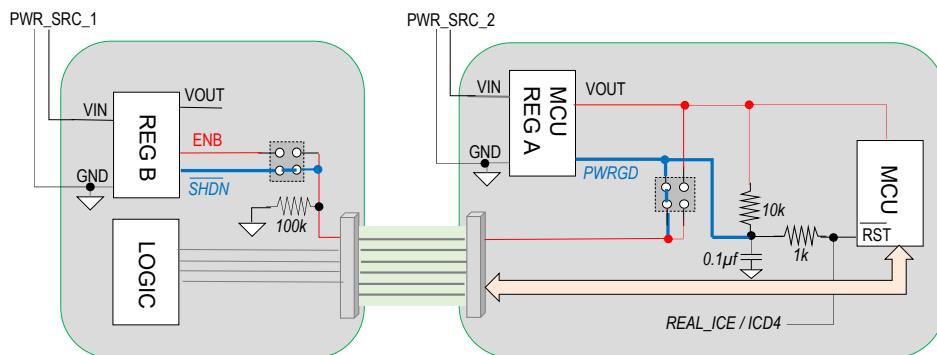
OPTIONS:

- The easiest design solution to circumvent unwanted injection current with remotely powered interconnected PCB's is depicted in the following figure. A lot of regulators, like MCP1727, MIC5528, MIC29151/301/501/751, have either an ENB pin, a SHUTDOWN pin, or a POWER GOOD function pin. The solution depicted below ensures that the MCU is always powered first before the remote PCBs are allowed to be powered on, hence the remote PCBs cannot power the MCU by injection current through the MCU I/O internal high side input protection diode. This also acts as a power sequencer. It is important that the MCU is always powered first. Whether the MCU uses a regulator PWRGD or even an MCU I/O pin, it is always recommended that the user use a control signal from the MCU PCB to make the other PCBs a power subject to the MCU PCB.

Method 1: A POWER GOOD on most regulators is an open collector output normally low until the MCU power has reached 90% of nominal value. The output is Tri-stated and the 10k pull-up forces it to a logic high enabling the remote PCB(s) regulator power.

Note: Using an MCU PCB regulator with POWER GOOD can also be used as an MCU reset supervisor when connected to the MCU reset pin in the configuration shown in the following figure.

Method 2: Same concept and net result of Method 1, except using the MCU PCB VOUT as remote PCB regulator ENABLE signal.

Figure 7-6. Injection Current Design Solution Option

- For relatively low-speed signals (i.e., typically $\leq 2.5\text{Mhz}$), a series resistor at the MCU input pins is in line with the remote signals to limit the injection current to $\sim 1.0 \text{ mA/pin}$ will usually suffice. The sum of all injection currents must not exceed $\sim 15 \text{ mA}$ total.

As a rule of thumb:

$R_{SERIES(max)} = ((VDD * 0.75) / 1 \text{ mA})$. Where, then the input signal Frequency(max) $\leq 1 / (1.95E-10 * R_{SERIES(max)})$. Limiting the injection current to a sufficiently low value will insure it will not be able to power the MCU, and impact the internal power on reset logic.

- Another option is to electrically isolate the interconnected signals using components similar to those listed in the following table:

Table 7-1. Signal Isolation Components

Signal Isolation Components	Inductive Coupling	Capacitive Coupling	Opto Coupling	Analog Signal Coupling
ADuM7241 / 40 ARZ (1 Mbps)	X			
ADuM7241 / 40 CRZ (25 Mbps)	X			
ISO721		X		
LTV-829S (2 Channel)			X	
LTV-849S (4 Channel)			X	
FSA266 / NC7WB66				X

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7.5 Crystal Oscillators

Note: In all MCUs, the crystal Automatic Gain Control (AGC), logic performs the AGC function only once at start-up. They do not continuously monitor and adjust crystal gain over temperature or voltage changes.

7.5.1 PIC32MZxxEFxx

Problem 5: Using a primary oscillator with a crystal, but some PIC32MZxxEFxx devices are intermittently not starting up.

Problem 6: Running a PIC32MZxxEFxx at 200Mhz and some devices are experiencing lockups or exception errors.

This MCU family has documented crystal errata that defines both required crystal circuit configurations, hardware and software, as well as supported crystal frequencies in addition to silicon revision B2 errata concerning restricted operating frequency versus Flash WS (i.e., wait states as defined in PRECON.PFMWS).

⚠ CAUTION

The PIC32MZxxEFxx silicon revision B2 currently supports only up to 184 MHz operation with 2 wait states. Operating frequencies in excess of 184 MHz requires 3 WS. With program memory cache enabled; however, this will affect MCU bandwidth <1.5%.

7.5.2 PIC32MK/PIC32MZxxDAxx/PIC32C

Problem 7: Using an external clock with the MCU in external clock (EC) mode, the clock is an input to the MCU, but nothing is happening.

Problem 8: Using a crystal with automatic gain control enabled, POSCAGC = 1, and getting a clock fail detect.

These device families and some PIC32C variants of MCUs (consult data sheet for information) have automatic gain control features defined by configuration words 'enabled by default' if not explicitly defined by the user which is often overlooked. When the automatic gain control is enabled, the manual coarse and fine crystal gain settings are ignored. When the POSCAGC bit is enabled and POSC HS mode is selected, in the appropriate configuration word, the Primary Oscillator will automatically do a linear step search starting from the lowest crystal oscillator circuit gain to the highest, to find the lowest power/gain setting to guarantee oscillation with the user's crystal. The delay between each AGC gain search step is defined by POSCAGCDLY.

⚠ CAUTION

If External Clock (EC) mode and AGC are selected, it will result in no internal clock and a dead CPU.

⚠ CAUTION

When AGC, POSCAGC = 1, and clock fail monitoring, the FCKSM is enabled in the configuration words. If POSCAGCDLY is set to long, a "Clock Fail Detect", OSCCON.CF and RNMICON.CF on some families, can occur because the clock fail timeout expectancy expired before the AGC was able to reach a stable gain step to allow stable crystal operation. Decrease the POSCAGCDLY settings.

If using an AGC and experiencing excessive crystal start-up delays, change the POSCAGCDLY settings.

7.5.3 SAMxx

Problem 9: Auto Gain Control is being used, but intermittent start-up issues are occurring on some boards and/or over temperature.

The SAM product families that employ the equivalent to a crystal Automatic Gain Control, sometimes referred to as Automatic Loop Control Enable (ENALC), or Automatic Amplitude Gain Control (AMPGC) depending on the product family, work quite differently than the AGC of the PIC32MK / PIC32MZ families. In the SAM product families, the manual gain settings are controlled by one of the following, depending on the family:

- XOSCCTRL.ENALC: XOSCCTRL.IMULT Oscillator Current Multiplier, XOSCCTRL.IPTAT Oscillator Current Reference and XOSCCTRL.LOWBUFGAIN are crucial
- XOSCCTRL.AMPGC: XOSCCTRL.GAIN

In these instances, once the gain range has been selected by the user, the automatic gain control will only seek the lowest crystal oscillator power level within the users selected gain range setting.

⚠ CAUTION

If the users gain settings are too low, the automatic gain control will not help them and can result in random oscillation failures across device population, particularly at colder temperatures and/or lower MCU operating voltages. If any of these symptoms are experienced, increase the gain range using the appropriate XOSCCTRL.LOWBUFGAIN = 1 or higher XOSCCTRL.GAIN setting for the family in question. In some instances, better results are attained by disabling the automatic gain control and simply selecting a higher gain setting. The automatic gain control will be better described as a gain attenuator in that for the selected user, the gain setting will attenuate it to achieve the lowest power level to sustain oscillation.

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7.5.4 Crystal Loading Capacitors

Crystal loading capacitors affect not only the crystals but the Automatic Gain Control circuits ability to oscillate. Many users mistakenly assume that the load capacitors they should use in their circuit design are the crystal manufacturer recommended load capacitors. The crystal manufacturers recommended C_{LOAD} value in fact represents the recommended *EFFECTIVE* circuit capacitance, NOT the actual literal capacitance to use.

Notes: Crystal series limiting resistance is not required if the MCU Automatic Gain Control features are used or if no XOSC signal clipping is seen. To calculate the equivalent effective capacitance for selecting the crystal load capacitance:

Equation 1: Crystal MFG $C_{LOAD} = \{([C_{IN} + C1] * [C_{OUT} + C2]) / [C_{IN} + C1 + C2 + C_{OUT}] \} + \text{oscillator PCB stray capacitance}$

Assuming $C1 = C2$ and XOSC pin $C_{IN} \approx$ XOSC pin C_{OUT} , the formula can be further simplified and restated to solve for $C1$ and $C2$ by:

Equation 2: Simplified Crystal C_{LOAD} formula: $C1 = C2 = ((2 * \text{MFG } C_{LOAD} \text{ spec}) - C_{IN} - (2 * \text{PCB capacitance}))$

1. C_{IN} and C_{OUT} must be defined in the data sheet, if not assume 4.5 pF for both.
2. If $C_{IN} \neq C_{OUT}$ then $C_{IN} = C_{OUT} = (C_{IN} \text{ DATA SHT} + C_{OUT} \text{ DATA SHT})/2$.
3. Standard PCB trace capacitance = 1.5 pF/12 mm (i.e., 1.5 pF/0.47 inches).

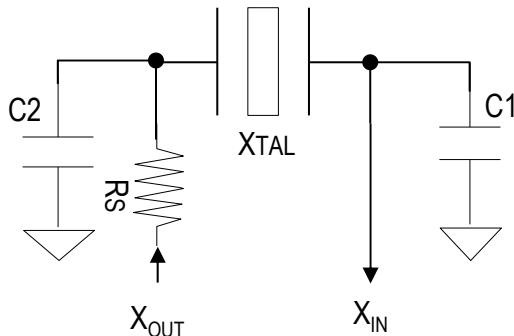


Tip: To increase oscillator gain (i.e., to increase peak-to-peak oscillator signal) follow these:

- Select a crystal oscillator with a lower XTAL manufacturer ESR rating
- $C1$ and $C2$ values also affect the gain of the oscillator. The lower the values, the higher the effective gain.
- To improve start-up performance, make $C1$ slightly smaller than $C2$.

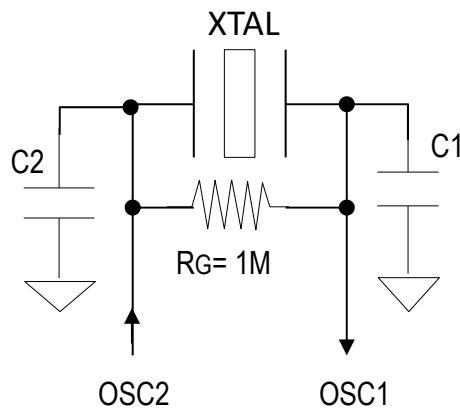
Note: Some of these gain improvement tips are negated by using the Automatic Gain Control (AGC) option.

Figure 7-7. PIC32MZ/PIC32MK/PIC32C and SAM Typical Primary Oscillator Crystal Circuit



Note: Crystal R_S is not required if using Automatic Gain Control or if X_{OUT} and X_{IN} are not clipping. To monitor X_{OUT} or X_{IN} on a scope, the user must use a special FET probe with ≤ 2 pF for good results. A standard Oscilloscope 10-12 pF probe will load and attenuate the crystal giving inaccurate results.

Figure 7-8. PIC32MX Typical Primary Oscillator Crystal Circuit



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7.6 Clock Switching

7.6.1 PIC32MX/PIC32MZ/PIC32MK

Problem 10: The MCU operating frequency is not as expected or no MCU code is executing.

In these product families there exists the technical possibility to do either a silicon hardware clock switch or a software clock switch which can sometimes lead to problems for an unwary user. The configuration word control bits associated with clock switching in these families are:

- **IESO:** Internal External Switchover bit
1 = Internal to External HDW Clock Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal to External HDW Clock Switchover mode is disabled (Two-Speed Start-up is disabled)
- When IESO is set, the CPU hardware will start up executing code on the FRC and automatically switch to the clock source defined by FNOSC when that oscillator source is ready and stable, regardless of whether or not FCKSM clock switching is enabled.
- **FCKSM:** Clock Switching and Monitoring Selection Configuration bits
11 = Software run-time clock switching is enabled, and clock monitoring is enabled
10 = Software run-time clock switching is disabled, and clock monitoring is enabled
01 = Software run-time clock switching is enabled, and clock monitoring is disabled
00 = Software run-time clock switching is disabled, and clock monitoring is disabled

All configuration bits are set to "1" (i.e., Flash Erased Condition) by default unless the user explicitly defines each and every configuration control bit. As a result a user often wants to do a clock switch in software using the OSCCON register at the beginning of their application code. Unfortunately, if the user forgot to clear IESO = 1 there exists the possibility that:

⚠ CAUTION While the users code is attempting to do a software clock switch, the IESO hardware clock switch could simultaneously be in progress resulting in neither clock switch being successful due to logic contention.

⚠ CAUTION One of the two clock switches, HDW or SW, may be successful but which one is not always certain. If the IESO HDW clock switch is successful, the final clock will be the one defined by FNOSC in the configuration words. Otherwise, if the SW clock switch is successful then the clock source is defined by the NOSC bits in the OSCCON register.

⚠ CAUTION IESO = 1 in combination with either FCKSM = 0x11 or 0x01 should be exclusive of each other except in very controlled conditions where the possibility of both NOT happening simultaneously can be guaranteed.

Problem 11: Trying to clock switch from FRC to FRC w/PLL, but the system clock is still only 8Mhz and/or the OSCCON.OSWEN bit indicates the clock switch never completed.

Note: See appropriate data sheet but this is a typical OSCCON.NOSC clock source listing.

Software clock switching only supports switching between any of these combinations using the OSCCON clock switch procedure:

OSCCON.NOSC: New Oscillator Selection bits

111 = Reserved

110 = Backup Fast RC (BFRC) Oscillator

101 = Internal Low-Power RC (LPRC) Oscillator

100 = Secondary Oscillator (SOSC)

011 = USB PLL (UPLL) input clock and divider are set by UPLLCON

010 = Primary Oscillator (POSC) (HS or EC)

001 = System PLL (SPLL) input clock and divider set by SPLLCON

000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits

There is an FRC and a separate SPLL, but no FRC_PLL. In order to do that, the user needs to follow these steps assuming they are already running on an FRC and the users PLL configurations bits were not configured during compile or programming step in anticipation of the FRC_PLL operation later for a future clock switch. If not, then the user must perform these steps:

1. Configure PLL SPLLCON.PLLMULT, PLLODIV & PLLRANGE. (i.e. SPLLCON.PLLIDIV is ignored when PLLICLK = 1).
2. Write SPLLCON.PLLICLK to select FRC as input to the PLL.
3. Perform the OSCCON unlock sequence.
4. Write NOSC = SPLL and OSWEN = 1 to perform the OSCCON clock switch.

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8. Unexpected Resets



Important: In the PIC32MX/PIC32MZ/PIC32MK family of devices, if the user's code attempts to modify at RUN time any configuration registers values in Flash, it can cause either a reset due to a configuration register mismatch and a lock up. Refer to the RCON and RNMICON register for the cause of the reset. Do not attempt any run time configuration register modifications.

8.1 PIC32MX POR/BOR

Problem 12: Sometimes a reset happens on a wake from sleep, or during a clock switch.

- On the PIC32MX family of devices, on a wake from a sleep event, during a clock switch from a relatively low frequency to full speed operation, when using IESO = 1, or two speed start-up, the instantaneous current surge puts a strain on the internal LDO which has a finite response time to sudden current demand changes. If the external VCAP bypass capacitor for the internal LDO is not at least 10 μ F or better and has a capacitor ESR < 1-3 ohms, a POR or BOR can occur. The 10 μ F VCAP is required to stabilize the internal LDO during fast transient currents. A ceramic or solid tantalum cap is recommended. The lower the ESR the faster the response to instantaneous current changes, and therefore, less internal LDO noise and voltage fluctuations.

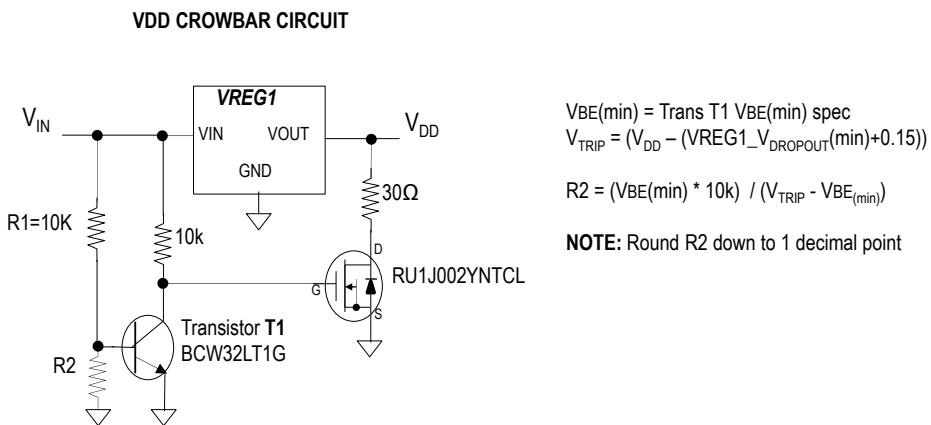
8.2 PIC32MZ/PIC32MK/PIC32C POR/BOR

Problem 13: A lock-up sometimes occurs during a power anomaly or when power cycling the application.

On the PIC32MZ/PIC32MK and some PIC32C families, the "VPOR" data sheet spec is listed as:

- VPOR = VSS+0.3v(max). Which means that in order to guarantee a proper Power-On Reset (POR) the VDD must fall below the POR threshold. In situations where there are transient power anomalies or rapid power cycling of the system, VDD may not always fall low enough or fast enough between the time the power loss began and power levels being restored to normal. How fast the system VDD decays is a function of the amount of BULK capacitance on the VDD power bus and the active load seen by the regulator. The circuit in the following figure addresses the issue by rapidly pulling the VDD low when the regulator input voltage drops below the regulator's drop out voltage to force the VDD < 0.3v, and releases the VDD when input power levels return to ~90% of normal.

Figure 8-1. PIC32MZ/PIC32MK VDD Crowbar Circuit



8.3 NMI and Exception Events

Problem:14: Sometimes after hours, a lock-up occurs.

- In PIC32MX/PIC32MZ/PIC32MK families exception errors, if not explicitly defined by a user's software exception interrupt service routine, the compiler will automatically create one with a "while (1)" instruction inside.
 - If the application encounters an exception error it can result in an apparent lock-up that will require a reset event to recover.
 - To determine the source of the exception, examine the stack in SRAM and find the exception interrupt return address. That address minus one instruction is the instruction that produced the exception interrupt error.

Also try:

See COPROCESSOR 0 REGISTERS, CAUSE Reg 13 ExcCode Field to determine the type of exception.

There are two types of exceptions defined in the MIPS architecture, Precise and Imprecise.

An exception is imprecise when none of the following registers point to the instruction that caused the exception, (i.e. blank). Luckily most MIPS exceptions are Precise and one of the registers below therefore will generally contain the return address.

- COPROCESSOR 0 REGISTERS, EPC Reg 14, Program counter at last exception.
- COPROCESSOR 0 REGISTERS, ErrorEPC Reg 30, Program counter at last error exception.
- COPROCESSOR 0 REGISTERS, DEPC Reg 24, Program counter at last debug exception.

Imprecise exceptions:

- Bus Errors
- Cache Errors
- L2 Cache Errors

In these types of exceptions If the EXL bit in the COPROCESSOR 0 REGISTERS, EPC Reg 12 is set at the time the imprecise exception is recognized, the EPC would not be updated: for this case, the EPC would point to an instruction within the interrupt handler instead which is meaningless. A similar case can occur for late-arriving Floating-Point exceptions.

- If the user's application has enabled the WDT and an exception occurs in which the user did not explicitly define and exception handler, the compiler default exception handler with the while (1) will cause the WDT to reset the part. Refer to the RCON and RNMICON registers.

Problem 15: The device does not function. It is continuously stuck in a hard fault or a reset.

- In SAM and PIC32CM families this can occur if the PCB designer inadvertently connected the 1.2V VDDCORE to VDDIO. This can cause a variety of issues from hard fault lockups, device damage, or if the WDT enabled chip resets.

8.4 ESD/EMI/EFT Events

In most applications the ESD, EMI, and EFT sources occur external to the application PCB. As such, users must focus protection on all external pathways to the electronic logic. Think of the PCB as your home. When you install a security system you concentrate the protection on all entry and exit points to prevent burglars from gaining access. The same is true for the ESD, EMI, and EFT. The first level of protection must be to prevent access to the application from disruptive electrical events, otherwise once they have breached the electronic interface and/or power busses they can infiltrate and affect all of the subsystem's logic including the MCU. The most common results of an ESD, EMI, or EFT event are as follows:

- MCU and system Resets
- MCU Lockups
- Component failure

DEFINITIONS:

- ESD: Electrostatic Discharge
- EMI: Electromagnetic Interference
- EFT: Electrical Fast Transients

Simplified Protection Rule Recommendations:

- Protect all signals that come from, or go to external ports using various filters or transient suppressors
 - Protection should also extend to external power input or output sources
 - Unused MCU pins tie to ground through a 1k resistor
 - Do not connect chassis or external port cable shields to logic ground either directly or via a capacitor. Maintain, whenever possible as much isolation as prudent. Most ESD, EMI, and EFT events originate externally. As such, the application enclosure and cable shields become a primary conduit to conduct the electrical disturbance into the heart of the electronic logic which can result in unexpected behavior.
- ESD, EMI, and EFT disturbances are transient type events in the 1 ns-20 ns range as far as peak current or power.

Notes:

1. There is much more comprehensive information available regarding ESD, EMI, or EFT protection, which can be found on the Microchip web site, in a document titled: [AN2587 - EMI, EMC, EFT, and ESD Circuit Design Consideration for 32-bit Microcontrollers](#), or on any of the 32-bit product web pages under the tab "Documentation" > Application Notes.
2. ESD certification testing covers two basic types of tests, CONTACT DISCHARGE and AIR DISCHARGE. Contact discharge as the name implies is an electrical discharge directly anywhere on the exposed surface of the applications enclosure including the Screen display, keyboard, push buttons, USB ports, RS232 ports, SD ports and so on, but never directly to the surface on the PCB. PCB ESD tests only allow for AIR DISCHARGE, an electrical arc discharges directly above the PCB, usually 1 inch.

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9. Debug Issues

Problem 16: The PC does not recognize ICD4 and/or PICKIT 4.

- When using the Microchip development tools, if the tool will not function properly or at all, it may be as a result of an incorrect device driver being installed. If the Windows® Operating System (OS) installs its default USB device drivers for a Microchip development tool, the wrong USB driver may have been installed.

To correct the issue, refer to: ww1.microchip.com/downloads/en/DeviceDoc/51417E.pdf.

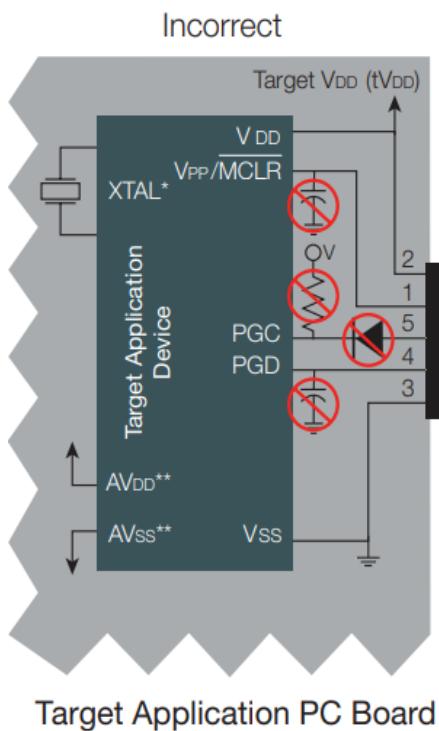
9.1 ICD4/REAL_ICE ICSP (PGDx/PGCx) Debug Issues

Problem 17: In debug mode why are some PIC32MX/PIC32MZ/PIC32MK register values not showing as expected?

- Some products have a slightly different behavior in debug mode. For example, on some devices, on a break point, certain peripherals may not halt as expected. Some products have reported that the DMA controller continues unabated in the middle of a packet transfer until complete, despite the peripherals being halted. This can cause data corruption in some cases. For a list of known issues in any version of MPLAB® X IDE and debugger/programmer, refer to the respective readme files at the following location:
 - C:\Program Files (x86)\Microchip\MPLABX\v5.4\docs. Substitute your current version in place of v5.4

Problem 18: Unable to connect with ICD4 or Reallice to target.

Figure 9-1. ICD4/Reallice Target Circuit Design Precautions

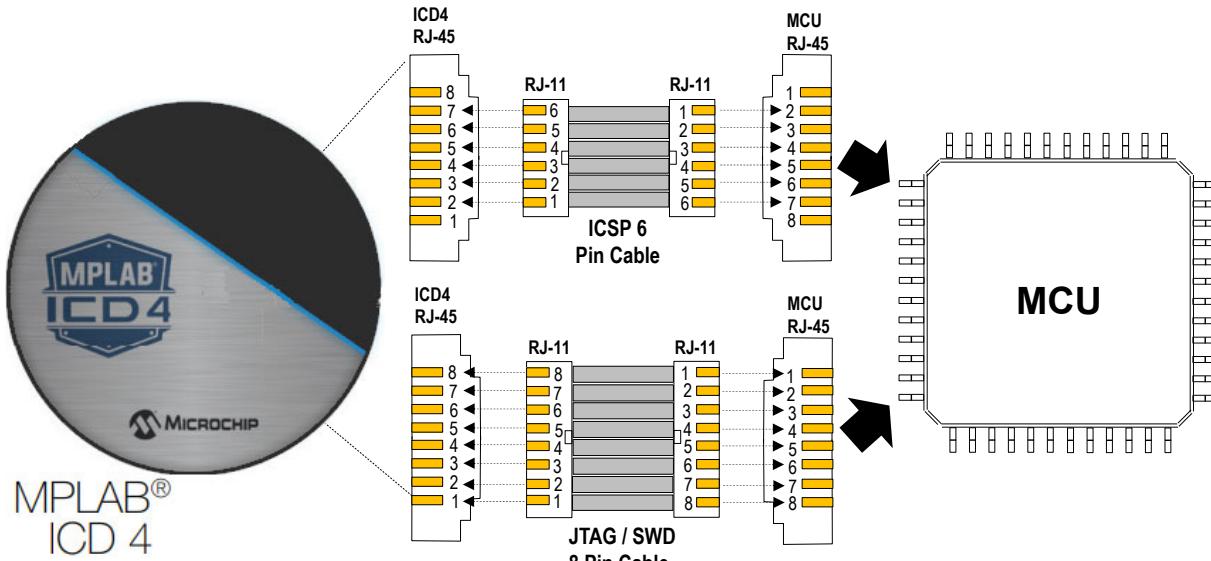


Note: The pinout shown is for the ICD 4 RJ11 connector.

- Do not use capacitors directly on the MCLR: They will prevent fast transitions of the MCLR needed to meet timing for entering and sustaining debugging, or programming modes
- Do not use multiplexing on active PGCx/PGDx: They are dedicated for communications to MPLAB ICD 4/ Reallice
- Do not use capacitors on PGCx/PGDx: They will prevent fast transitions on data and clock lines during programming and debug communications
- Do not use diodes on PGC/PGD: They will prevent bidirectional communication between MPLAB ICD 4 and the target PIC® MCU

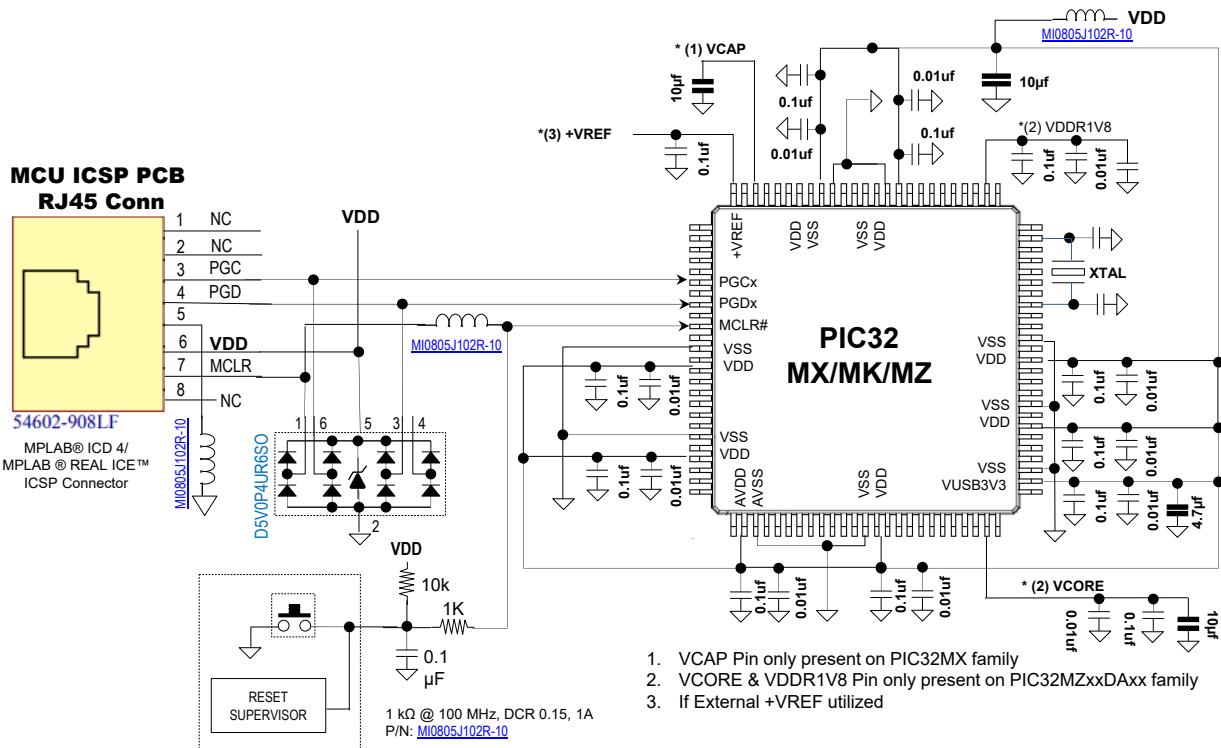
- Do not exceed recommended cable lengths: Refer to the Hardware Specification of the MPLAB ICD 4 online help or user's guide for cable lengths

Figure 9-2. ICD4 ICSP/JTAG/SWD Wiring Diagram

MPLAB®
ICD 4

Signal	ICD4 RJ45 (Female Conn)	ICD4 RJ11 Cable (Male Conn)		MCU RJ11 Cable (Male Conn)		Target MCU RJ45 (Female Conn)
		(6) Pin RJ11	(8) Pin RJ11	(6) Pin RJ11	(8) Pin RJ11	
TMS / SWDIO	8	NC	8	NC	1	1
AUX	7	6	7	1	2	2
TCK / SWTCLK / PGC	6	5	6	2	3	3
TDO / SWO / PGD	5	4	5	3	4	4
GND	4	3	4	4	5	5
VDD	3	2	3	5	6	6
NMCLR (#MCLR)	2	1	2	6	7	7
TDI	1	NC	1	NC	8	8

Figure 9-3. PIC32MX/PIC32MZ/PIC32MK ICSP and Reset Circuit Diagram



9.2 JTAG/SWD

Figure 9-4. JTAG and Serial Wire Interface Diagram

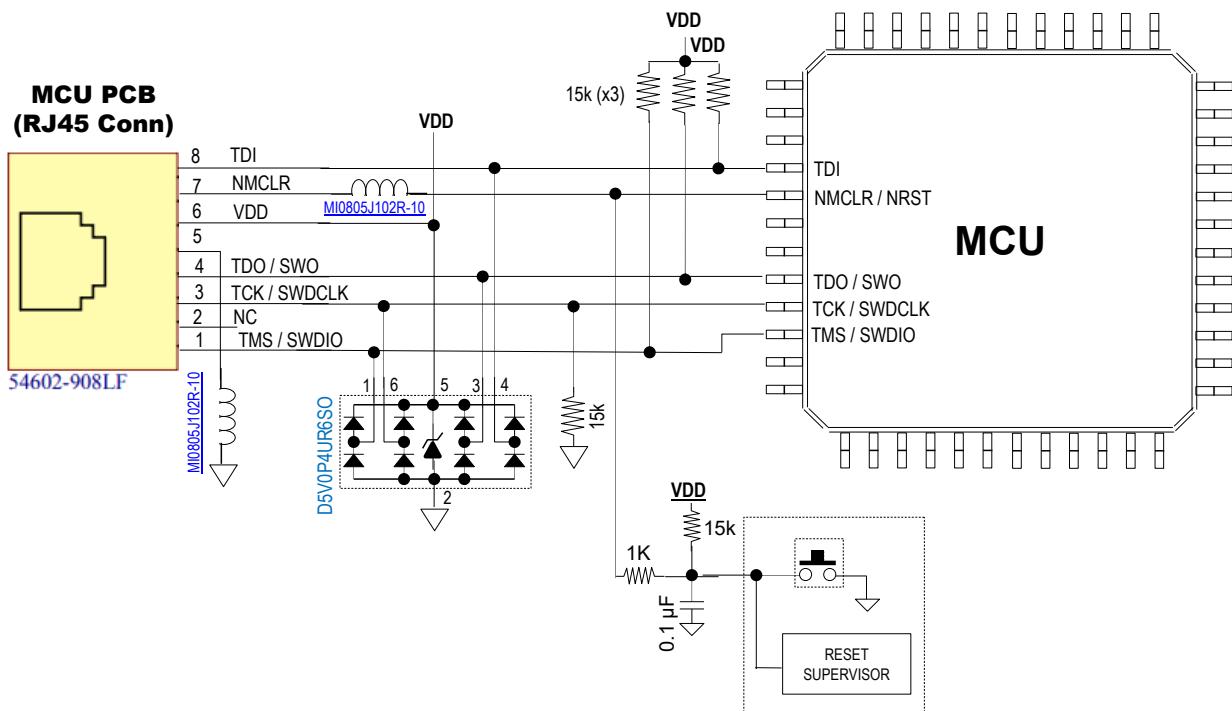


Figure 9-5. All Debugger RJ45 MCU Target Side interface Pinout

MPLAB® ICD 4 / REAL ICE			DEBUG									
Connector	Pin #	Pin Name	ICSP (MCHP)	MIPS EJTAG	CORTEX® SWD	JTAG	DW(IRES)	UPDI	PDI	AW	AVR®_ISP	TPI
	8	TTDI		TTDI		TDI					MOSI	
	7	TVPP	MCLR	MCLR	MCLR							
	6	TVDD	VDD	VIO_REF	VTG	VTG	VTG	VTG	VTG	VTG	VTG	VTG
	5	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
	4	PGD	DAT	TDO	SWO	TDO		DAT	DAT	DATA	MISO	DAT
	3	PGC	CLK	TCK	SWCLK	TCK					SCK	CLK
	2	TAUX	AUX	TAUX		RESET	SW-DAT		CLK		RESET	RST
	1	TTMS		TTMS	SWDIO	TMS						

Problem 19: Programming works, but not the debug.

- In programming mode, the programmer supplies the clock necessary to erase and program the target through the ICD4 PGC/TCK/SWCLK signal interface. However, in Debug mode the MCU oscillators must be running. If MCU system clock source is not working (POSC, XOSC, XOSC32, FRC and so on) your debugger will not function. Check clocks sources and user clock configurations.

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10. PCB MCU Connections



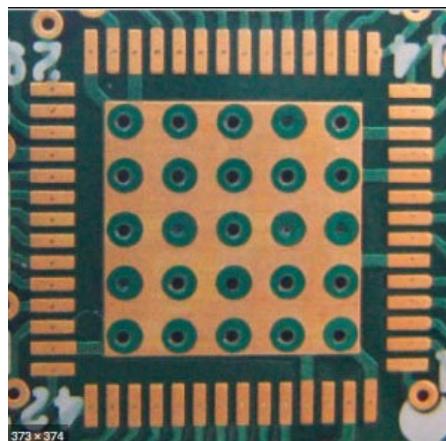
Important: In the PIC32MX/PIC32MZ/PIC32MK family of devices, the function priority of any pin is defined by the order of the signals left to right in the pin map tables. Any pin function utilized by the user will override all listed functions to the right of it in the pin name.

10.1 Exposed Pad

Problem 20: What needs to be done with the exposed pad on the MCU package for the PCB design?

The user should attach (solder) the exposed pad on packages that have them, to a matching perimeter ground landing beneath the package punctuated with vias to the ground layer like indicated in the following figure. This is not a substitute for the designated power ground pins on the device, they must still be connected to ground. This makes for easy connections of ground pins to the ground plane.

Figure 10-1. Exposed Pad Landing Pattern Example



10.2 PIC32MX/PIC32MZ/PIC32MK VUSB3V3 Pin

Problem 21: Some of the I/O pins and alternate function pins are not working at all even though they are configured correctly.

USB On-The-Go (OTG) consists of the following cable interface signals:

- D+ (Standard USB Data)
- D- (Standard USB Data)
- VBUS (Standard USB +5v)
- USBID (OTG Support, needs)
- VBUSON (OTG Support)

In the PIC32MZ/PIC32MK family of devices, the internal USB PHY transceiver, and therefore all of these interface I/O pad signals are powered by the VUSB3V3, not the VDD. The standard USB signals in the list above are dedicated pins and not multiplexed with any other alternate function or I/O. The USBID and VBUSON functions have alternate functions and I/O mapping capabilities.

⚠ CAUTION

Even if not using USB, the VUSB3V3 must be connected to the VDD in order to power any of the alternate functions or I/O that share the pins with USBID and VBUSON for those devices that have them.

⚠ CAUTION

If using the USB but OTG support is not required, the USBID and VBUSON pin features must be disabled in the configuration words in order to use any low-priority functions mapped to those pins. When the USB is enabled these OTG USB extensions USBID and VBUSON become active unless disabled in the configuration words.

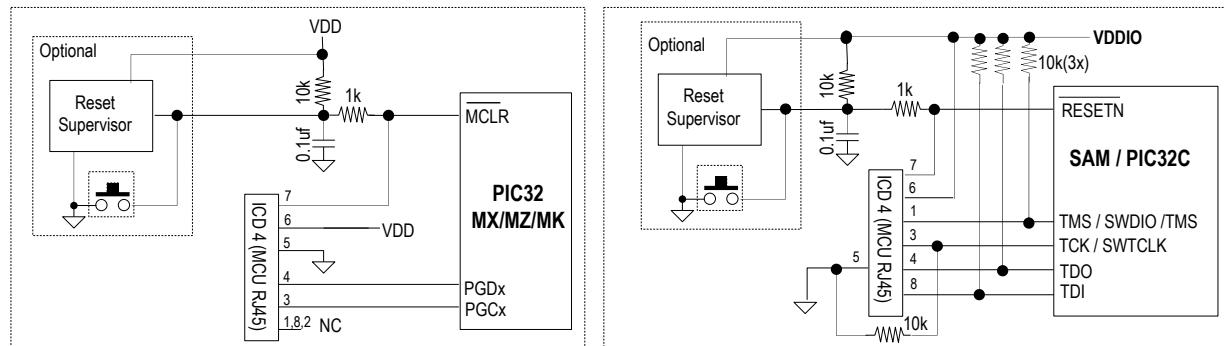
Note: The PIC32MZ devices with USB do not have a VBUSON OTG signal.

10.3 MCLR#/RESETN

Problem 22: MPLAB does not connect to the PIC32 target device.

- It is critically important that there is a 470-1K isolation resistor separating the PIC32 ICSP MCLR input from the 0.1uf cap and reset supervisor, or reset push button

Figure 10-2. MCLR#/RESETN Circuit Diagram



10.4 VBAT

Problem 23: Do bypass caps need to be used on the VBAT input pin?

It is recommended to place a 4.7 uf and 0.1 uf capacitor in parallel across the VBAT input pin to ensure that during the internal switch over from VDD power to VBAT power there are minimal transients as depicted in the diagram below.

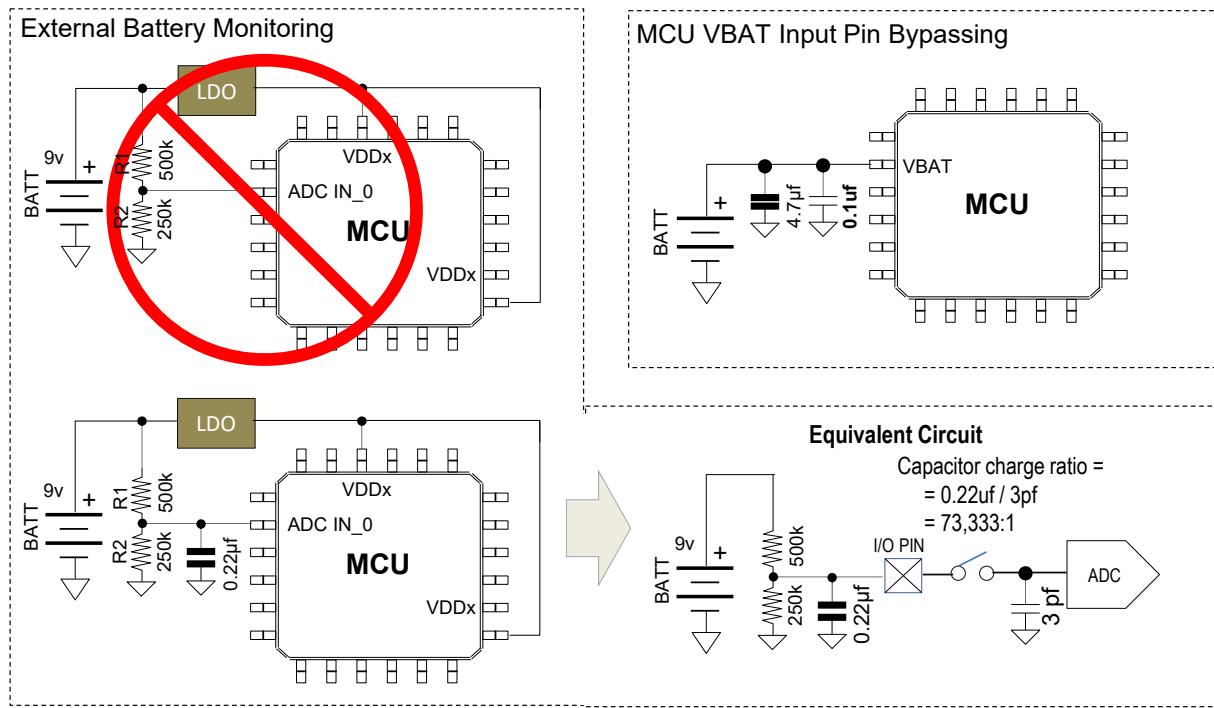
Problem 24: The external battery voltage cannot be measured correctly using the ADC.

When monitoring an external battery, typically users use a voltage divider similar to what is shown below to insure:

- They scale the battery voltage to less than MCU (VDDANA-0.6v) for proper ADC measurements
- That the battery monitoring will draw minimal power from the battery to extend battery life in MCU low power modes

Due to the large, required resistors used in the battery voltage divider to minimize static power drain from the battery the sample time required for the ADC to measure the battery is either prohibitive in the application due to other ADC analog sampling responsibilities in the application, or it is simply not achievable. A simple workaround is to use a capacitor at the input to the ADC battery input channel. The capacitor will fully charge from 0v in $\sim (5 * R1 * C)$. When the ADC measures the battery voltage after that period, an infinitesimal small amount of charge from the external capacitor will instantly be transferred to the ADC internal $\sim 3\text{pF}$ internal hold capacitor that would require only the minimal sampling ADC time at a reasonable ADC throughput rate. The effective ADC sample/hold RC sampling time now is simply the ADC internal $R_{SAMPLE} * C_{SAMPLE}$. Internal ADC R_{SAMPLE} is generally between 2-5k. R1 is a non-factor now.

Figure 10-3. VBAT Bypassing and Battery Monitoring Diagram

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11. Serial Data Corruption Errors

11.1 Impedance Matching

Problem 25: There is frequent to intermittent data corruption between the MCU and target IC.

Signal Integrity issues or reflections can occur due to fast signal rise and fall times, and impedance mismatches between source and target device(s). It follows that the higher the signal frequency, then the rise and fall times are faster. (See the Signal Integrity Figure below.)

A general guideline to determine when the transmission line termination approach is necessary is:

- Terminate the transmission line in its characteristic impedance when the one-way propagation delay of the PCB trace is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster)

Since most designers do not know the PCB trace propagation delay, the following procedure should be used:

- Check that all high-speed signals in excess of ~15Mhz are terminated with a series resistor at the point of origin, (i.e., source of the signal), or in the case of bi-directional signals, at all device output pins on the bus

To determine which termination resistor value to use based on the user's PCB design specifications, calculate the line impedance at:

<https://www.eeweb.com/tools/microstrip-impedance> = Trace Impedance

Equation 3: PCB signal series termination resistor(s) value = $\{[(VDD-VOH(\min)) / IOH(\max)] - \text{Trace Impedance}\}$

Table 11-1. Typical PCB Trace Characteristics Illustration Only

Trace Width	PCB Height between layers	Trace Thickness	PCB Substrate Dielectric	Trace Impedance
0.175 mm	113 µm	1.41 mils (1 oz Cu)	4	54.6 Ohms

For example,

PCB signal series termination resistor(s) value = $\{[(VDD-VOH(\min)) / IOH(\max)] - \text{Trace Impedance}\}$

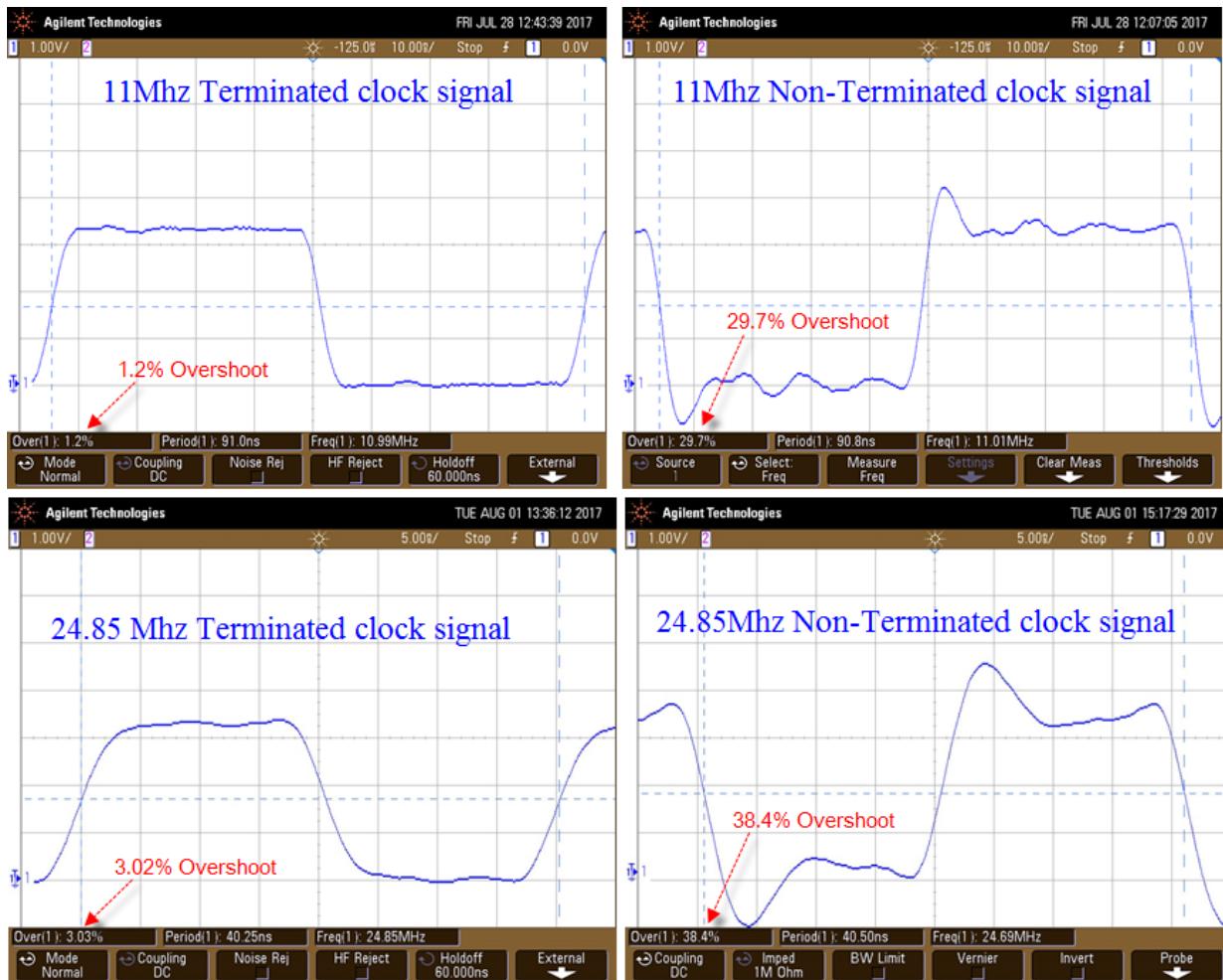
$$= \{(3.3-2.4) / 10 \text{ mA} - 54.6 \text{ ohms}\}$$

= 35.4 ohms (Rounding up or down to the nearest standard resistor value)

= 33 ohms

Note: Too much termination resistance will impact the slew rate and speed of the signal to the point that the signal no longer meets specified timing requirements.

Figure 11-1. Signal Integrity Illustration of Before and After Transmission



11.1.1 Abbreviated General High-Speed Signal Layout Guidelines

1. Layout differential and high-speed traces first to maintain differential impedance matching when required on PCB layer 1 adjacent to ground plane layer on the same side of the PCB as the signal source/destination for MCU devices.
2. Ensure clock and high-speed signal traces have unbroken reference ground plane with no gaps or voids beneath them.
3. Copper pour all voids on signal layers with signal ground.
4. Minimize the use of vias throughout the design on high speed signals. Vias add capacitance, impedance changes, and frequency to signal traces which leads to reflections and radiated EMI.
5. Use the 3-Width rule to provide enough trace separation to avoid cross talk problems.

Note: See [Complete PCB Layout Guidelines](#) in the back of this document.

11.1.2 PIC32MZ/PIC32MK

In lieu of using termination resistors for MCU high-speed signals, some device families, such as the PIC32MZ, PIC32MK have I/O output pin slew rate control features. By attenuating the rise and fall times you can improve signal integrity and eliminate data transceiver errors.

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11.2 Ground Loops

Problem 26: There is intermittent data corruption on communication links between remote PCB stations or equipment.

- Ground loops can be caused when equipment between different locations are digitally interconnected through cables sharing a common digital ground, but whose local PCB digital grounds are at different potentials as depicted in the figure below. The amount of ground loop current is dependent on the current drawn by the active loads on the same AC power bus or even across different power busses on a different AC phase. On Non-Isolated logic supplies, such as switch mode supplies, this causes the grounds to be ever so slightly at different voltages, usually in the millivolt range as the digital ground is relative to AC neutral potential. On the same PCB, since the ground offset is common to all the logic on a singular PCB there is no problem between the individual MCU component signals on the same PCB.

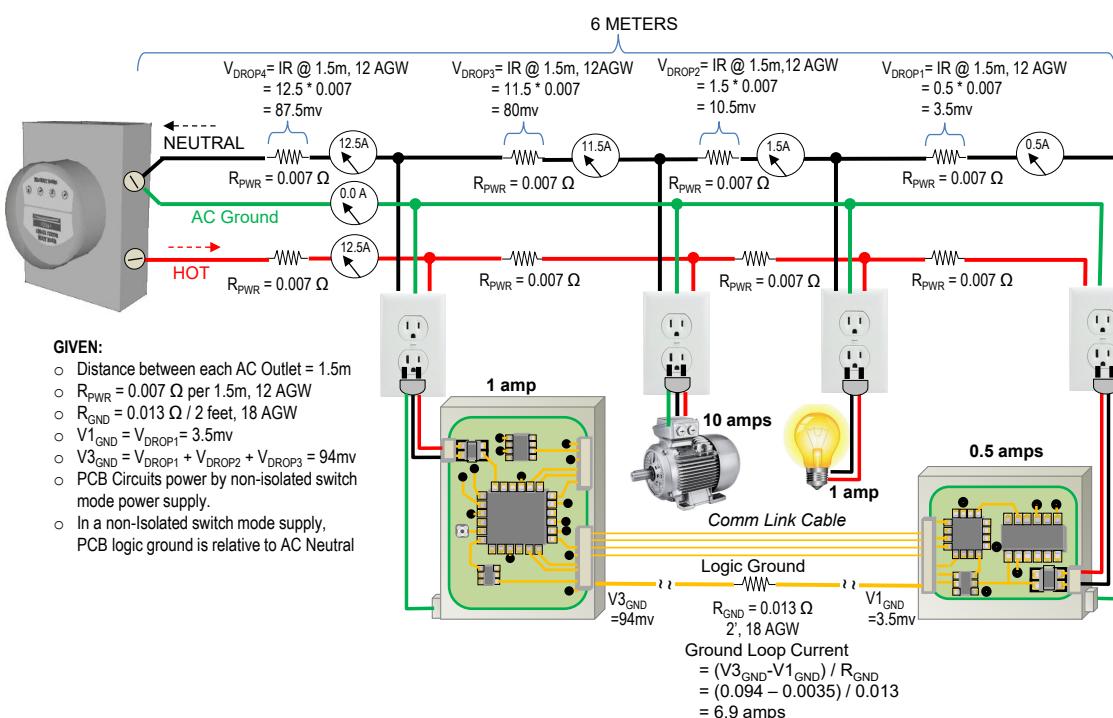
When multiple boards are interconnected through cables is when the problem manifests. Since $I = V/R$ and also since the resistance of typical interconnected PCB cabling is relatively small, even a very small logic ground offset can cause large ground loop currents between PCB systems. This ground offset changes the relative VIL/VIH and VOL/VOH signaling thresholds between the remote PCB systems because VIL/VIH/VOL/VOH are always relative to their local logic ground. During periods when many AC loads are active, the signaling problem can become worse and likewise may improve as the number of AC active loads are turned off or disabled. This is why 4-20 mA current loop communication between equipment in industrial control systems is popular because it does not depend on, or use communication link grounding. Most communication between your household thermostat and HVAC is 4-20 mA current loop control.

- If ground loop issues are suspected, a simple way to confirm or deny this is to power the interconnected PCB systems from the same AC outlet. If the communication link data corruption errors disappear then it is confirmed, a ground loop current issue exists that will need to be addressed.

Options:

- Electrically isolate the PCB communications link cable interface signals using components similar to those described in [Signal Isolation Components](#) and eliminate the digital ground wire interconnect or use a higher voltage signaling level, such as RS232 that improves both noise immunity and ground loop offset nullification.
- Use an isolated power supply to power the PCB systems

Figure 11-2. Ground Loop Illustration Example



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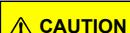
11.3 SPI/SQI

Problem 27: Clock and data are present, but the target SPI device it is not responding.

- The Serial Peripheral Interface (SPI) has four typical transmission modes for data. SCK polarity describes the default idle state of the clock, and the SCK Phase/edge describes which edge of the SCK the data will be valid on.

Table 11-2. SPI Modes of Operation

MODE 0	SCK Polarity – CPOL/CKP	SCK Phase – CPHA/CKE
0	0 = SCK Idle Low	0 = Rising Edge Data Sampled
1	0 = SCK Idle Low	1 = Falling Edge Data Sampled
2	1 = SCK Idle High	0 = Falling Edge Data Sampled
3	1 = SCK Idle High	1 = Rising Edge Data Sampled



Most SPI peripherals on the SPI bus only operate or accept one or two modes of operation defined above in the tables. All devices on the SPI bus must operate or be configured for the same mode. Ensure the MCU SPI is configured in a SPI mode compatible with the remote SPI devices on the SPI bus. If either of these requirements are not met the user will not have a successful SPI communication with the target. Compare the MCU SPI settings with the SPI target peripheral data sheet modes.

Problem 28: Why is the SPI data always shifted by one bit?

- In designs where there is only one SPI target in the system, designers often save pins simply by tying the target SPI #CS to the ground in an effort to use only the minimum 3-wire SPI interface. In that case, the user must ensure a proper pull-up if the SCLK polarity is idle high, or a pull-down if the slave SCLK polarity is idle low. The SPI master has a programmable SCLK polarity bit that the user sets to match the target default SCLK polarity. It also has a programmable Clock Edge.



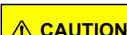
If a user selects the SPI clock edge to output data changes on transitions from the active clock state to the Idle clock state and the clock polarity is idle high then, without a master supplied chip select to the target, when the MCU powers up the I/O pins used are Tri-Sate and float low. When the SPI is enabled and the I/O pin SCLK function is output, the pin will transition from the Tri-States floating logic low to the SCLK idle logic high state. The target device will see this as a valid clock edge and shift whatever is in the slave shift register Msb out, good, bad, or nothing. After this point on every transfer will be off by one bit. It is highly recommend to use #CS even if there is only one target SPI in the system to avoid this possibility.

Problem 29: Why is the SPI /SQI data corrupted?

- In PIC32MX/PIC32MZ/PIC32MK ensure to set the SPIxCON.SMP bit when in master mode for the fastest data rates. There is a significant speed difference available depending on the state of the SMP bit in master mode.
- There is also a difference in the maximum speed that the SPI can achieve depending on the following::



Use the dedicated SPI SCLK pin functions as opposed to the PPS remappable SCLK in PIC32MX.MZ/ PIC32MK families for higher speeds.



Use the corresponding IOSET pins for the SPI interface signals in the SAM / PIC32C families for the highest speeds possible.

- SQI peripheral modules have maximum input clock restrictions. Check the errata and data sheet for limitations.
- At higher speeds ≥ 15 MHz use termination resistors on all high-speed output driver side signals. (See the design example below, and [Impedance Matching](#).)

Abbreviated General High-Speed Signal Layout Guidelines

1. Ensure the clock and high-speed signal traces have an unbroken reference ground plane with no gaps or voids beneath them.
2. Copper pour all voids on signal layers with signal ground.
3. Minimize the use of vias throughout the design on high-speed signals. Vias add capacitance and impedance changes at frequency to signal traces that lead to reflections and radiated EMI.
4. Use the 3-Width rule to provide enough trace separation to avoid cross talk problems.

Note: See [Complete PCB Layout Guidelines](#) in the back of this document.

Figure 11-3. SPI and SQI External EEPROM/SRAM/FLASH Design Diagram

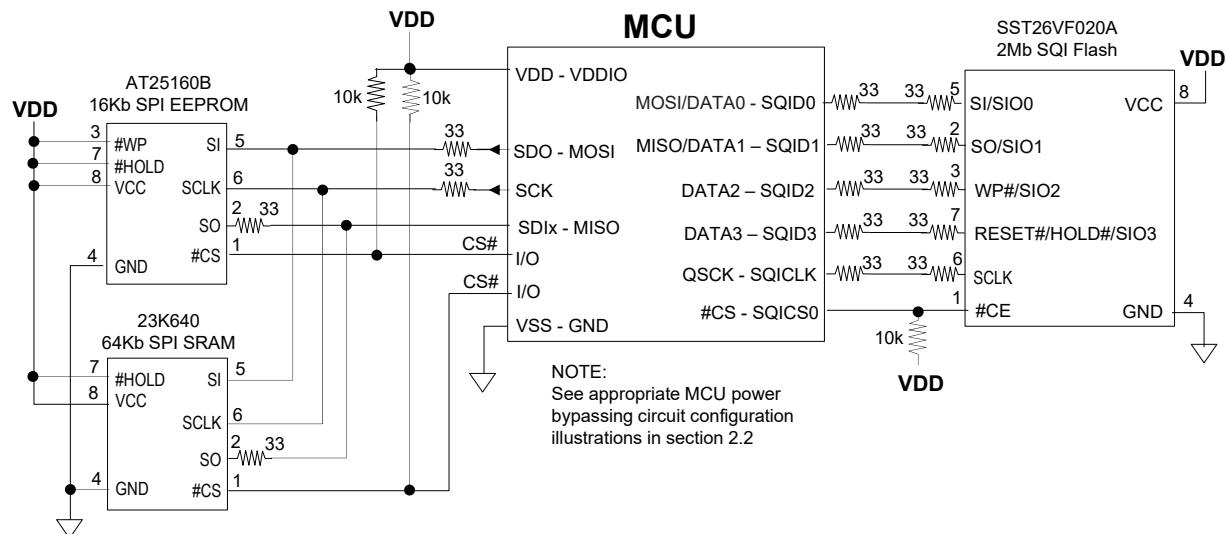
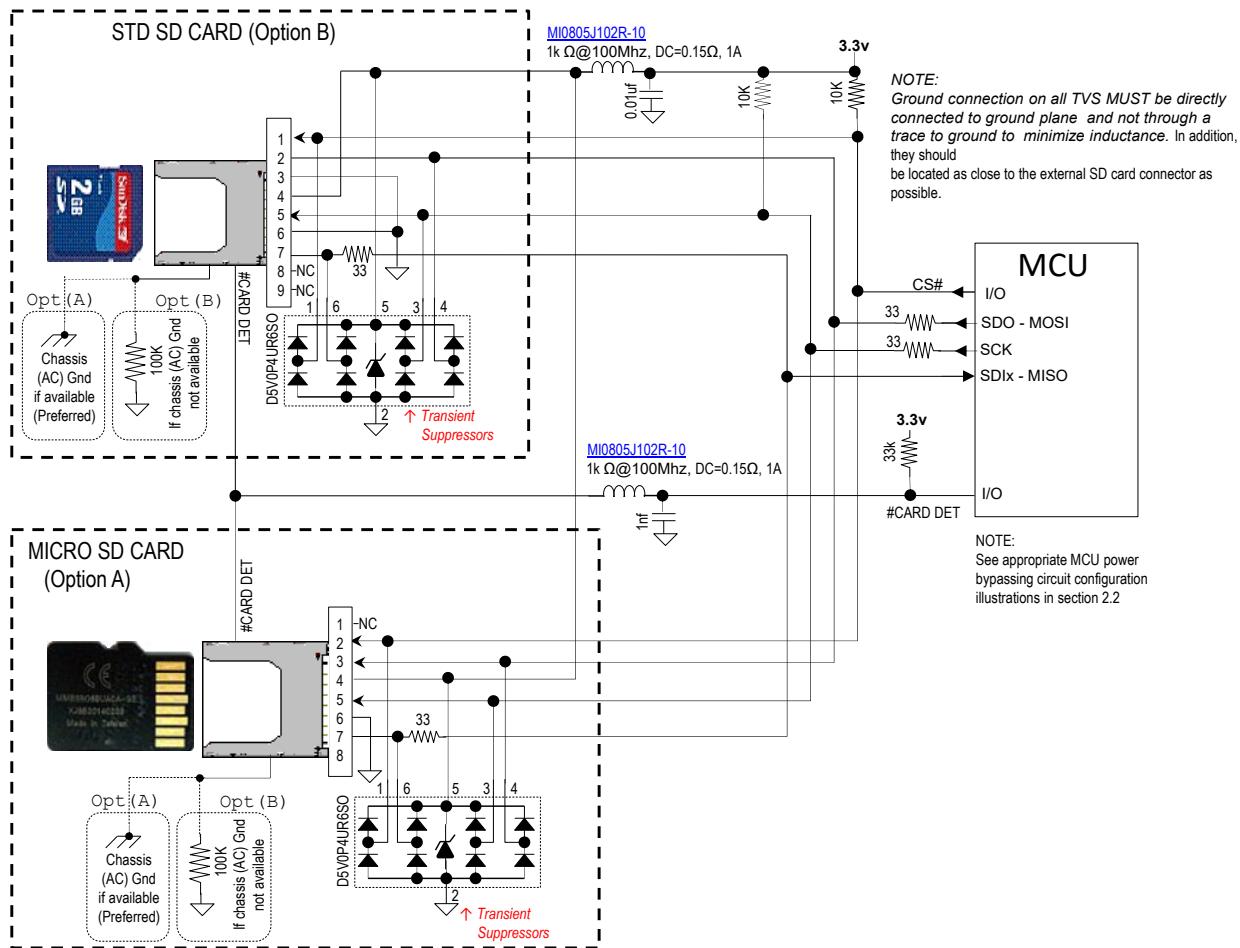


Figure 11-4. SPI SD Card Design Example Diagram



11.3.1 Key SPI SD Card Protection Design Points

- The SD card receptacle must be connected to the chassis AC earth ground if possible, or through a 100k resistor to digital ground to attenuate any potential ESD discharge event.
- Signal termination resistors in this case are not required, because the ESD protection device [CM1422-03CP](#) has a 100 ohm series resistor as part of the ESD RC filter.
- All SD card signals are routed through the ESD RC filter.

There is comprehensive information available on ESD, EMI, or EFT on the web site that can be found in the document: [AN2587 - EMI, EMC, EFT, and ESD Circuit Design Consideration for 32-bit Microcontrollers](#), or on any of the 32-bit product web pages, which are available under the tab *Documentation > Application Notes*.

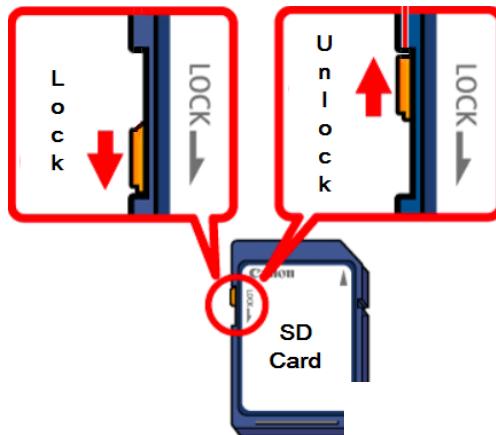
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11.4 SD Host Controller (SDHC)

Problem 30: The SD Card will not write or erase, only read.

- The SD Card may be locked. There is a small side switch on the side of your SD card. Sometimes, while handling the card, the slide can sometimes get turned on, rendering the SD card write protected.

Figure 11-5. SD Card Write Protect Switch Diagram



Problem 31: The SD Card cannot be accessed.

- If you are using a software framework or stack, it may require a Card Detect (i.e., #CD) input to the MCU interface



Check if the MCU interface and SW configuration require card detect.



The Card Detect is a mechanical tension switch that closes and connects the card detect to ground when an SD card is inserted. If your MCU and SW interface requires card detect, ensure the switch is still functional. Check the card detect signal and confirm it is logic low. This status signal requires a pull-up if used.

- There are three types of SD cards; Standard, Mini and Micro. They all support SPI and SDHC interfaces but interface connections vary.



If this is the first time using an SD card in the application then double check the schematics and connections to make sure they match the interface pinout listed in the following figure.

- Try reducing the SD Card CLK frequency to slow down the data access rate. If this solves the problem, then there may be a PCB trace length and/or an impedance matching issue relative to the data rates that are expected.

Figure 11-6. Standard SD, Mini and Micro SD Card - SPI and SDHC Pinout Diagram

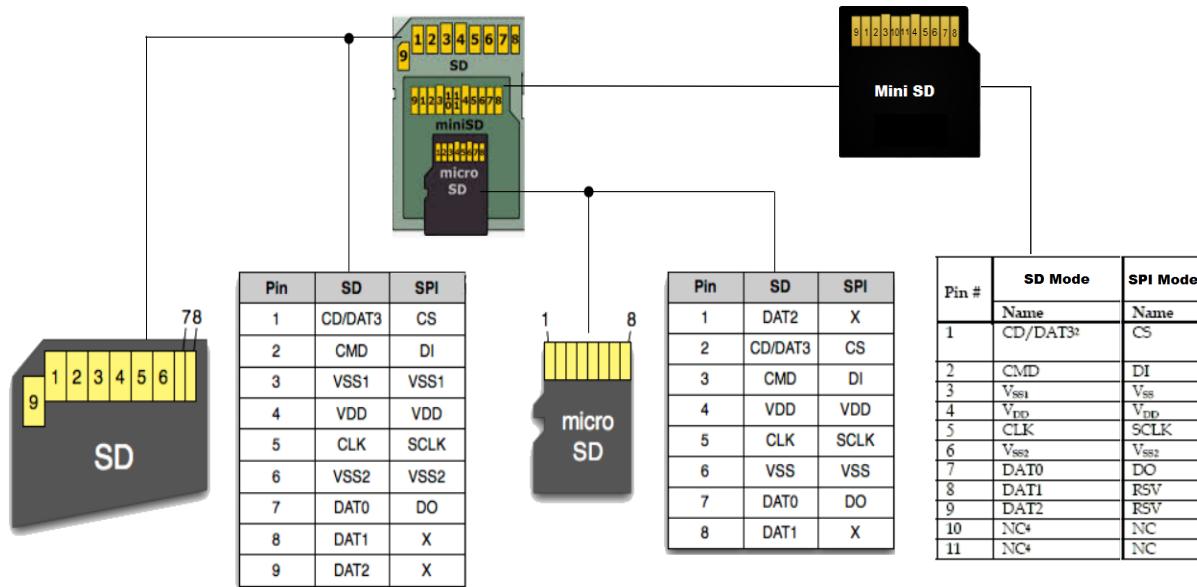
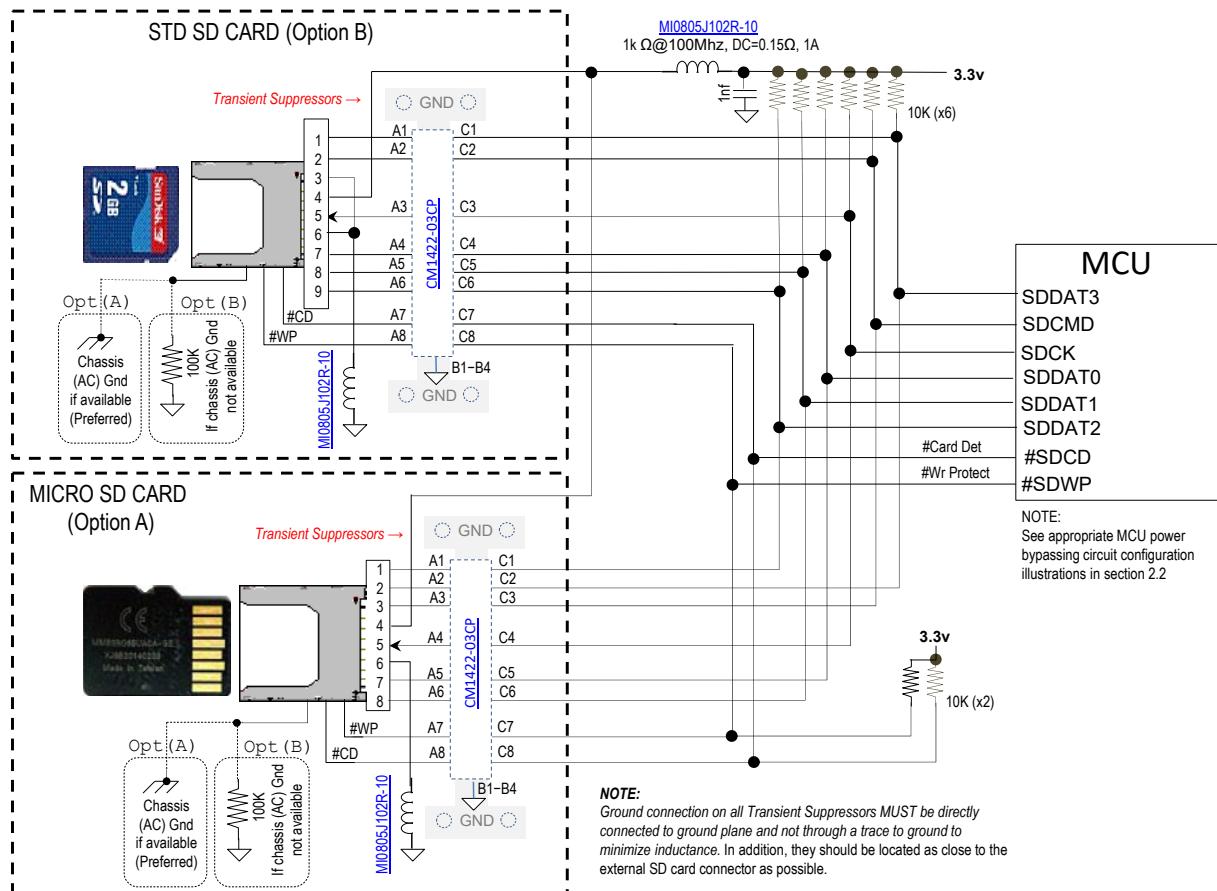


Figure 11-7. SD Card SDHC Design Example Diagram



11.4.1 Key SD Host Controller (SDHC) Protection Design Points

- The SD card receptacle should be connected to the chassis AC earth ground if possible, or through a 100k resistor to digital ground to attenuate any potential ESD discharge event
- Signal termination resistors in this case are not required, because the ESD protection device CM1422-03CP has a 100 ohm series resistor as part of the ESD RC filter
- All SD card signals are routed through the ESD RC filter

There is comprehensive information available on ESD, EMI, or EFT on the Microchip web site that can be found in the document: [AN2587 - EMI, EMC, EFT, and ESD Circuit Design Consideration for 32-bit Microcontrollers](#), or on any of the 32-bit product web pages under the tab *Documentation > Application Notes*.

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11.5 UART

Problem 32: Why is the UART data corrupted?

- The UART baud rate error cannot exceed $\pm 3\%$ total by industry specification (i.e., $\pm 1.5\%$ Transmitter plus $\pm 1.5\%$ Receiver allowance) between source and target. There are two sources of error in the MCU UART:
 - The MCU UART clock source % accuracy error
 - $BR_{ERR} = (((BR_{DESIRED} - BR_{CALCULATED}) / BR_{CALCULATED}) * 100\%)$
TOTAL MCU UART BAUD_RATEERROR = $(BR_{ERR}\% + \text{UART clock source \% error}) \leq 1.5\%$



If using an internal RC clock for the UART clock source, check the data sheet and confirm if the RC plus PLL or DFLL has the required guaranteed % error accuracy. In many MCU's an external clock reference like a crystal or clock oscillator are needed for the accuracy required.

- Unique to the PIC32MZ/PIC32MK family, REFCLK can also be selected as a UART clock source.



Never use REFCLK as a source clock for any asynchronous peripheral (i.e., UART, CAN, ADC, and so on). REFCLK produces a pseudo fractional clock frequency by cycle stealing to produce an average frequency, meaning that over a given unit of time the number of clock pulses are not consistent. This means that the UART bit times cannot be guaranteed.

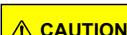
Problem 33: Why is the first UART byte always wrong after a power-up or wake from sleep?

- On any reset the I/O pins are Tri-States and generally float low, remaining that way until the user's code initializes the UART and assigns the pins. For other UART devices in the application the High-Z floating logic low condition is perceived as a "START" bit. The target UART Rx sees a false floating low start condition, and will begin sampling the Rx pin data even if there is no actual transmitted data.



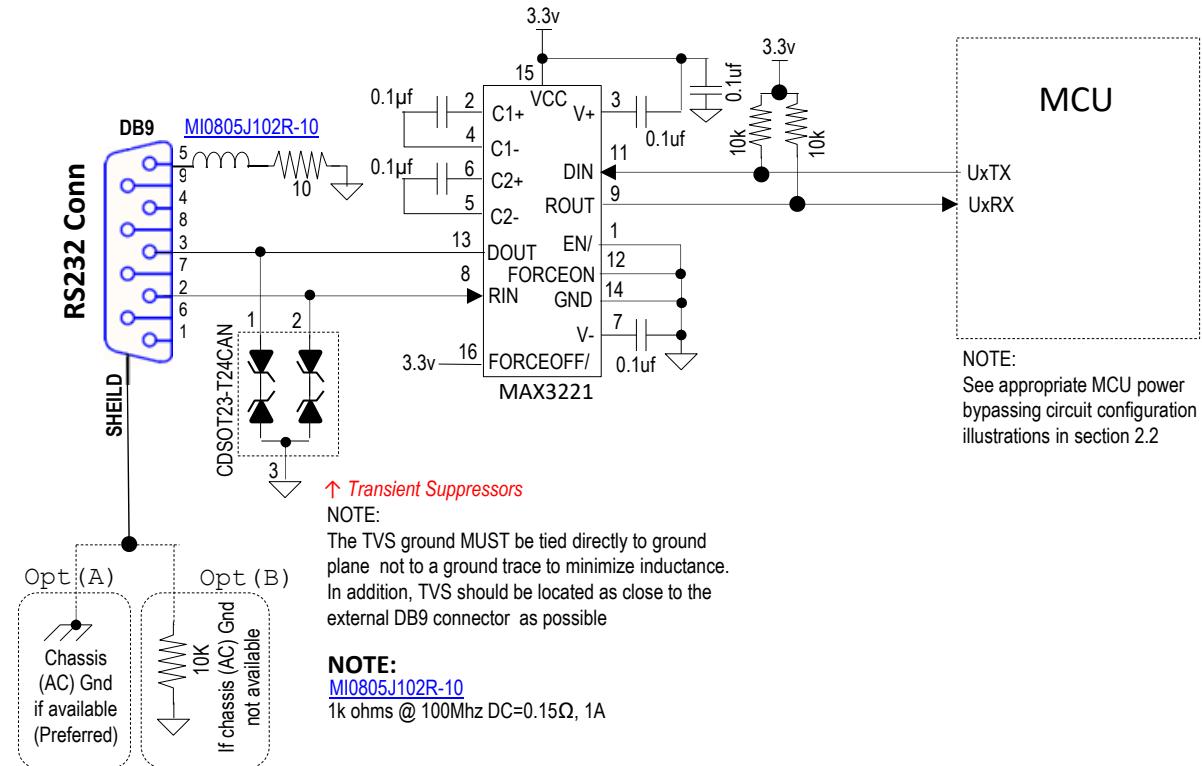
Always use pull up on the MCU UART Tx and Rx pins. The resulting MCU logic high on the Tx and Rx logic in the system during the MCU reset and initialization period represents the UART's natural idle state.

- On many MCU devices and in some sleep modes, the UART clocks are disabled and re-enabled on wake from sleep by an interrupt triggered by the reception of a START bit (i.e., logic high-to-low transition). The falling edge of the START bit is what synchronizes the sampling bit clock of the UART receiver. However, by the time the MCU can wake from sleep and re-enable the clocks, the receiver bit sampling is no longer in phase with the external transmitted Tx data.



The user must discard the first received byte in the case where the UART clocks were disabled in low power mode and transitioned to active mode as a result of remote Tx start bit detection.

Figure 11-8. UART RS232 Design Example Diagram



11.5.1 Key UART Protection Design Points

- On the RS232 DB9 connector shown in the figure above, note that the "SHIELD" is NOT directly tied to the digital signal ground which is a typical design error. Not connecting the SHIELD to the digital ground ensures that an ESD discharge event does not infiltrate the digital ground system and disrupt normal application operation, which results in an MCU reset or component failure. Attach the shield to the chassis ground. If the chassis ground is not accessible, then connect through either:
 - 1k Ohms @ 100 MHz Ferrite Bead 1A, DCR = 0.15 Ohm for ESD protection only concerns.
 - Recommended:** A 10k fixed resistor adds the same ESD protection as the ferrite bead but with the additional benefit of ground loop current isolation between the remote system shield or case and the local digital ground in the event that the remote system did not follow good design practices. 10K is still low enough to shunt and attenuate the RF and EMI on the RS232 cable shield.
- The UART has the RS232 DB9 digital ground connector, pin 5, the ferrite bead, and the 10-ohm resistor. The ferrite bead protects against a possible ESD ground discharge event from the remote system, and the 10 ohm resistor is to limit potential ground loop currents (see [Ground Loops](#)), while not effecting signal VIL/VIH and VOL/VOH levels.
- Transient voltage suppressors on the UART signal lines entering and leaving the local system complete the protection

Note: It is a common belief that because a component vendor says their IC can withstand $\pm 15\text{V}$ that it already provides adequate protection on the I/O, but that is not the only requirement for external interface components and signals. Usually the $\pm 15\text{V}$ rating is for the IEC 61000-4-2 air discharge specification. This is fine for non-external interface signals, but does not cover the IEC 61000-4-2 ESD contact discharge with an $\pm 8\text{V}$ @ 30 amp peak current discharge requirement for equipment enclosure, external facing signals interfaces, ports, connectors, and cable hardware.

There is comprehensive information available on ESD, EMI, or EFT on Microchip web site that can be found in the document: [AN2587 - EMI, EMC, EFT, and ESD Circuit Design Consideration for 32-bit Microcontrollers](#), or on any of the 32-bit product web pages under the tab *Documentation > Application Notes*.

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11.6 USB



Important: All PIC32MX and PIC32MK device families do not support low-speed USB mode (see errata). Use Full-Speed mode instead.

Problem: 34: Why does a USB data transfer take longer than expected?

- When data packets are dropped due to CRC errors caused by timing or signal integrity issues the USB protocol allows continuous retries of the packets in all but Isochronous data transfers. This leads to long transfer times as the same data packets are retransmitted over and over again until the CRCs match, see *Cautions* in the next problem.

Problem: 35: Why will the USB DEVICE not enumerate?

Most USB issues are similar and come back to signal integrity and timing accuracy issues discussed in more detail below.

- On SAM products and some PIC32C products:



The output drivers for the DP/DM USB line interface must be fine-tuned with calibration values from production tests. The calibration values must be loaded by the user from the NVM Software Calibration Area into the USB Pad Calibration register (PADCAL) by the software, before enabling the USB, to achieve the specified accuracy.



For USB DEVICE only mode using the SOF clock recovery for the USB 48 MHz clock, the user must first Load the DFLLVAL.COARSE register prior to enabling the USB DEVICE from the "DFLL48M COARSE CAL" NVM Software Calibration Area Mapping. (Consult the Data Sheet. If there is no DFLL48M COARSE entry in the NVM Software Calibration Area Mapping there is a good chance that it is handled by the hardware.). For the SAMD21/D11/L21/L22 Product families, or any that use DFLL48M as the default startup oscillator, the user must load the calibration value manually by software.

Problem 36: USB connection has been lost.

- When USB transmission errors occur depending on the frequency of their incidence, the USB system software determines if and when a timeout occurs or how many retry attempts are allowed. When either of those thresholds are met the USB connection will be terminated.
- As per USB 2.0, any USB device can be classified as either low power (5V @ 100 mA) or high power (5 V @ 500 mA). Once connected, a USB device is allowed to draw only 100 mA current initially while enumerating and negotiating its power budget with the host. Based on the enumeration, the host will either raise the power delivery to 500 mA or continue at 100 mA. If the downstream device draws more power than either the host can

support, or more than its negotiated limit, the host will disconnect the downstream offending port. (This description does not include the new Battery Charging Spec BC 1.2 ECN to the USB 2.0 specification.)

Table 11-3. USB Modes and Data Rates Summary

USB Modes	Clock Accuracy	Data Rate
HS: High Speed	±0.05%	480Mb/s
FS: Full Speed	±0.25%	12 Mb/s
LS: Low Speed	±1.5%	1.5 Mb/s

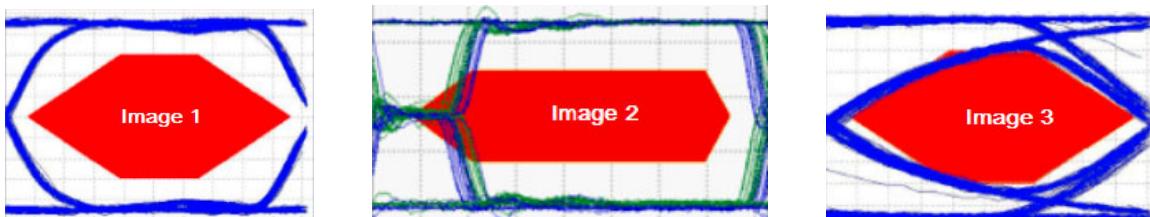
Table 11-4. USB Transfer Types and Error Retry Summary

USB Data Transfer Types	Auto Resend on CRC error	Use Cases
Control Transfer	YES	Used to configure the device (Enumeration)
Interrupt Transfer	YES	Used to send short, simple data like keyboard, mouse, touch pad, touchscreen, or game controller.
Bulk Transfer	YES	Used to transfer large amounts of data like files, pictures, printer data with 100% accuracy.
Isochronous Transfer	NO	Used for streaming video and audio.

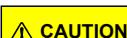
Note: CRC checks are done automatically by the USB hardware. At transmission, the packet CRC is encoded in the packet header. On packet reception the CRC of the data packet is calculated again and compared to the transmitted encoded CRC value in the packet.

- The two most common design issues related to USB are signal integrity due to impedance mismatches and timing violations. The following figure shows what is called a USB eye diagram. The area in RED represents a restricted area that a USB signal cannot intersect, or it will not be in compliance with the USB specifications. Such a violation can cause CRC errors and dropped packets.

Figure 11-9. USB EYE Diagram



- Image 1 represents a passing USB differential eye diagram with excellent timing, rise/fall times and impedance matching.
- Image 2 represents a timing issue associated usually with USB source clock accuracy and/or jitter issues.



Ensure that the combined MCU clock source plus any used PLL and/or DFLL used to supply the USB clock meet the clock accuracy requirements in the [USB Modes and Data Rates Summary](#) table listed above.



If using a PLL or DFLL to supply the USB clock, check the data sheet jitter spec if listed, or calculate using the formula provided in the data sheet to insure it meets the accuracy specifications again.

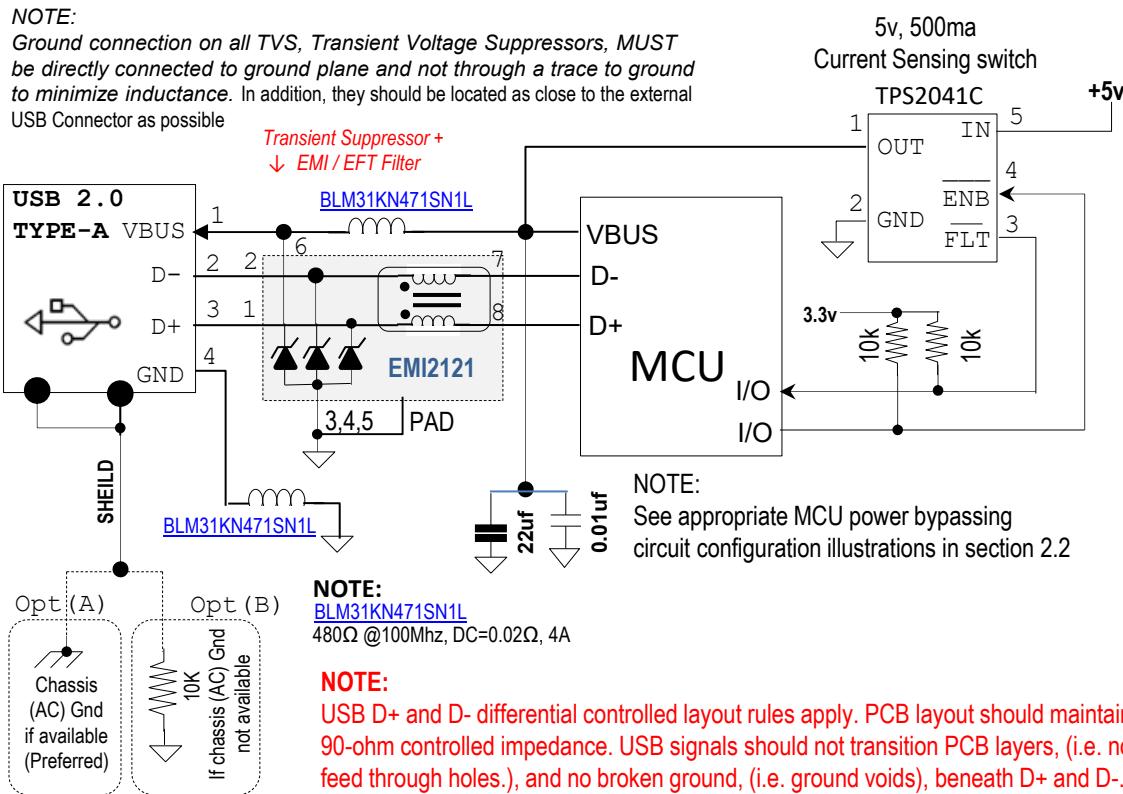
- Image 3 represents a typical impedance mismatch issue either due to PCB layout, component selection that is in contact with the D+ and D- signal, or the use of a non-certified USB cable

Table 11-5. USB PCB Layout Rules and Restrictions

1	Layout USB and USB differential traces first <i>maintaining differential 90-ohm impedance matching</i> on PCB layer 1, MCU component side, adjacent to ground plane layer.
2	D+ and D- PCB traces should not exceed: <ol style="list-style-type: none"> 1. USB High Speed = 3.5 inches, (88.9mm) 2. USB Full Speed = 4.5 inches, (114.3mm) 3. USB Low Speed = 6 inches, (152.4mm)
3	Ensure that D+ and D- traces have an <i>unbroken reference ground plane</i> with no ground gaps or voids beneath them.
4	Ensure that D+ and D- <i>trace lengths are identical</i> .
5	D+ and D- traces should <i>not have any PCB via's</i> , (i.e. feedthrough holes), or sharp corners or they will disrupt the impedance at frequency and cause reflections.
6	The USB connector shield <i>should not</i> be directly connected to the digital logic ground. Although differential signals offer good noise immunity, they are susceptible to ground loops that can create offsets on the signal level thresholds. A capacitor between the USB shield and logic ground is not a good design practice as it will conduct an ESD discharge directly into the MCU system. (See the USB design example illustrations on the pages that follow.)
7	If using protection components: <ol style="list-style-type: none"> 1. Locate these immediately close to the USB PCB connector and do not use stubs. Components should be surface mounted in-line with D+ and D- traces to maintain impedance matching and minimize reflections. If a stub is unavoidable, ensure it's less than 200mils. 2. High Speed & Full Speed, USB, protection component load should not exceed 1.5pF per signal.
8	D+/D- traces should not have any extra components to maintain signal integrity. For example, traces should not be routed to multiple USB connectors ideally.
9	Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC's that use or duplicate clock signals.

Note: See [Complete PCB Layout Guidelines](#) in the back of this document.

Figure 11-10. USB Host Design Example Diagram



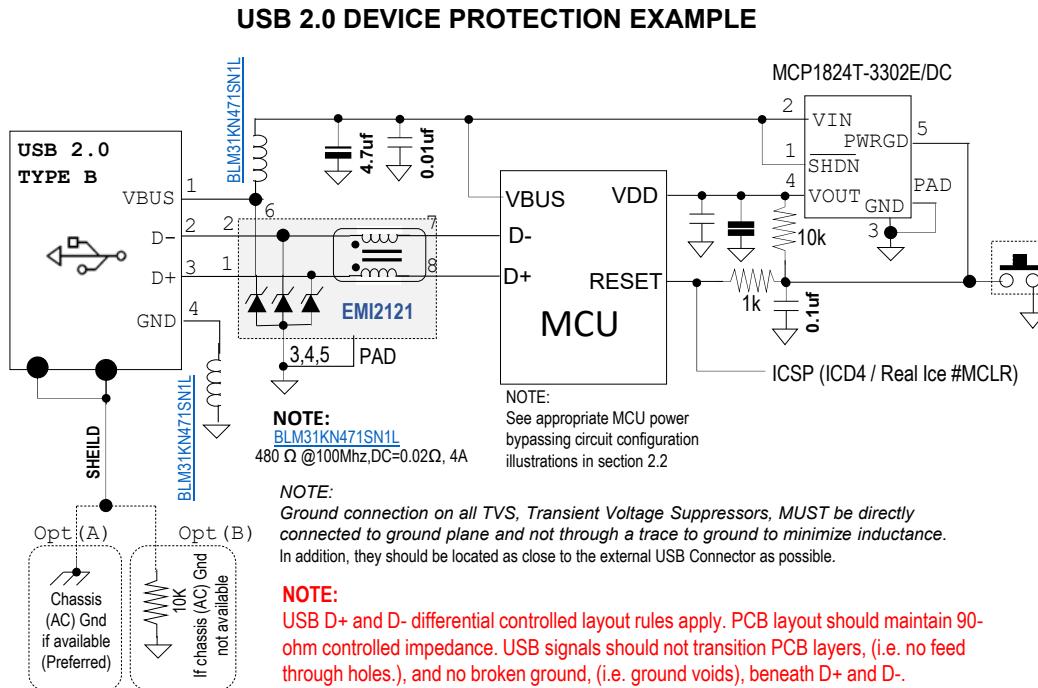
11.6.1 Key USB Host Design Points

- On the USB connector as shown in the figure above, note that the shield is not tied to the digital signal ground which is a typical design error. Connecting the shield to the digital ground ensures that an ESD discharge event does not infiltrate the digital ground system and disrupt normal application operation, which will result in an MCU reset or component failure. Attach the shield to the chassis ground. If the chassis ground is not accessible, then connect through either:
 - 1k Ohms @ 100 MHz Ferrite Bead 1A, DCR = 0.15 Ohm for ESD protection only concerns (i.e. **MI0805J102R-10**)
 - Recommended:** A 10k fixed resistor which adds not only ESD protection but a ground loop current isolation between the remote system shield or case and the local digital ground in case the remote system did not follow good design practices. The 10k is a low enough impedance for the shield, so that RF and EMI interference is effectively attenuated to maintain the USB cable shield effectiveness.
- On the USB connector, the digital ground, pin 4, and the ferrite bead to help protect against possible ESD ground discharge event from the remote system. The normal series resistor is in line with the ferrite on many other peripheral interfaces to limit potential ground loop currents. It is absent here due to the potentially large USB downstream power requirements.
- The transient voltage suppressors and 90Ω common mode choke should be located as close to the USB connector as possible. The common mode choke is only for conducted EMI isolation.
- The TPS2041C current limiting switch, TPS20xxx is available in 500 mA to 2 amp varieties in 0.5amp steps. Its purpose is to limit downstream VBUS loading to protect the 5V supply on a host system.

Note: There is comprehensive information available on ESD, EMI, or EFT on Microchip web site that can be found in the document: [AN2587 - EMI, EMC, EFT, and ESD Circuit Design Consideration for 32-bit Microcontrollers](#), or on any of the 32-bit product web pages under the tab *Documentation > Application Notes*.

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Figure 11-11. USB Device Design Example Diagram



11.6.2 Key USB Device Design Points

- On the USB connector in the figure above, note that the shield is not directly tied to the digital signal ground which is a typical design error. Not connecting the shield to digital ground is to ensure that an ESD discharge event does not infiltrate the digital ground system and disrupt normal application operation, generally resulting in an MCU reset or component failure. Attach the shield to chassis ground. If chassis ground is not accessible, then connect through either:
 - 1 k Ohms @ 100MHz Ferrite Bead 1A, DCR=0.15 Ohm for ESD protection only concerns, (i.e. [MI0805J102R-10](#)).
 - Recommended:** A 10k fixed resistor which adds not only ESD protection, but ground loop current isolation between the remote system shield / case and the local digital ground in the event that the remote system did not follow good design practices. The 10k is a low enough impedance for the shield so that RF and EMI interference is effectively attenuated to maintain the USB cable shield effectiveness.
 - On the USB connector, the digital ground, pin 4, and the ferrite bead help to protect against a possible ESD ground discharge event from the remote system. The normal series resistor is in line with the ferrite on many other peripheral interfaces to limit potential ground loop currents, but is absent here due to the potentially large USB downstream power requirements.
 - The transient voltage suppressors and the 90 Ω common mode choke should be located as close to the USB connector as possible. The common mode choke is only for conducted EMI isolation.
 - The MCP1824T 3.3vLDO is shown to illustrate how it can also be used as a reset supervisor to the MCU.
- Note:** The required 1k isolation resistor is a requirement for the ICSP.

Note: There is comprehensive information available on ESD / EMI / EFT on our web site that can be found in the document: [AN2587 - EMI, EMC, EFT, and ESD Circuit Design Consideration for 32-bit Microcontrollers](#), or on any of the 32bit product web pages under *Documentation Tab > Application Notes*.

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11.7 CAN FD

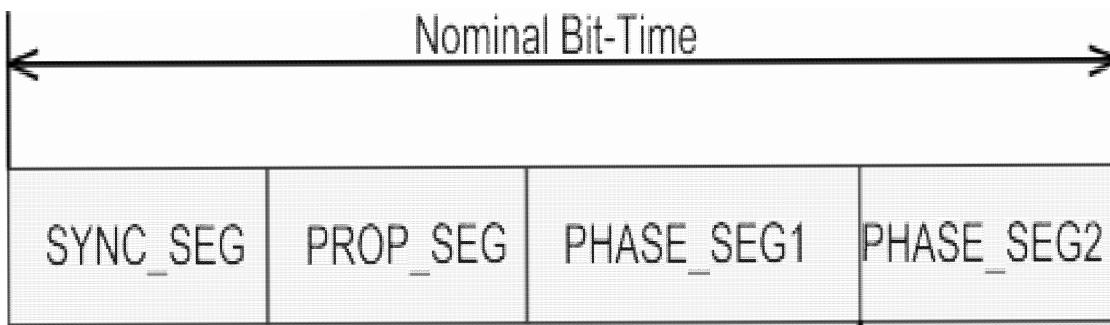
Problem 37: Why is the CAN sending message errors?

Problem 38: Why will the CAN not connect?

11.7.1 CAN FD Silicon Configuration Requirements

- The maximum data rate error for CAN /CAN FD is $\leq 1\%$.
- At least one CAN device must have a fixed CAN bit rate configured. If more than one CAN device has a fixed CAN bit rate configured, it must be the same bit rate for each of the fixed CAN bit rate devices on the network.
- Each CAN node ID must be unique in the CAN network.
- The CAN data rate is determined by:
 - CAN Time quantum (i.e. TQ) = ((Data Baud Rate Prescalar + 1) / FCAN)
 - Note:** The FCAN is the CAN module input clock frequency (Recommend 20 MHz, 40 MHz, or 80 MHz).
 - Bit Period = $(TQ * ((SYNC + (TSEG1 + 1) + (TSEG2 + 1))))$
 - CAN Bit Rate = $(1 / (((BRP + 1)) / FCAN) * (SYNC + (TSEG1 + 1) + (TSEG2 + 1))))$
OR Bit Rate = $1 / \text{Bit Period}$
 - $1\% \text{ Error} \geq [(\text{Bit Rate} - \text{User Desired bit rate}) / \text{Desired bit rate}] * 100$

Figure 11-12. CAN Nominal Bit Times Diagram



CAN PHASE SEGMENT RESTRICTION RULES

- (Prop Seg + Phase Seg1) \geq Phase Seg2.
- $8 \leq (\text{Sync (i.e. SJW)} + \text{Prop Seg} + \text{Phase Seg1} + \text{Phase Seg2}) \leq 40$.
- Sync (i.e. SJW) \leq Phase Seg 2.

Table 11-6. CAN FD Bit Time Registers

CAN FD SEGMENTS	SAM & PIC32C		PIC32MK		
SYNC SEGMENT	DBTP.DSJW		NBTP.DSJW	CFD1DBTCFG.SJW	
PROP SEGMENT			DBTP.DTSEG1		
PHASE SEG1		\geq	NBTP.DTSEG1	CFD1DBTCFG.TSEG1	\geq
PHASE SEG2	DBTP.DTSEG2		NBTP.DTSEG2	CFD1DBTCFG.TSEG2	
					CFD1NBTCFG.TSEG2

Notes:

- The bit rate configured for the CAN FD data phase through the SAM/PIC32C [DBTP Reg] or the PIC32MK [CFD1DBTCFG] must be higher or equal to the corresponding bit rate configured for the arbitration phase through the SAM/PIC32C [NBTP Reg] or the PIC32MK [CFD1NBTCFG Reg].
- The max CAN data rate error percentage must also consider the clock source inaccuracy + Jitter % error.
- Check all of the above for proper configuration for the actual data rate versus the expected data rate and % error.

⚠ CAUTION

On the PIC32MX/PIC32MZ/PIC32MK family never use the REFCLK as a source clock for any asynchronous peripheral (i.e., UART, CAN, ADC, and so on). The REFCLK produces a pseudo fractional clock frequency by cycle stealing to produce an average frequency, so over a given unit of time the number of clock pulses are not consistent. This means that the CAN bit times cannot be guaranteed.

11.7.2 CAN FD Hardware Requirements

- There are only two 120 Ohm bus termination resistors installed or configured in a CAN network *at the two physical end points of the CAN network between CAN_H and CAN_L*.
 - This can be checked easily by powering down all CAN devices and measuring the resistance in between the "CAN High" and "CAN Low" wires. The measured resistance must be approximately 60 Ohm (i.e., $R_{PARALLEL} = ((120 * 120) / (120 + 120)) = 60 \text{ ohm}$). Any value lower than 60 Ohm indicates that there are probably more than two 120 Ohm bus termination resistors present and this must be resolved.
 - The 120 ohm terminating resistor must be between CAN high and CAN low for it to work correctly.
 - A value larger than 60 Ohm typically indicates that there is at least one bus termination resistor missing, or the bus terminators have the wrong resistance value.
 - The proper placement of the two bus terminators of 120 Ohm at both end points of the network has to be checked visually.
 - The CAN GND in the network must have exactly one point connected to earth potential.
 - When using double shielded cables, the outer shield needs to be connected to the earth potential at one point. There must not be more than one connection to the chassis/earth ground in the network.
- There are two types of CAN cables. Unterminated and self-terminated cables. Terminated cables already have the 120-termination built into the cable assembly. Ensure that terminated cables are not mixed with CAN terminated circuit nodes. When connecting multiple CAN devices that already have termination, non-terminated cables are required.

Figure 11-13. Typical CAN Network

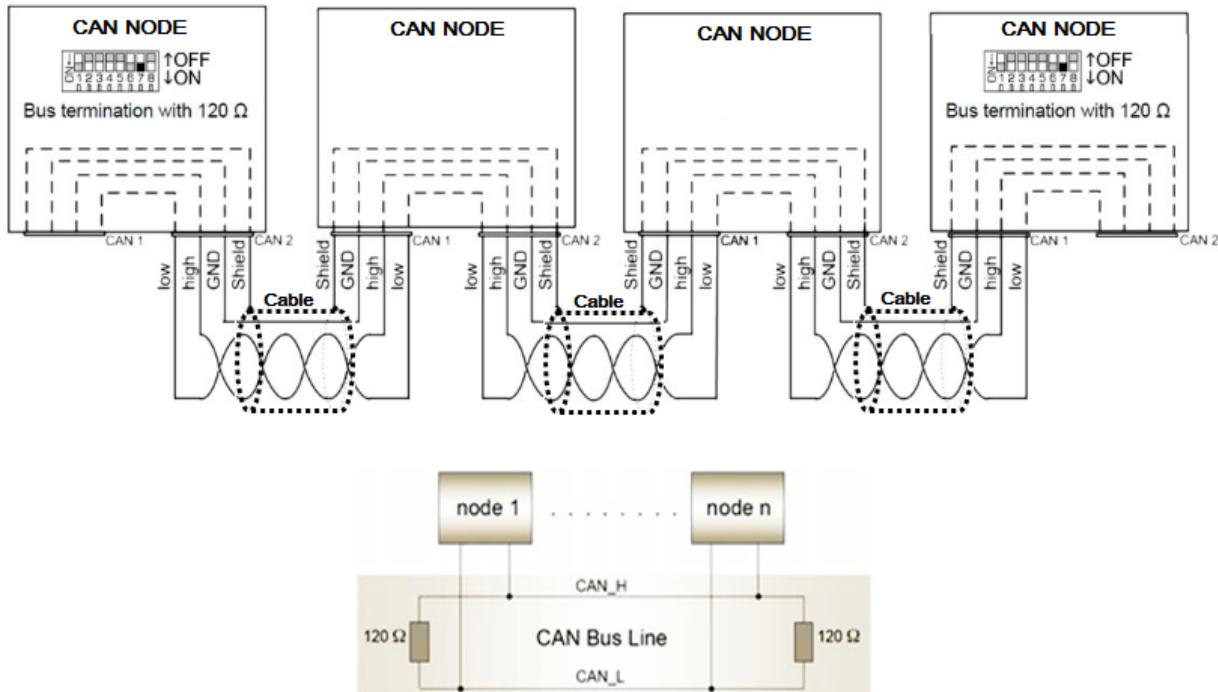
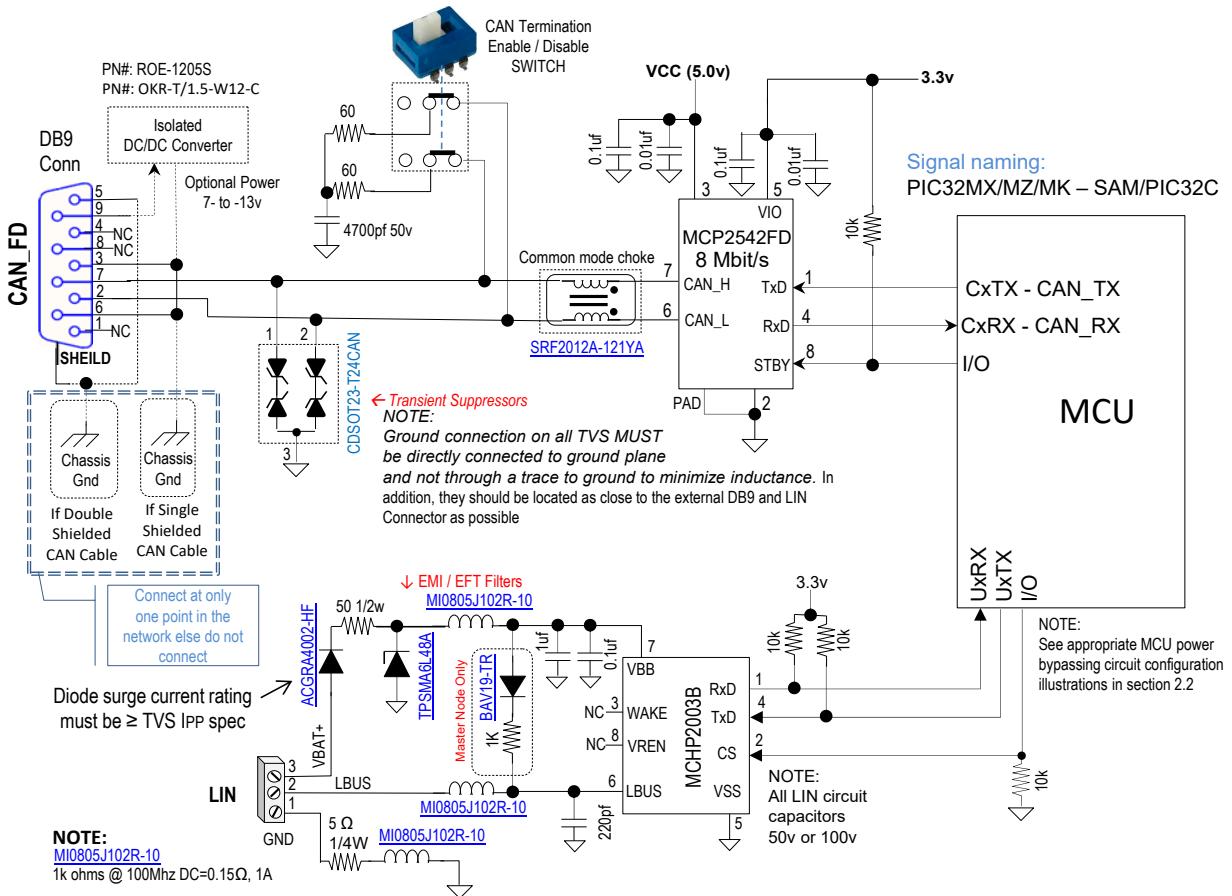


Figure 11-14. CAN FD / LIN Design Example Illustration



11.7.3 Key CAN FD/LIN Protection Design Points

- On the CAN DB9 connector in the figure above, the shield is not tied to the digital signal ground in CAN as it is in other peripherals. The CAN definition states that CAN communication is a two-wire differential protocol (CANH and CANL) bus. Dominant and recessive states of the bus are determined based upon the differential voltage read between the CANH and CANL regardless of the ground.
- The shield must only be connected to the chassis/earth ground at only one point in the CAN network.
- On some CAN networks the optional power is also routed to the cable pin 9. In the event a user intends to use that power source, beware that the line voltage fluctuations can be large. Also, the ground offset due to large currents over the entire network would require an isolated AC/DC converter to isolate the MCU power and ground from CAN cable power and ground.
- The 120-ohm termination resistors can only be at both ends on the CAN network, therefore the switch to enable or disable terminations depends on the user's PCB order and location in the CAN network.
- A common mode choke is recommended for data rates over 1 mbps.

Note: It is a common belief that because a component vendor says their IC can withstand 15 Kv that it already provides adequate protection on the I/O, but that is not the only requirement for external interface components and signals. Usually the 15 Kv rating is for the IEC 61000-4-2 air discharge specification. This is fine for non-external interface signals, but does not cover the IEC 61000-4-2 ESD contact discharge with an 8 Kv at 30 amp peak current discharge requirement for equipment enclosure, external facing signals interfaces, ports, connectors, and cable hardware.

There is comprehensive information available on ESD, EMI, and EFT on Microchip web site that can be found in the document: [AN2587 - EMI, EMC, EFT, and ESD Circuit Design Consideration for 32-bit Microcontrollers](#), or on any of the 32-bit product web pages under the tab *Documentation > Application Notes*.

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12. ADC

Problem 39: Why is the SAR ADC result 0v with input voltages up to 30 mv or more?

Problem 40: Why is the SAR ADC results not consistent and accurate?

ADC accuracy and repeatability are due to the possible error sources listed below:

- ADC silicon TUE, (i.e., total Unadjusted Error)
- System noise
- Reference voltage accuracy and drift over temperature and fab process
- User PCB circuit design implementations and IR drops
- ADCx BIASCOMP, BIASREFBUF, BIASR2R values that must be loaded from NVM Software Calibration Area Mapping Register

12.1 Typical SAM SAR ADC Total Unadjusted Error Sources (TUE)

- ADC Offset Error ⁽¹⁾
- ADC Gain Error ⁽¹⁾
- Quantization Error ⁽¹⁾
- Non-Linearity Error (INL, DNL) ⁽¹⁾

Notes:

1. These error sources are all documented in the data sheet and must be considered when assuming expectations of ADC accuracy. However, there are other factors as well that impact ADC accuracy that are not defined in the data sheet and some that are but might not be obvious. User PCB design and VREF accuracy can also affect the ADC accuracy, and a user must consider these for their application, which are typically overlooked. It is worth noting that SAMPCTRL.OFFCOMP (i.e., offset compensation), in most SAM SAR ADC's compensate for only the comparator inside the ADC, and that is in reference to the ADC's internal ground not the PCB system ground.

12.2 ADC Noise

Unique to the SAM and PIC32C families, I/O pins with mixed signal functions, (i.e. shared analog functions), are powered by VDDANA. (See data sheet GPIO Clusters map). This means that when a mixed signal pin is being used for a digital function and driving a load and toggling at even a moderate rate, the instantaneous on/off current sourced from VDDANA or sunk by GNDANA creates a ripple noise in the analog domain and additional challenges especially when trying to measure low-level signals in the double digit milli-volt range.

12.3 VREF Accuracy

- FS Lsb Error = (((VREF accuracy + Drift + System Noise) / VREF)/2n)
= ((2n * (VREF accuracy + Drift + System Noise)) / VREF)
- Actual worst-case ADC Result = (ADC Ideal Result / 2n) * FS Lsb Error
For example: SAM D5x/E5x Family SAR ADC Worst Case configuration over distribution of parts, process, voltage and temperature in LDO mode.

Where,

- Internal VREF = 1.2v ± 50 mv
- Internal VREF drift over Temperature 0.02%/°C over 25c-85c = 14 mv
- System noise LDO mode = ~50-75 mv, BUCK Mode ~200-300 mv
- 12-bit resolution
- ADC AIN0 input signal = 0.6V, (i.e., 50% scale of VREF)

$$\text{FS Lsb Error} = (2^n * (\text{VREF accuracy} + \text{VREF Drift} + \text{System Noise})) / \text{VREF}$$

$$= (4096 * (50 \text{ mv} + 14 \text{ mv} + 50 \text{ mv})) / 1.2\text{V}$$

$$= 389.12 \text{ LSB}$$

$$\text{ADC Result Error} = (\text{ADC Ideal Result of } 0.6\text{v input} / 2^n) * \text{FS Lsb Error}$$

$$= (2048/4096) * 389.12$$

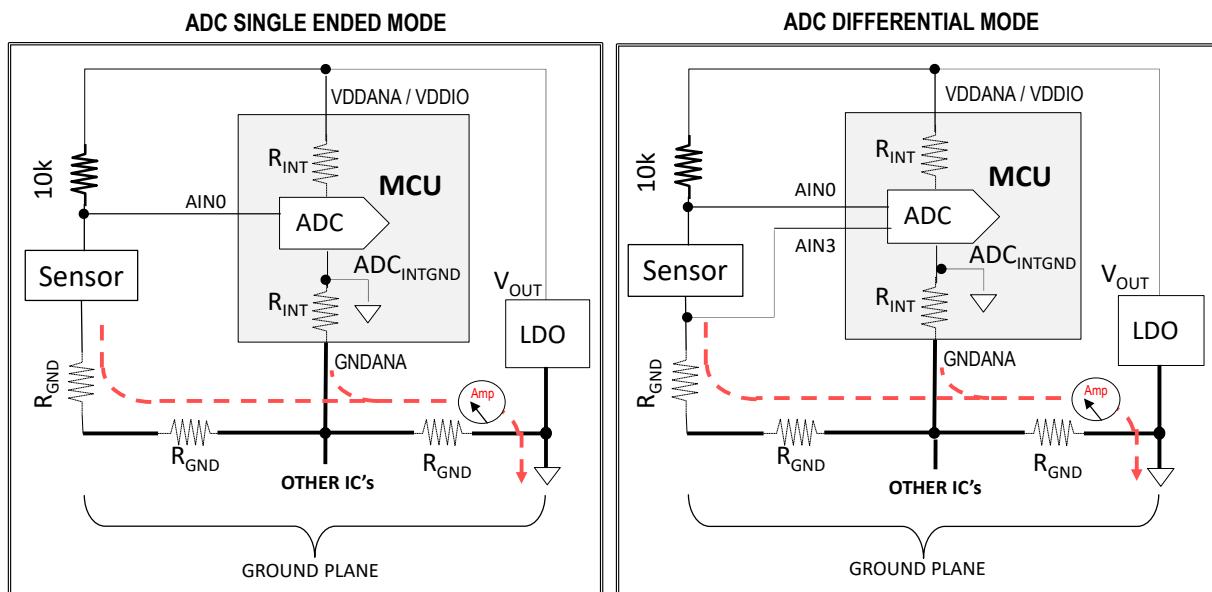
$$= 194.56 \text{ Lsb error or } 57 \text{ mv, (i.e., } 1 \text{ Lsb} = (\text{VREF}/2^n) = (1.2\text{v}/4096) = 293\mu\text{V/Lsb)}$$

12.4 Circuit IR Drop Errors

- Typical SAM/PIC32C SAR ADC (Referring to the figure below)
 - ADC IDD = 45-600 μA
 - R_{INT} = 45-50 Ω
 - V_{RINT} = (ADC IDD * R_{INT})

$$= 2.02 \text{ mv} \leq V_{RINT} \leq 30 \text{ mv}$$
- Typical Circuit Board Characteristics
 - Ground plane = ~0.06 ohms/inch (i.e., 0.06 ohms/25.4 mm)
 - Assumption: Ground plane W = 76.2 mm, L = 101.6 mm, ADC-to-Sensor ~50.8 mm
 - Ground current 200-1000 mA
 - Therefore: 25 mv \leq VRGND \leq 120 mv

Figure 12-1. ADC PCB Design Induced Errors, Single Ended Versus Differential Diagram



❑ R_{GND} = Distributed resistance along ground plane and connecting traces or wires to load Sensor.

❑ R_{INT} = Internal MCU resistance of metal runs and bond wires to analog power & ground pins

❑ ADC_{INTGND} = Local relative ground of the internal ADC module.

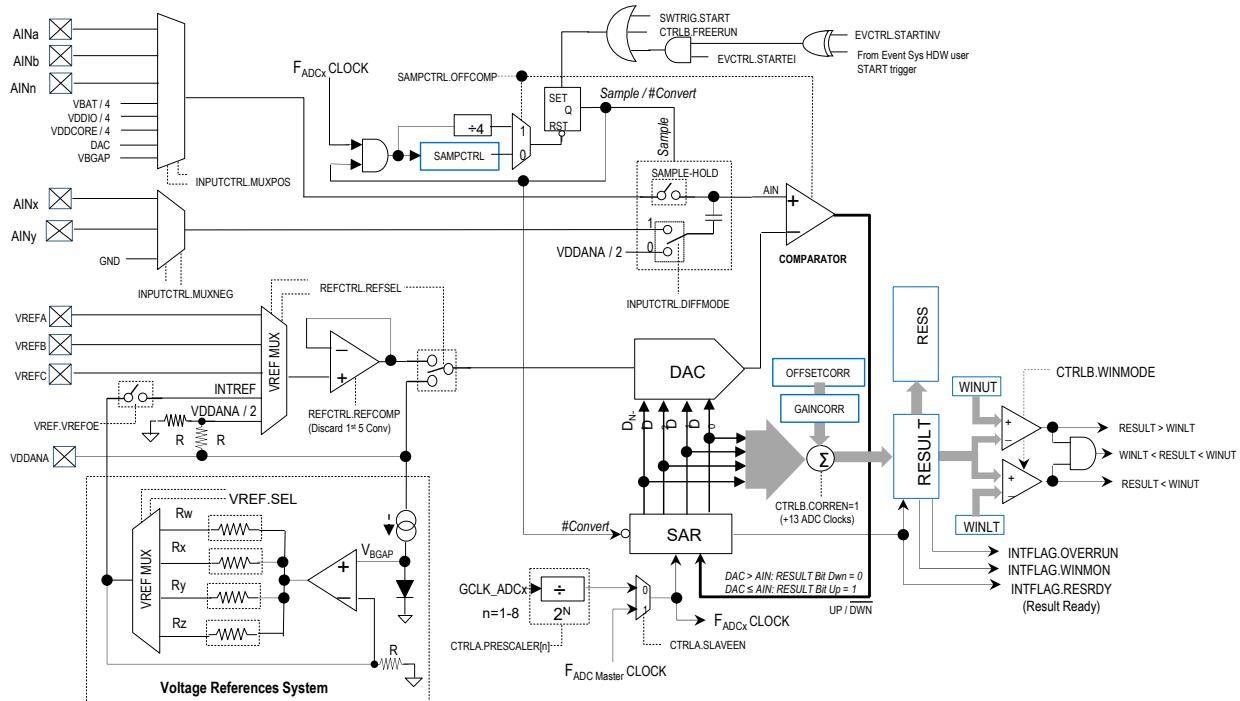
Notes:

- Referring to the ADC Single Ended mode figure above, the voltage as seen across the SENSOR by the ADC has an offset proportional to the ground current and ground resistance due to the ground IR drop (i.e., voltage difference), between the common sensor and the ADCINTGND. It is the sum of VRINT + VRGND and typically can induce an error of 30 mv to 50 mv or more. ADC single ended conversion results are relative to the analog input signal and the ADC internal ground, ADCINTGND.
- Be sure to load the ADCx BIASCOMP, BIASREFBUF, and BIASR2R values from the NVM Software Calibration Area Mapping Register to ensure the ADC is configured for optimum performance.
- When an application demands high resolution, consider using differential mode for improved accuracy. Unlike Single-Ended mode that measures an input relative to the internal ADC ground, and subject to the ground IR drops/offsets, differential mode measures the difference between two inputs irrespective of the ADC internal and external ground. If the ADC is in Differential mode, as shown in figure above, the input impedance of the ADC is very high, resulting in very little current flow into the analog input pins. In turn, the IR drop into the AINx pins is insignificant and the ground IR drop in the system is irrelevant. This allows for a much more accurate low-level signal sensor measurement.



Separate the analog and digital grounds and connect them only at the nearest point to the power source to minimize the ground IR drops.

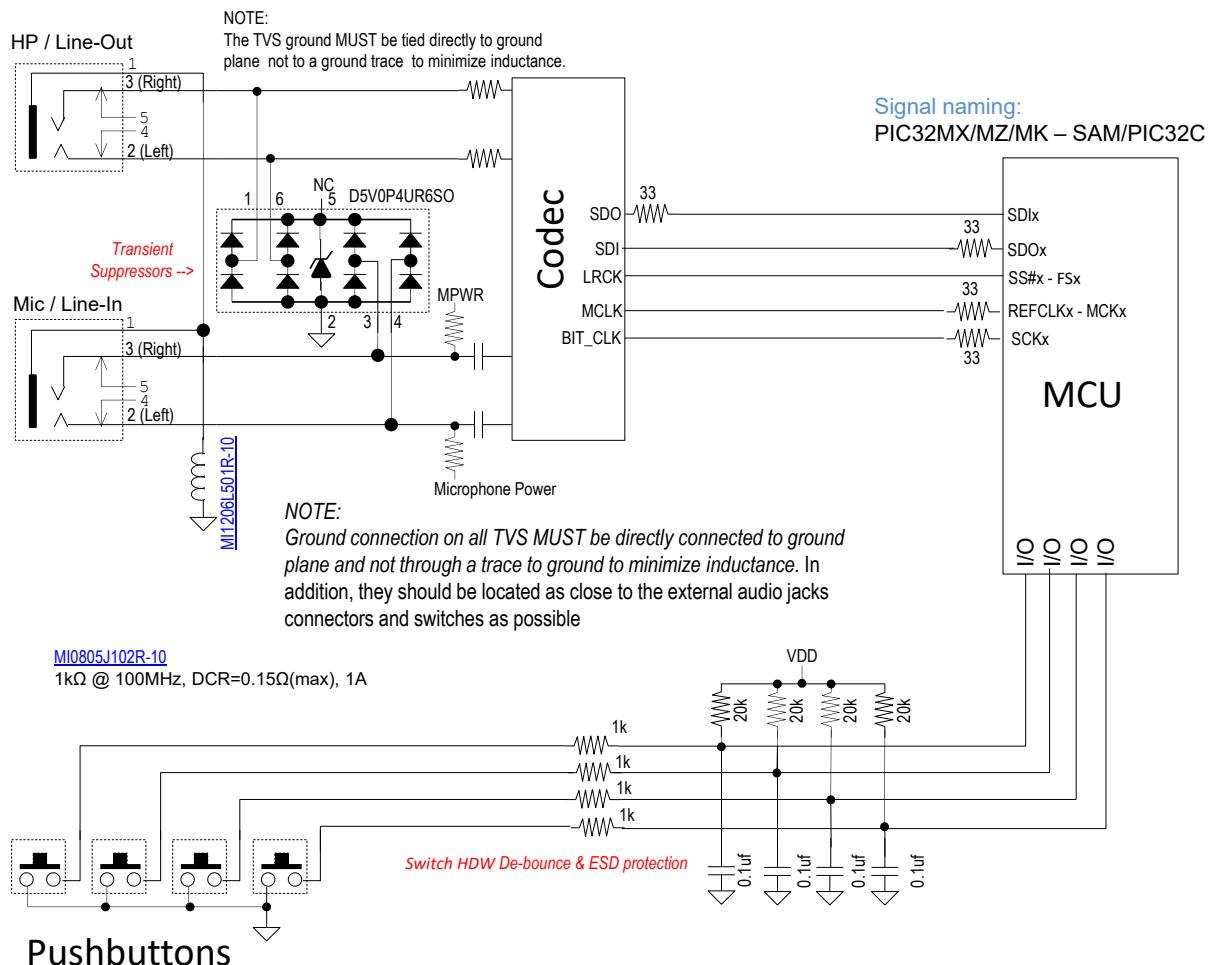
Figure 12-2. Typical SAM/PIC32CM SAR ADC Block Diagram



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13. I²S and Push Button Protection Illustration

Figure 13-1. I²S and Push Button Protection Design Diagram



13.1 Key I²S and Push Button Protection Design Points

- Push Button 1k series resistors and 0.1 μF caps form an ESD RC low-pass filter and a hardware push button denouncer
- ESD protection on ground, audio in, and audio out signals

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14. I²C

Problem 41: Why does the I²C com link not work?

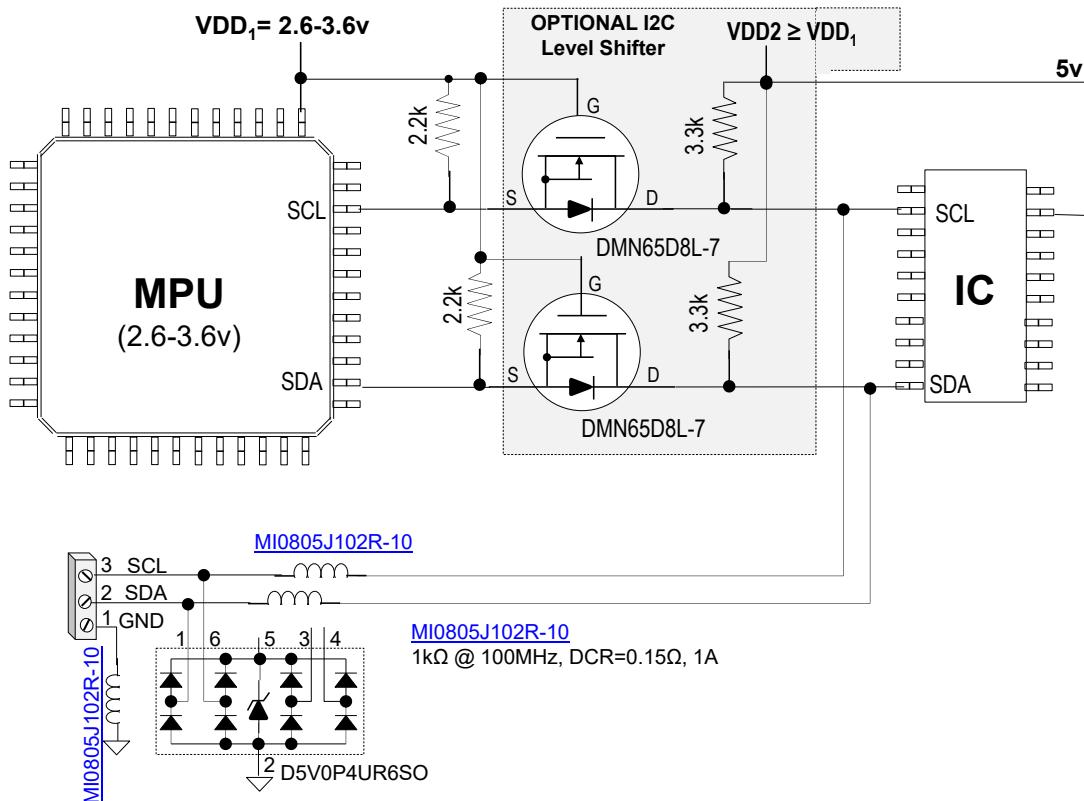
- The I²C default interface standard under the original I²C specification was 5V for TTL compatibility. All of the SAM legacy devices, except 5V VDDIO parts, do not have any 5V tolerant I/O pins and therefore are not compatible with anything other than 3.3V nominal signaling levels. On PIC32MX/PIC32MZ/ PIC32MK only select the I/O pins that are 5V tolerant and not all the I²C ports. For additional information, refer to the device-specific data sheet

Notes:

1. It is vital for reliability and proper signaling compatibility levels that the user ensure that any inter I²C communication and external cable I²C bus devices on the network are signal level compatible.
2. In most designs, only the master has pull up on what normally is open drain SDA and SCL. Every device has a certain SDA and SCL drive strength (i.e., IOL spec). If there are multiple I²C nodes on the network with pull-ups the user must ensure that the sum of all the pull-ups does not exceed any one node's ability to sink the sum of the network pull-up currents to ensure the proper I²C logic signal levels (i.e., VOL and VIL spec levels).
3. In a mixed signal level network, If the pull-up is on the 3.3v side then the resulting VOH may not meet one or more of the nodes on the high voltage sides logic high VIH spec. If the pull-ups are on a high voltage node then there is the possibility of injecting current into the lower voltage nodes IC's unless the user employs a level shifter.
4. If the users application provides the ability to connect to an external I²C bus network, often times the user's application cannot anticipate what equipment the external nodes I²C bus operating voltage levels are. In the case of non-5v tolerant SDA/SCL in nominal 3.3V MCU's, the user must consider a level shifter as depicted in the following figure to be compatible with respect to the external I²C node operating voltage levels.



Important: VDD2 must be \geq VDD1

Figure 14-1. I²C Protection Design Diagram

14.1 Key I²C Protection Design Points

There is an optional level shifter to interface 3.3V nominal logic to a 5V and higher nominal logic. When a low voltage I²C node signal level goes low, the FET is turned on pulling the higher voltage I²C bus low also. When the high voltage node side goes low, it forward biases the FET internal diode pulling the low voltage node side low minus the diode drop. When both sides are high the FET is off, and the FET internal diode is reverse biased.

- ESD protection on ground, SDA, and SCL

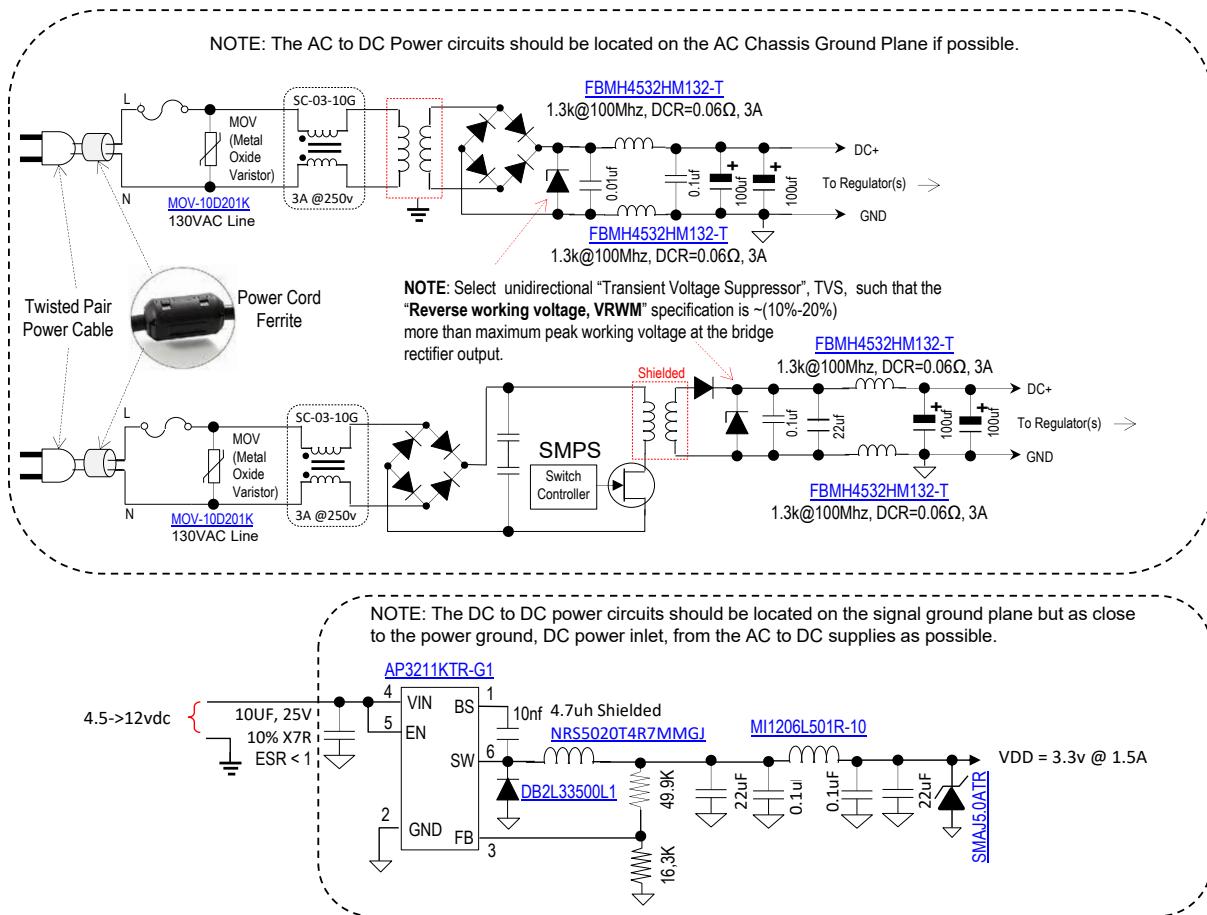
Table 14-1. Example I2C Level Shifter Logic Truth Table

3.3v Low Voltage side I ² C Node (MCU)	5v High voltage side I ² C node	3.3v I ² C node side	5v I ² C node side
0	0	0v	0v
1	0	0.3v	0v
0	1	0v	0v
1	1	3.3v	5v

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15. Inlet Power Protection Illustration

Figure 15-1. Power Source Input Protection Diagram



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16. Ethernet

Problem 42: An Ethernet connection cannot be established.

- Be certain the network side of the magnetics face the RJ45 connector and the device side of the magnetics face the LAN device.
- Differential pairs must be constructed as 100-ohm, controlled impedance pairs.
- Differential pairs must be the same length.
- Distance between LAN IC and magnetics must be ≤ 2.5 inches.
- Ensure that the [PCB layout rules](#) defined in the sections below are met.

16.1 Special Ethernet 10/100 Base-T Design Guidelines

16.1.1 Ethernet TX± and RX± Differential Pair Considerations

1. Both the RX± and TX± pairs must be routed as differential pairs. This includes the entire length of travel of the traces from the RJ45 connector to the LAN device.
2. the RX± and TX± differential pairs should be routed as close together as possible. Typically, when beginning the impedance calculation, the smallest trace space (4 – 5 mils) is selected. The trace width is then adjusted to achieve the necessary 100-ohm impedance.
3. Differential pairs should be constructed as 100-ohm, controlled impedance pairs.
4. Designs employing common mode chokes for EMI isolation must be 100ohm.
5. Differential pairs should be routed away from all other traces. Try to keep all other high-speed traces at least . 300" away from the Ethernet front end.
6. Each trace of the differential pair should be matched in length. The matched lengths of each positive and negative pair should be within 50 mils of each other.
7. The differential pairs should be as short in length as possible.
8. The use of vias is not recommended. If vias are used, keep to a minimum and always match vias so the differential pairs are balanced.
9. Layer changes are also not recommended. Keep the differential pairs referenced to the same power/ground plane whenever possible.
10. For optimum immunity, route Transmit pairs and Receive pairs as far away from each other as possible.
11. Always reference any Transmit terminations to the same reference plane that the Transmit routes are referenced to. Likewise, always reference any Receive terminations to the same reference plane that the Receive routes are referenced to.
12. Precedence should be given to the differential pair routing. Terminations must be added after the routing is determined. The terminations should simply be “dropped” onto the differential routing.
13. All resistive terminations in the Ethernet front end should have values with 1.0% tolerances.
14. All capacitive terminations in the Ethernet front end should have tight tolerances and high-quality dielectrics (NPO).
15. For optimum separation, experimentation can be explored with inserting a ground plane island between the Transmit pair and the Receive pair. A separation from this ground plane from any of the traces of 3 – 5 times the dielectric distance should be maintained.
16. This same technique can be used to separate different Ethernet ports if port cross talk is an issue. A ground plane can be inserted between Ethernet channels. The separation space between the two channels must be as wide as possible. Again, a separation from this ground plane from any of the traces of 3 to 5 times the dielectric distance must be maintained.

16.1.2 Unused Ethernet Cable Pairs Considerations

1. The unused cable pairs (pins 4, 5, 7, and 8 on the RJ45 connector) must be properly terminated for common mode considerations. These terminations must be routed with heavy, short traces and as close as possible to the RJ45 connector.

-
2. If not using an RJ45 connector with internal termination for unused cable pairs then terminate with 75-ohm resistors to a proper chassis ground plane through a high voltage (2KV) capacitor.

16.1.3 Ethernet RJ45 Connector Considerations

1. A shielded, metal enclosed RJ45 connector is recommended.
2. The metal shield must be connected to a proper chassis ground plane.
3. Another ESD enhancement may be the use of an RJ45 connector with surface mount contacts. This may simplify routing and allow greater separation in the Ethernet front end to enhance ESD/susceptibility performance.

16.1.4 Ethernet Magnetics Considerations

1. Many different types and configurations of magnetics available for use with any particular LAN device. Different packages, orientations, and sizes are all factors that need to be considered when selecting magnetics.

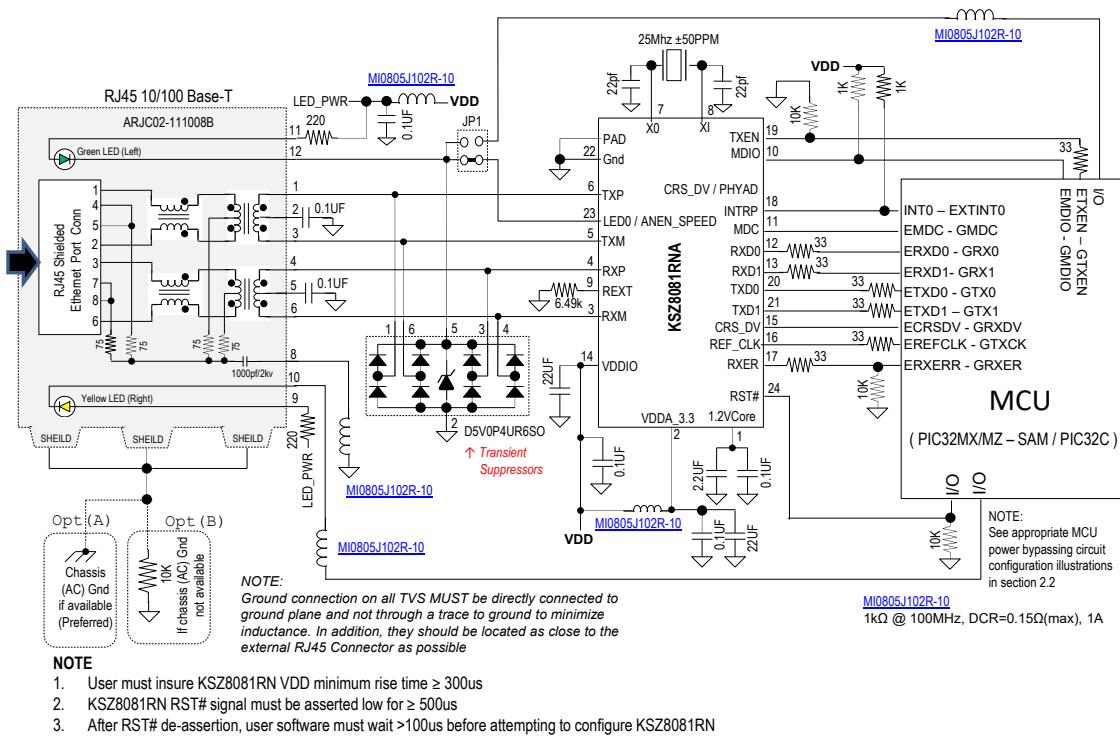
Table 16-1. Ethernet Magnetics Selection Criteria

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	-
Open-circuit inductance (minimum)	350 μ H	100 mV, 100 kHz, 8 mA
Insertion loss (typical)	-1.1dB	100 kHz to 100 MHz
HIPOT (minimum)	1500 Vrms	-

2. The magnetics must be placed as close as possible to the RJ45 connector.
3. Depending on which style of magnetics is selected (North/South or East/West), this will determine the orientation of the magnetics as related to the RJ45 connector. Be certain the network side of the magnetics face the RJ45 connector and the device side of the magnetics face the LAN device. This will ensure that the high voltage barrier through the middle of the magnetics can be correctly routed and designed on the PCB. Ideally, the LAN device should then be placed as close as possible to the magnetics. If this is not possible, the RJ45 connector and magnetics must remain in close proximity. The LAN device then can be located somewhat remotely from the RJ45 or magnetics area.

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Figure 16-1. Ethernet RMII Design Example Diagram



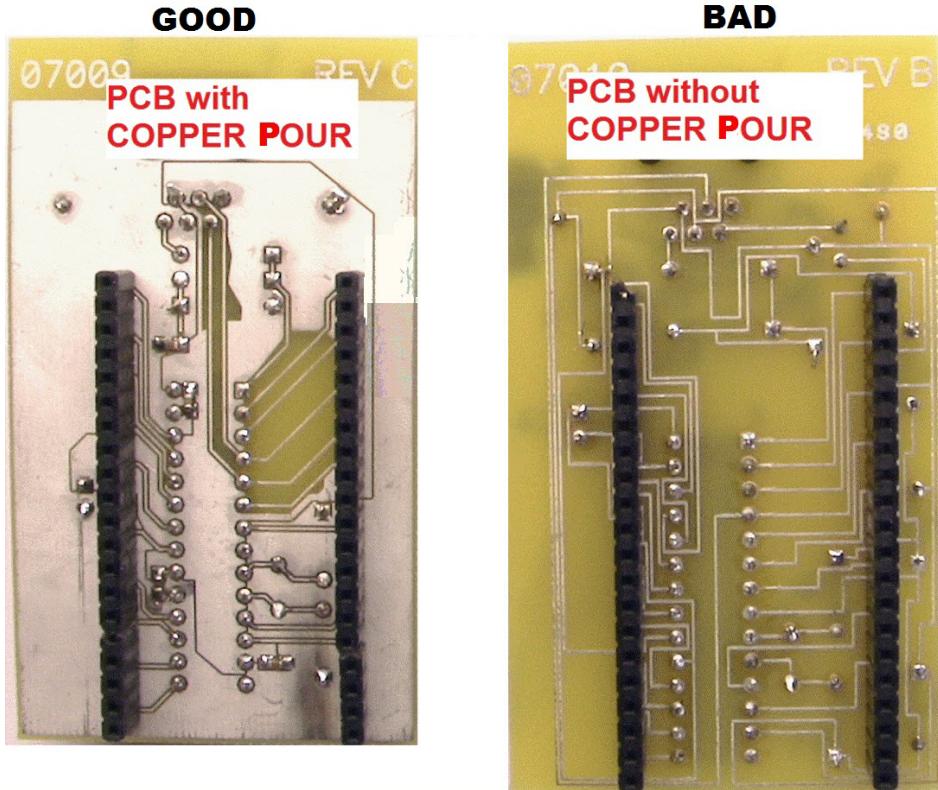
16.1.5 Key Ethernet Protection Design Points

- The use of ferrites on the Ethernet PHY on the magnetics and the LED indicators in the PHY.
- Ideally the Ethernet PHY shield must be connected to the chassis/earth ground if available. If the chassis/earth ground is not available, then through a 10k resistor to logic ground. This is for ESD and ground loop isolation from the MCU logic ground.
- Differential TX and RX pairs must be constructed as 100-ohm, controlled impedance pairs from MCU to ethernet controller, and ethernet controller to PHY. The signal distance between the components ≤ 2.5 inches.

17. Comprehensive PCB Layout Guidelines and Recommendations

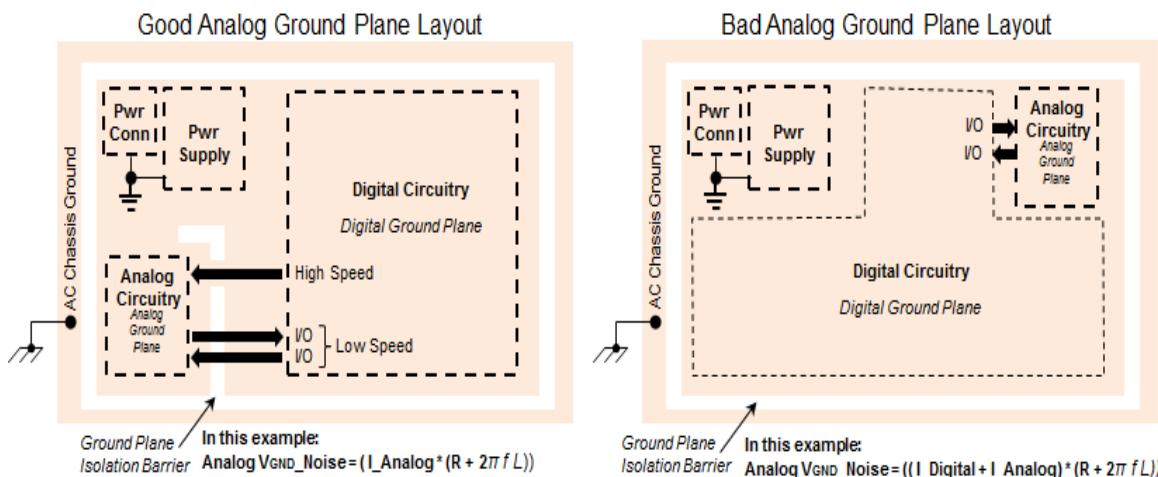
1. Layout differential and high-speed traces first, maintaining differential impedance matching on PCB layer 1 adjacent to ground plane layer.
2. Ensure that all clock and high-speed signal traces must have an unbroken reference ground plane with no gaps or voids beneath them.
3. Copper pour all voids on signal layers with signal ground.

Figure 17-1. Copper Ground Pour in PCB Voids



4. Use separate digital and analog grounds when appropriate and do not connect the ground planes together except at power ground (i.e., closest to the respective input power regulator).

Figure 17-2. Analog Versus Digital Ground Layout Placement

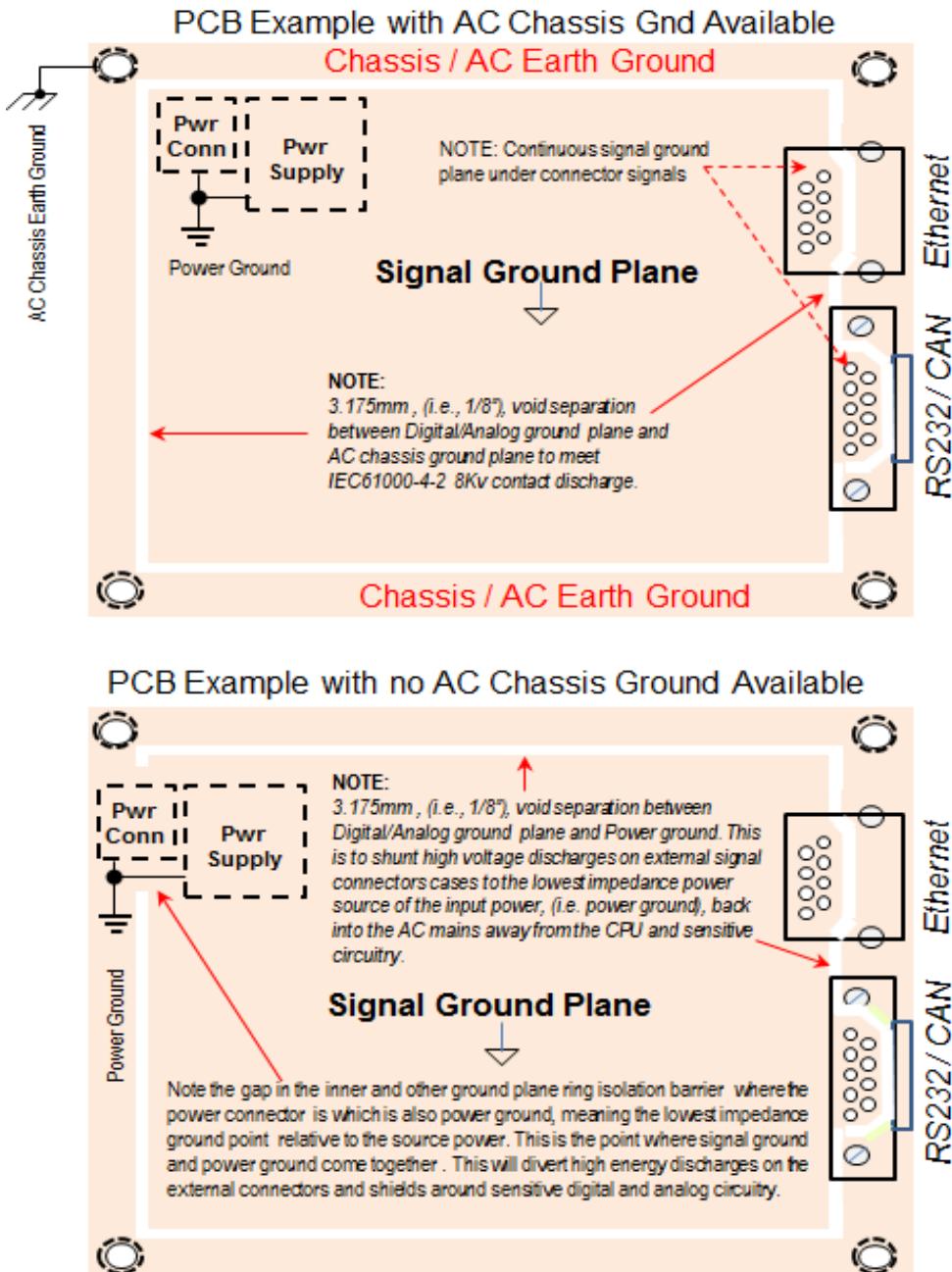


Comprehensive PCB Layout Guidelines and Recommenda...

Digital noise and current are generally much larger than that of the analog circuitry. As a result, choose a layout strategy where the analog ground current has a separate and not additive digital ground current and noise as depicted above. Use ground isolation barriers to steer and contain digital noise/current away from the analog circuitry. Remember that high frequency noise will seek the path of least inductance which is generally the shortest distance on a ground plane. Most analog control signals from the digital domain are low and medium speed so routing over ground voids in those instances is acceptable. In cases where high speed signals from digital to analog domain is required, such as the audio codec master clock, do not route over ground voids. Instead, use an isolation barrier bridge as shown in the 1st example as well as a termination resistor at the clock source of ~50 ohms.

5. Do not run sensitive analogue signals in parallel over or near fast digital transit signals. If necessary, then insure they cross at right angles to minimize the capacitive cross section of the traces.
6. The lengths of traces carrying high-speed digital signals or clocks should be minimized. High-speed digital signals and clocks are often the strongest noise sources. The longer these traces are, the more opportunities there will be to couple energy away from these traces. Remember loop area is generally more important than trace length. Make sure that there is a good high-frequency current return path very near each trace.
7. The lengths of traces attached directly to the connectors (I/O traces) must be minimized. Traces attached directly to the connectors are likely paths for EMC, EMI, and EFT energy to be coupled on or off the board. The use of TVS and ferrite beads and/or common mode chokes as required are recommended on all external connector I/O pins. Refer to schematic recommended design protection examples.
8. In general, it is a good PCB design rule to not run any traces in between any surface mount pads (resistors, capacitors, ferrite beads, etc).
9. PCB traces must be designed with the proper width for the amount of current they are expected to supply. The use of mini planes in a local area on either the top or bottom layers will ensure the proper current supply.
10. All component leads to any power plane or ground plane should be as short as possible. The best solutions are plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections must be less than 5 – 10 mils in length. Trace connections must be as wide as possible to lower inductance. This will include any power ferrite beads feeding power planes, fuses feeding power planes, and so on.
11. Signals with high-frequency content should not be routed beneath components used for board I/O. Traces routed under a component can capacitive or inductively couple energy to that component.
12. All connectors when possible should be located on one edge or on one corner of a board. Connectors represent the most efficient EMC/EMI antenna parts in most designs. Locating them on the same edge of the board makes it much easier to control the common-mode voltage that may drive one connector relative to another.

Figure 17-3. Grounding Recommendations for External Connectors



13. In applications where the AC chassis ground is available, it is strongly recommended that the digital signal ground and AC chassis ground NOT be connected and are separated by at least 3.175 mm (i.e., 0.125 inches), for the 11-12 KV spark gap isolation to meet IEC61000-4-2 level-4 ±8 KV contact discharge. Peripherals, such as USB, Ethernet, SD memory card holders, RS232, and CAN, the connector cases are electrically isolated from the signal ground. The case should be connected to the AC chassis ground whenever available (i.e., Earth Ground), to shunt the high voltage discharges to the earth ground harmlessly and not into the digital or analog ground circuitry.

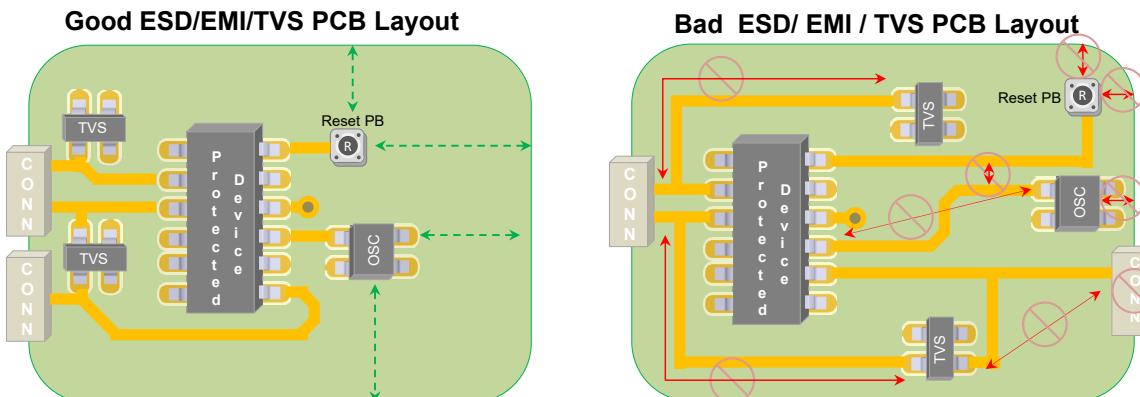
Note: In the figures the ground plane is always continuous under all the high-speed signal connections of the peripheral connector, but the connector case is isolated to the outer AC chassis plane.

Note: Not all connectors like audio metal input/output jack cases are isolated. They are in fact the signal ground. In situations like that they must not be mounted to an isolated AC chassis ground, but instead to the digital/analog ground as appropriate using a ferrite bead (see audio circuit design protection example). The user must determine for the external peripheral connector in use if it has an isolated or non-isolated case to signal ground or not. For isolated connectors, connect only the connector case to the AC chassis ground, otherwise connect to signal ground through an appropriate ferrite bead.

On the second example where there is no AC chassis ground (i.e. earth ground) available, the best strategy is to still have an isolation barrier and join the inner and other planes at the lowest impedance point in the circuit relative to the power source at the power inlet and regulator (otherwise called power ground). This will divert high energy discharges on the external connectors and shields around sensitive digital and analog circuitry to be dissipated through the power source and coupled back into the AC mains.

14. No high-speed circuitry should be located between I/O connectors. Even if two connectors are on the same edge of the board, high-speed circuitry located between them can induce enough common-mode voltage to drive one connector relative to the other resulting in significant radiated emissions.
15. Critical signal or clock traces when possible should be buried between power/ground planes. Routing a trace on a layer between two solid planes does an excellent job of containing the fields from these traces and prevents unwanted coupling.
16. Select active digital components that have maximum acceptable off-chip transition times. If the transition times of a digital waveform are faster than they need to be, the power in the upper harmonics can be much higher than necessary. If the transition times of the logic employed are faster than they need to be, they can usually be slowed using series resistors or ferrites.
17. All off-board communication from a single device should be routed through the same connector. Many components (especially large VLSI devices) generate a significant amount of common-mode noise between different I/O pins. If one of these devices is connected to more than one connector, this common-mode noise will potentially drive a good antenna (The device will also be more susceptible to radiated noise brought in on this antenna).
18. Locate Transient Voltage Suppressors (TVS) as close to external signal connectors as possible with the TVS ground connecting directly to the ground plane. Avoid ground trace connections.
19. High-speed or susceptible analog or digital traces must be routed at least 2X from the board edge, where 'X' is the distance between the trace and its return current path. The electric and magnetic field lines associated with traces very near the edge of a board are less well contained. Crosstalk and coupling to and from antennas tend to be greater from these traces and makes them more susceptible to ESD, EMI, and EFT events.

Figure 17-4. Printed Circuit Board Layout Examples



20. Differential signal trace pairs must be routed together and maintain the same distance from any solid planes. Differential signals are less susceptible to noise and less likely to generate radiated emissions if they are balanced (i.e., If they have the same length and maintain the same impedance relative to other conductors).
21. All power (for example, voltage) planes that are referenced to the same power return (for example, ground) plane, must be routed on the same layer. For example, if a board employs three voltages: 3.3 volts, 3.3 volts analogue, and 1.8 volts, then it is generally desirable to minimize the high-frequency coupling between these planes. Putting the voltage planes on the same layer will ensure that there is no overlap. It will also help to

- promote an efficient layout, because the active devices are unlikely to require two different voltages at any one position on the board.
- 22. The separation between any two power planes on a given layer should be at least 3 mm, (i.e., 11Kv isolation). If two planes get too close to each other on the same layer, significant high-frequency coupling may occur. Under adverse conditions, arcing or shorts may also be a problem if the planes are too closely spaced.
 - 23. On a board with power and ground planes, no traces should be used to connect to power or ground. Connections should be made using a via adjacent to the power or ground pad of the component. Traces on a connection to a plane located on a different layer take up space and add inductance to the connection. If high-frequency impedance is an issue (as it is with power bus decoupling connections), this inductance can significantly degrade the performance of the connection.
 - 24. If the design has more than one ground plane layer, then any connection to ground at a given position should be made to all the ground layers at that position. The overall guiding principle here is that high-frequency currents will take the most beneficial (lowest inductance) path if allowed to. Do not try to direct the flow of these currents by only connecting to specific planes.
 - 25. Ideally there should be no gaps or slots in the ground plane unless user has sensitive analog logic they are attempting to isolate (refer to [Analog Versus Digital Ground Layout Placement](#)). It's usually best to have a solid ground (signal return) plane and a layer devoted to this plane. Any additional power or signal current returns that must be DC isolated from the ground plane should be routed on layers other than the layer devoted to the ground plane.
 - 26. Be certain to review the entire PCB design for any high-speed signal traces crossing over any reference plane cuts. This will more than likely create an EMC occurrence. Avoid this.
 - 27. All power or ground conductors on the board that contact (or couple to) the chassis, cables or other good "antenna parts" must be bonded together at high frequencies. Unanticipated voltages between different conductors both nominally called ground are a primary source of radiated emission and susceptibility problems.

17.1 PCB Bypassing

- 1. Bypass capacitors must be placed near all power entry points on the PCB. These caps will keep unwanted high-frequency noise from entering the design; the noise will simply be shunted to the ground.
- 2. Bypass capacitors must be utilized on all IC power supply connections and all voltage regulators in the design.
- 3. All bypass capacitor leads should be as short as possible. The best solutions are plane connection vias inside the capacitor surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5- 10 mils in length. Trace connections must be as wide as possible to lower inductance.
- 4. IC decoupling capacitors and ferrite beads should be placed as close to the IC power pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. Ideally there should be two bypass caps 0.1 μ F and 0.001 μ F in parallel. Run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing the PCB trace inductance.
- 5. The use of a bulk capacitors distributed over the area of the power plane in the design is recommended to improve the power supply stability particularly in the area of large current consumption devices. Typical values range from 4.7 μ F to 47 μ F.

17.2 PCB Layer Strategy

- 1. 4-Layer PCB Example:
 - Layer 1 component + signal side (short traces)
 - Layer 2 ground plane
 - Layer 3 power plane
 - Layer 4 signal

Note: It is strongly recommended for all high-speed Ethernet LAN designs and minimum requirements to meet most EMC, EMI, and EFT requirements.

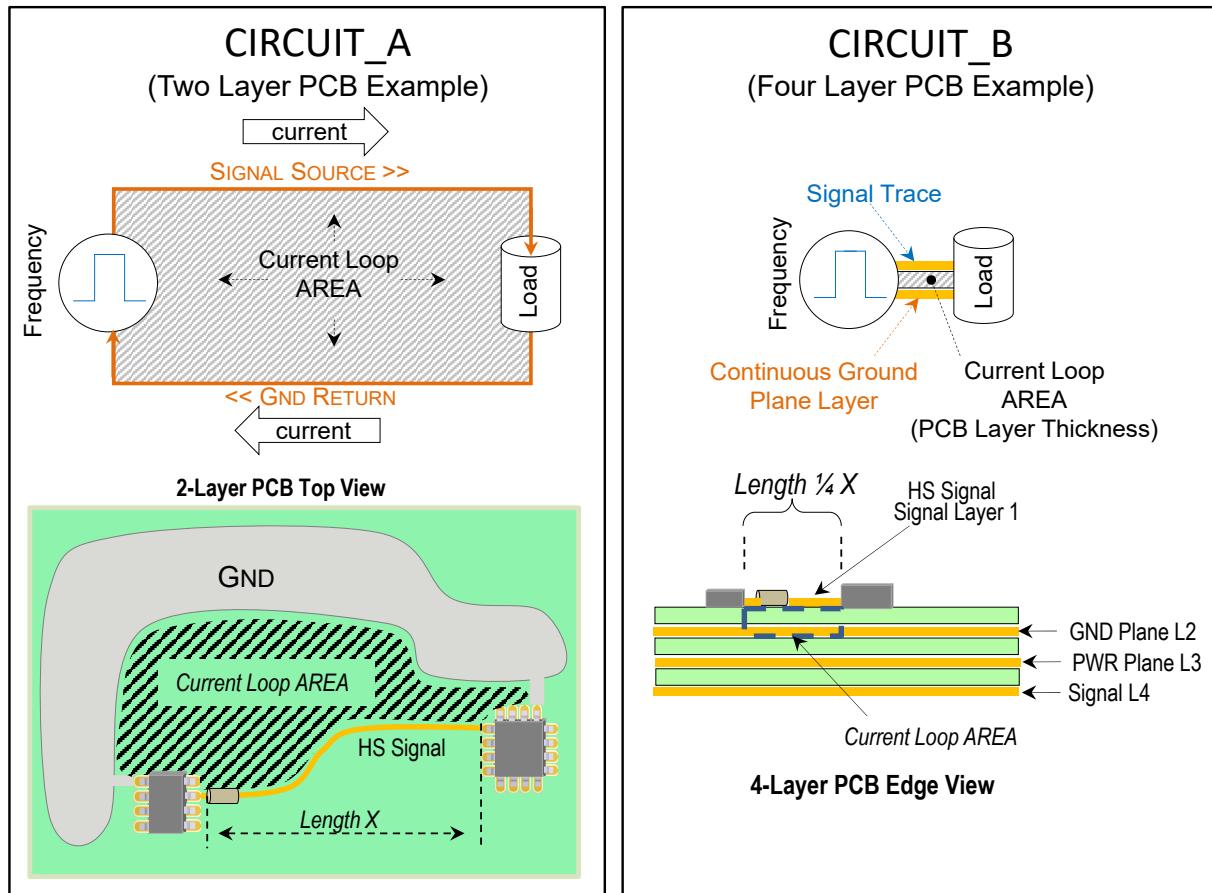
2. 6-Layer PCB Example:

- Layer 1 component + signal side (short traces)
- Layer 2 ground plane
- Layer 3 signal
- Layer 4 signal
- Layer 5 power plane
- Layer 6 signal

Note: Layer 1 on either 4-layer or 6-layer PCB's is considered the prime layer for critical routes and components because of the solid digital ground plane directly beneath it and Layer 1 also requires no vias to connect components located on Layer 1.

3. All PCB traces (especially high-speed and critical signal traces) must be routed on Layer 1 next to the solid, contiguous ground plane layer. These traces must have a continuous reference plane for their entire length of travel. This will help ensure optimum signal integrity and EMC performance.
4. The implementation of an Ethernet chassis ground plane separate from the digital ground plane is required.
5. Avoid creating current loops in the PCB design and the system design. In order to facilitate routing and minimize signal cross talk issues, adjacent layers in a multi-layer design should be routed orthogonal. Current loops create excellent antennas and make the circuit very susceptible to picking up noise and radiated EMI. The larger the current loop, the bigger the antenna, and the more noise it attracts. Poor PCB designs that unintentionally create current ground loops are most common on 2-layer PCB designs. For high speed signals these are one of the biggest issues leading to data corruption.

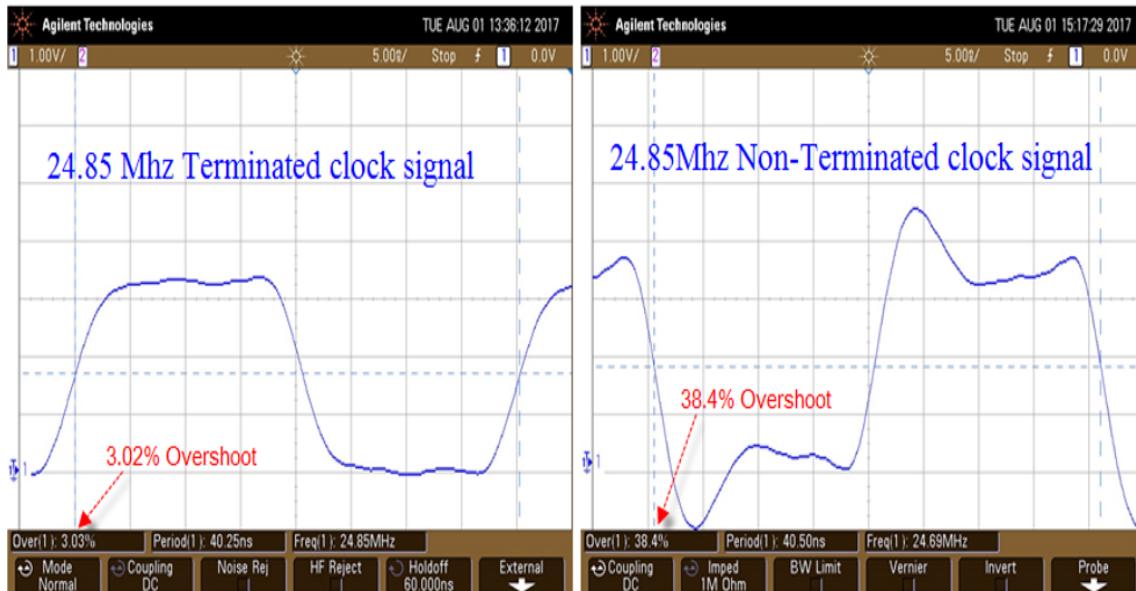
Figure 17-5. Current Loops in the PCB Design Diagram



17.3 PCB Signal Integrity Concerns

- Provide resistor terminations for all high-speed switching signals and clock lines >15 MHz on the PCB. Locate these terminations on the driver side of the trace. The exception is high speed silicon *impedance controlled* differential signal,s such as USB that do not require resistor termination because the drivers themselves have guaranteed output impedance by specification.
For bi-directional signals, place a series resistor at the output of any output driver on the bus.

Figure 17-6. High Speed Signal Termination Scope Plot Illustration



There are two methods to determine the required termination resistor values.

Step 1: Calculate the PCB line impedance by entering the PCB trace information into an impedance calculator:

<https://www.eeweb.com/tools/microstrip-impedance> = Trace Impedance

Table 17-1. PCB Trace Impedance Calculation Example

Trace Width	PCB Height between layers	Trace Thickness	PCB Substrate Dielectric FR4 Bd	Trace Impedance
0.175mm	113µm	1.41 mils (1 oz Cu)	4	54.6 Ohms

Table 17-2. Typical Trace Thicknesses Based on Copper Weight

Cu weight	Thickness in Mils
1 oz	1.4 mils
2 oz	2.8 mils
3 oz	4.2 mils
4 oz	5.6 mils

Step 2: Once the trace impedance is calculated by entering the PCB trace information then:

Method 1 of 2: (Ball Park method)

PCB signal series termination resistor(s) value = $\{[(VDD-VOH(\min)) / IOH(\max)] - \text{Trace Impedance}\}$
 $= \{(3.3-2.4) / 10 \text{ mA}\} - 54.6 \text{ ohms}\}$

= 35.4 ohms (Rounding up or down to the nearest standard resistor value)

= 33 ohms

Method 2 of 2: (More accurate)

Set an I/O pin as an output, driving a logic high into a 1k resistor to ground. Many I/O pins have selectable drive strength, hence configure the pin the same as required for the high-speed signals in the application. Record the measured MCU VDD and the VOH across the 1k resistor.

- Driver Impedance = $((VDD-VOH) * 1K) / VOH$
- PCB signal series termination resistor(s) value = (Driver Impedance - Trace Impedance)

Unterminated signal frequencies >30 MHz range can experience over/under shooting in the 50% range. Unterminated high-speed signals can be a significant contributor to the radiated EMI/EMC signature and crosstalk.

2. Minimize the use of vias throughout the design on high-speed signals. Vias add capacitance and distort impedance to the high-speed signal traces.
3. In general, review all signal cross talk design rules to avoid cross talk problems. Use the 3-W rule to provide enough trace separation to avoid cross talk problems. Guard traces may also be utilized to minimize cross talk problems on high-speed signals.

17.4 PCB Trace Considerations

1. PCB traces must be routed using 45° corners when changing directions. 90° corners must never be used.
2. All component leads to any power plane or ground plane must be as short as possible. The best solutions are plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections must be less than 5-10 mils in length. Trace connections must be as wide as possible to lower inductance. This will include any power ferrite beads feeding power planes, fuses feeding power planes, and so on.

[Return to Checklist](#)

18. Revision History

Revision A - September 2020

This is the initial released version of this document.

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