Lab No. 7: FMSD

Leonardo Fusser (1946995)

Objective: design a FMSD combining a counter with an FSM.

Hardware: see previous lab.

To hand in:

Listing of the following for each of your designs on LEA:

1. This sheet with answers and all screenshots.
2. Commented Verilog source files - module and top module.
3. Verilog testbench source file (with proper prolog headers).
4. A block diagram (Visio or other).
5. A state diagram using Visio or other Apps. Failure to submit a state diagram will result in **10 points** lost.

Also

- Each and every module should include a header.
- The main file must include a header: Lab number and name, author, description, version number.

Lab Work

Part1: Design and test bench a FMSD

You must design a delayed event by re-using modules and FSM from previous labs.
A time delayed event must trigger 9 seconds after the lock's secret code has been entered successfully.
The countdown must be displayed on one digit.
The trigger must represented by turning on all remaining three LEDs.
Therefore, all LEDS must be lit.

Once triggered, the system must be reset to restart.

	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
No code entered or reset or wrong code	**0**							
First code successfully entered								**0**
Second code successfully entered							**0**	**0**
Third code successfully entered						**0**	**0**	**0**
Fourth code successfully entered					**0**	**0**	**0**	**0**
9 seconds after the fourth code successfully entered	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Re-use/adapt the previous' lab combinational lock for this lab.

1. Draw the system's block diagram.
2. Write a module for your FSM. In order to keep your code portable and modular you must take a top module approach. The lock FSM, the prescaler counter, the countdown and the 7-segment-decoder should be 4 separated modules.

```
module top(
  input  mclk,
  input  [3:0] btn,
  input  sw0,       //Reset
  output [7:0] Led,
  output [6:0] seg,
  output [3:0] an
  );
```

Test Bench:

Test bench you FSM.

- Refer to “Figure 1” and “Figure 2” below.

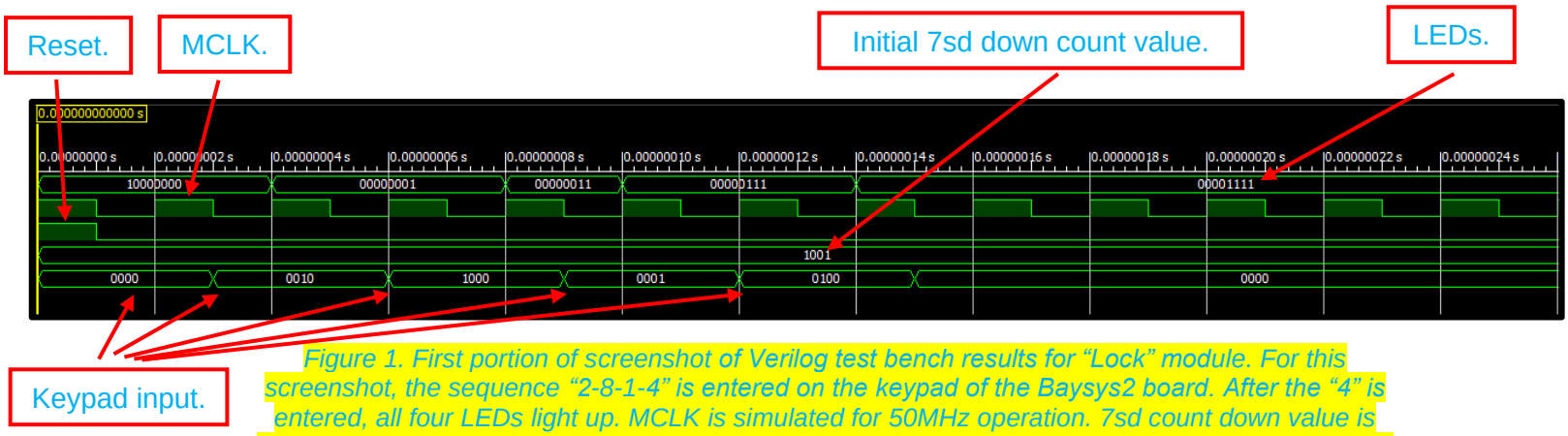

Figure 1. First portion of screenshot of Verilog test bench results for “Lock” module. For this screenshot, the sequence “2-8-1-4” is entered on the keypad of the Baysys2 board. After the “4” is entered, all four LEDs light up. MCLK is simulated for 50MHz operation. 7sd count down value is initially 9 but is not lit on the 7sd until after all four keypad inputs are entered correctly (value of ANx not showed in the screenshot). Count down starts after correct keypad sequence is entered.

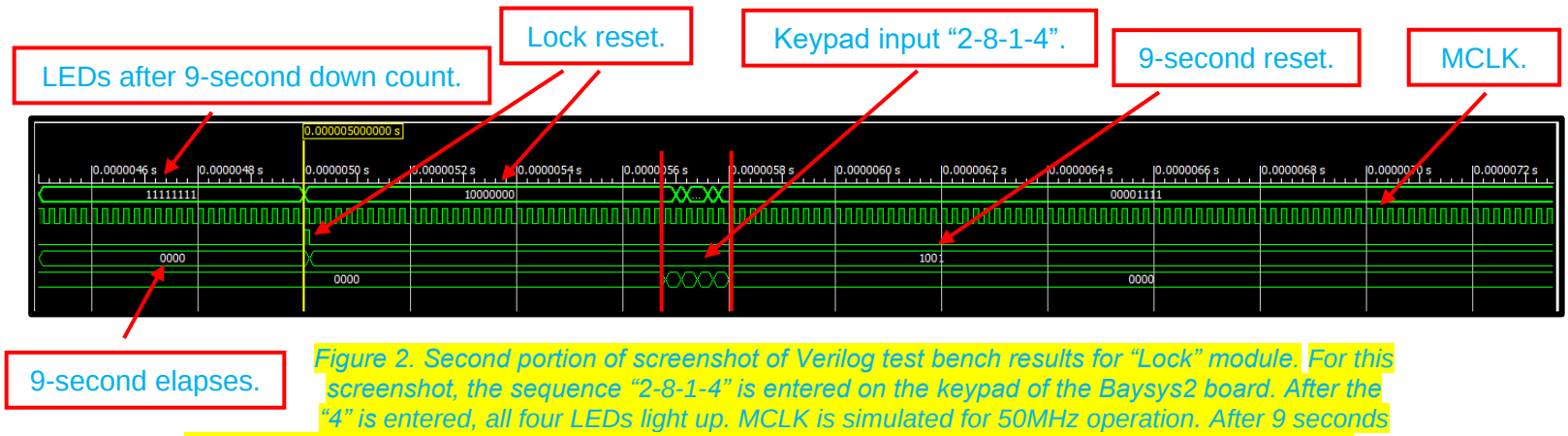

Figure 2. Second portion of screenshot of Verilog test bench results for “Lock” module. For this screenshot, the sequence “2-8-1-4” is entered on the keypad of the Baysys2 board. After the “4” is entered, all four LEDs light up. MCLK is simulated for 50MHz operation. After 9 seconds (when count down reaches 0), all eight LEDs are lit on the Baysys2 board. User can enter new keypad sequence when the lock is reset and the count down value goes back to 9. The count down sequence is not shown on the 7sd until all four keypad inputs are entered correctly (value of ANx not showed in the screenshot).

Test on the target:

Download the code on the target and test it on the target.

[Verilog code for Lab 7]

- Refer to code for “bin2seg” module in “bin2seg.txt” attached to this report submission.
- Refer to code for “Down_counter” module in “Down_counter.txt” attached to this report submission.
- Refer to code for “Lock” module in “Lock.txt” attached to this report submission.
- Refer to code for “PulseGen” module in “PulseGen.txt” attached to this report to this report submission.
- Refer to code for “Lab7_TOP” module in “Lab7_TOP.txt” attached to this report submission.

[Constraints file for Lab 7]

- Refer to code for “Lab7_constraints” file in “Lab7_constraints.txt” attached to this report submission.

[Test bench code for Lab 7]

- Refer to code for “Lock_TB” module in “Lock_TB.txt” attached to this report submission.

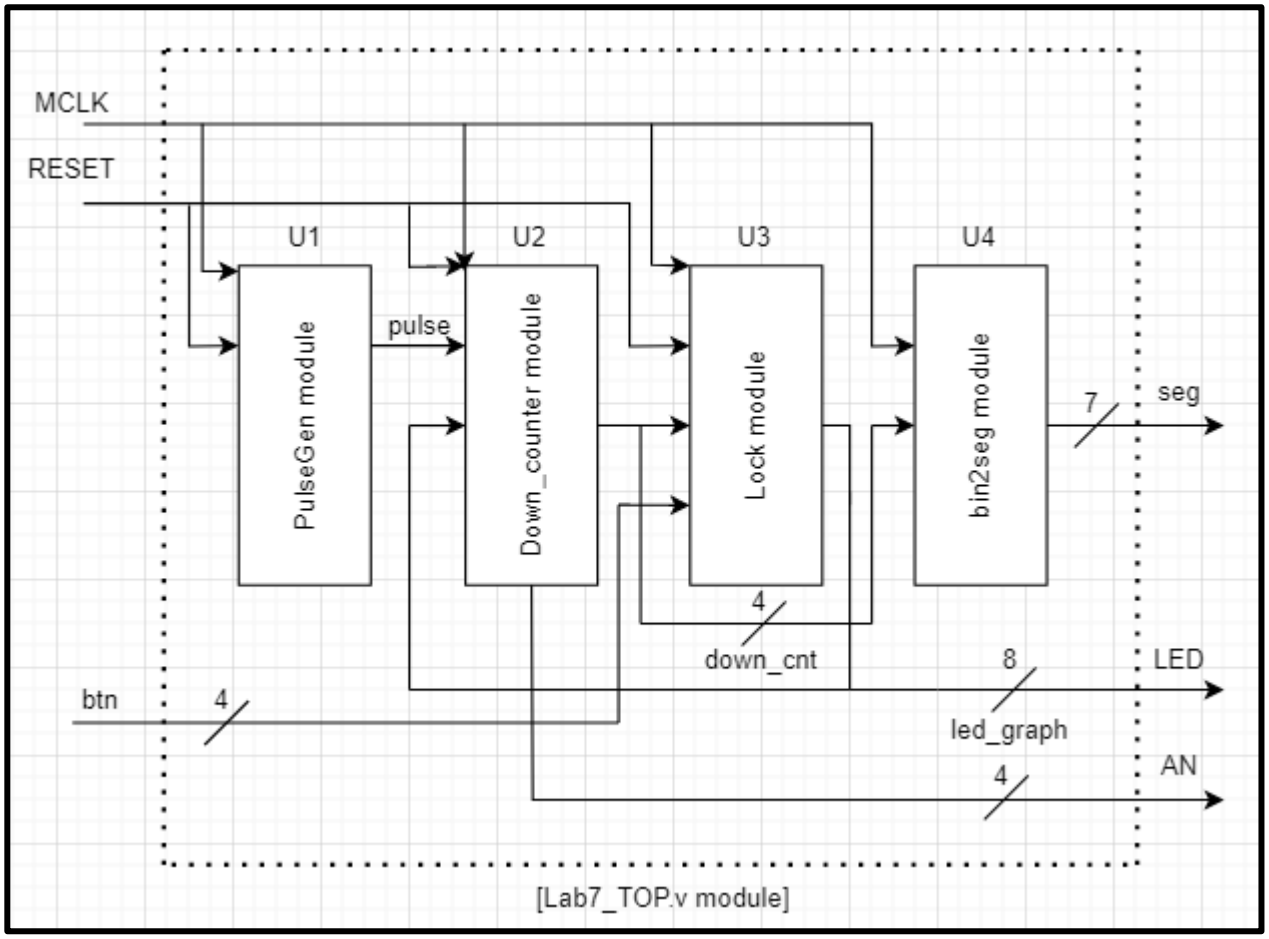

Figure 3. Block diagram for Lab 7 shown above.

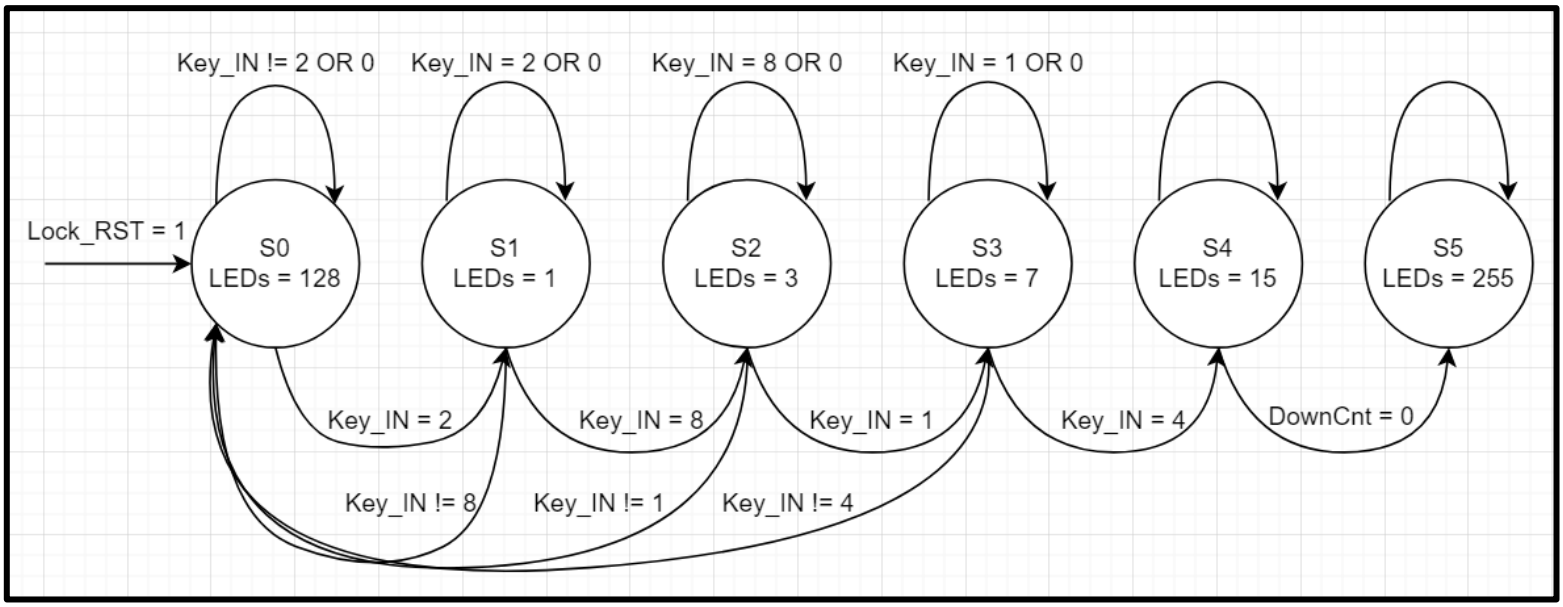

Figure 4. State diagram for Lab 7 shown above.