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VANIER COLLEGE - Computer Engineering Technology
247-205 Circuit Analysis and Simulation II

Lab 9 - Transistor and voltage-divider biasing

Purpose:

a) To test NPN and PNP transistors using a multimeter
b) To verify the voltages and currents in a transistor voltage-divider bias circuit
c) To construct the dc load line

To be submitted:

1. **Deadline**: In a week, to be submitted via Lea.
2. **NO formal report is required**.
    a. **Answer all the questions** in the lab in the blank space provided. (this is where you get your marks)
    b. If calculation is involved, clearly show all the working steps involved. (you can do it on a paper take a picture and add it to the word document in the proper place.)
    c. Attach table/plot, screen shots clearly labelled, whenever applicable.
    d. Include a final discussion and conclusion session.
3. **TO HAND IN:**
    a. This word document filled in properly.
    b. Your Proteus files.
    c. Please do not Zip the file, instead hand in two files one after the other.

Theory:

A transistor can be represented internally by 2 diode junctions. Hence, a multimeter/ohmmeter can be used to check each diode junction with simple test for open or shorted diode junctions. Then it is possible to determine if a given transistor is NPN or PNP.

Voltage-divider bias is often used because the based current is made small compared to the currents through the two base resistors. Consequently, the base voltage and collector current are stabilized against changes in the circuit.

Lab Work:

Part 1: Preparation

1. Do a bit of research on the web about how to use a multimeter to determine if a transistor is PNP or NPN. Write it up in your words.

    - **Determine the package type of the transistor to determine the placement of E, C and B (ex: TO92A, TO92B…).**
    - **Using a multimeter, put it in continuity or diode test mode.**

- **Based on the package type of the transistor, test the individual junctions of the transistor.**
- **Take measurements between the Emitter and the Base of the transistor.**
- **Record the results.**
- **If the transistor is an NPN transistor, there should be no conductivity between the Emitter and the Base of the transistor (Positive lead on E, negative on B).**
- **If the transistor is an PNP transistor, there should be a voltage drop between the Emitter and the Base of the transistor (If silicon: then 0.7V, if germanium: 0.3V).**
- **If any of the junctions are tested open, that junction is shorted.**

Using a typical value for the base-emitter voltage of a silicon transistor, 0.7 V, calculate the expected values of the dc-based voltage (V_B), emitter voltage (V_E), collector voltage (V_C), collector current (Ic), and collector-emitter voltage (V_{CE}) for the voltage-divider bias circuit shown in the schematic diagram of

2. Figure 1. ***Show all your calculations***. Record these values in Table 1.

Part 2: Voltage-divider biasing

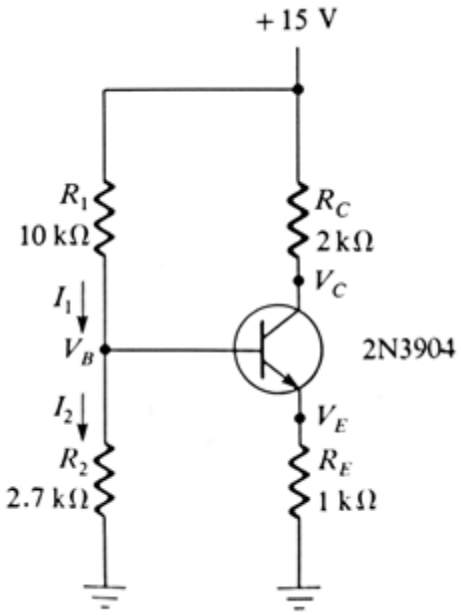


Figure 1 : Voltage-divider biasing

Parameter	Calculated values (pre-lab)	Measured values
V_B	***3.19V***	***3.15V***
V_C	***10.02V***	***10.09V***
V_E	***2.49V***	***2.46V***
V_{CE}	***7.53V***	***7.62V***
I_C	***2.49mA***	***2.45mA***

Table 1 : Basic voltage divider biasing readings

The calculations could be found at the end of this document.

Watch the 4 YouTube videos in order.
First video https://youtu.be/6m_7lFedM0I
Second video https://youtu.be/M-KqZEUYwEY
Third video to watch https://youtu.be/YdvsuXRV0OQ
Last video for this LAB https://youtu.be/regqmA8at-8

3. Using Proteus wire figure 3. Use DMM to measure V_B, V_E, V_C, V_{CE} and I_C. Record your values in Table 1. and compare with the calculated values from Pre-Lab.
   - **As one can see, the results that were calculated in the pre-lab are very close to the results obtained in the simulation (measured values). Therefore, the calculations that were made are correct.**

4. Measure I_1, I_2 and I_B of your circuit and record in Table 2.

Parameter	Value
I_1	***1.18mA***
I_2	***1.16mA***
I_B	***15.38uA***

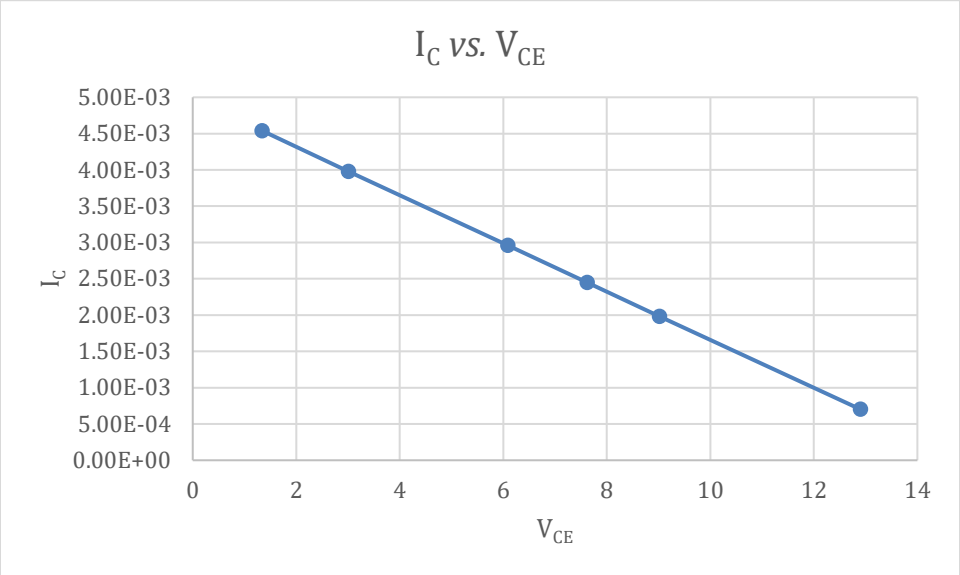
Table 2 : Measured values

5. What is the theoretical relationship between these current? Do your measurements conform to this?
   - **The relationship between these currents are proportional to each other. One could use KCL to answer the question. For example, I1 – I2 = IB, I2 + IB = I1…**

6. Change the value of resistor R_2 and take the following measurements in order to fill table 3.

R_2	I_C	V_{CE}
1K	***701.89uA***	***12.9V***
2.2K	***1.98mA***	***9.02V***
2.7K	***2.45mA***	***7.62V***
3.3K	***2.96mA***	***6.09V***
4.7K	***3.98mA***	***3.01V***
5.6K	***4.54mA***	***1.34V***

7. Draw a graph of I_C vs V_{CE}, this is your dc load line. You will see the theory next week for the load line.



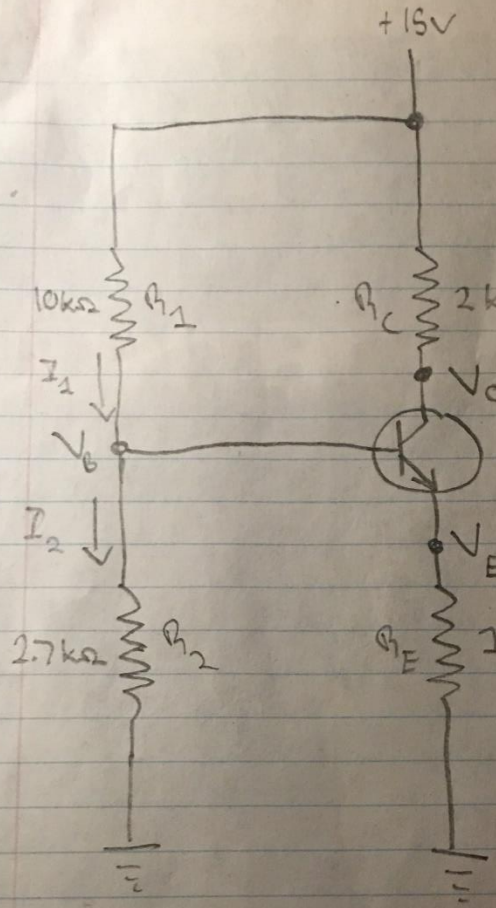
R_2	I_C	V_{CE}	I_C
1K	7.02E-04	12.9	7.02E-04
2.2K	1.98E-03	9.02	1.98E-03
2.7K	2.45E-03	7.62	2.45E-03
3.3K	2.96E-03	6.09	2.96E-03
4.7K	3.98E-03	3.01	3.98E-03
5.6K	4.54E-03	1.34	4.54E-03

The excel spreadsheet has been sent to you along with this document.

Discussion/Conclusion:

- **This was the first lab, where I simulated an NPN transistor. Along with this, I learned how to test/identify an NPN and PNP transistor. In the simulation, I simulated a 2N3904 NPN transistor in a voltage-divider bias circuit and compared results with calculations that were done before the simulation. Furthermore, I created a graph plotting various points, creating what's called the "DC load-line". This showed how the transistor behaved. I additionally learned some more feature in Proteus.**

Question 2 calculations



$$V_B \cong \left(\frac{R_2}{R_1+R_2}\right)\cdot V_{cc}$$

$$= \left(\frac{2.7k\Omega}{10k\Omega+2.7k\Omega}\right)\cdot 15V$$

$$\boxed{V_B = 3.19V}$$

$$V_E = V_B - V_{BE}$$

$$= 3.19V - 0.7V$$

$$\boxed{V_E = 2.49V}$$

$$I_E = \frac{V_E}{R_E}$$

$$= \frac{2.49V}{1k\Omega}$$

$$\boxed{I_E = 2.49mA}$$

$$V_{CE} = V_C - V_E$$

$$= 10.02V - 2.49V$$

$$\boxed{V_{CE} = 7.53V}$$

$$I_E \cong I_C$$

$$\boxed{I_C = 2.49mA}$$

$$V_C = V_{cc} - I_C \cdot R_C$$

$$= 15V - (2.49mA)\cdot(2k\Omega)$$

$$\boxed{V_C = 10.02V}$$