Computational Logic Circuits (Lab 4)

zyBooks & even parity generator

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Experiment Performed on **21 February 2020**
Report Submitted on **28 February 2020**

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OBJECTIVES

- To understand the topics covered in zyBooks for this week's lab.
- To understand how an even parity generator for a 3-bit word works.
- To understand how to effectively create Logic Circuits.

DESIGN

Experiment

- There were two parts in this lab. First, we asked to finish chapter 4 in our zyBooks. Then, we had to design and build an even parity generator for a 3-bit word by using one gate type (NAND). The circuit has 3 inputs, A, B and C. The output for the circuit will be '1' if the number of inputs that are HIGH are odd. The output for the circuit will be '0' if the number of inputs that are HIGH are even. A truth table, k-map, SOP equation, POS equation and logic diagram (using NAND gates) from the SOP and POS equations were created during the lab.

SCHEMATICS

Schematics from the Experiment

The schematic for the even parity generator for a 3-bit word (POS and SOP logic circuit diagrams) is on the attached loose-leaf.

QUESTIONS

Questions from the Experiment

There are no questions that were asked for this lab.