VANIER COLLEGE – Computer Engineering Technology – Winter 2021

Telecommunications (247-410-VA)

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# LABORATORY EXPERIMENT #6

## Analog-Digital Conversion

**NOTE**:

To be submitted using the typical lab format, one week later – at the start of your lab session.

This exercise can be done in individually or in teams of **2 students**, however each student must submit a lab report with original observations and conclusions.

## ***OBJECTIVES***

After performing this experiment, the student will be able to:

1. Build and test an ADC circuit.
2. Build and test a DAC circuit.
3. Explain the effect of resolution and quantization noise.
4. Explain the importance of sampling rate.

# *PROCEDURE*

## <u>Part 1</u>: Proteus installation

Download Proteus:
These are the installation and setup details for Vanier College CET program.

You MUST Install 8.11:

Please download the Proteus Software from the following link:

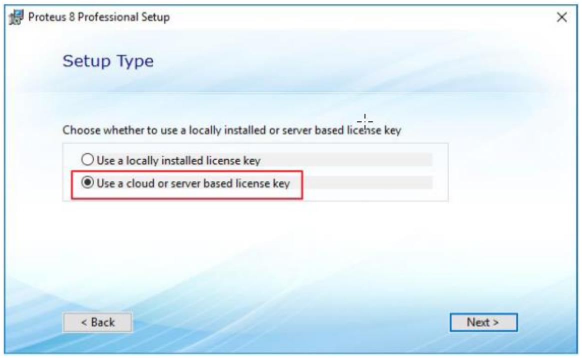
<u>http://downloads.labcenter.co.uk/prosys811/proteus8.11.SP1.exe</u>

Username: proteus811
Password: swift196CHAIN

**Installation Instructions:**
**-----------------------------------**

There is an instruction video here: <u>https://labcenter.s3.amazonaws.com/movies/v8/cloudLicenceClient.mp4</u>

During in the installation You need to select Network / Cloud License option:



Proteus 8 Professional Setup

Setup Type

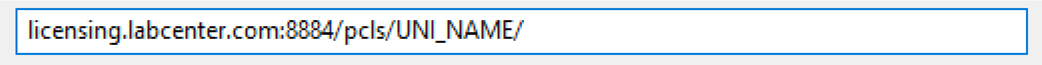
Choose whether to use a locally installed or server based license key

○ Use a locally installed license key
● Use a cloud or server based license key

and then enter the following:

**licensing-am.labcenter.com:8884/pcls/Vanier/**

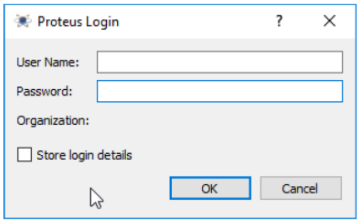
(including all '/'). Please note that Outlook or other email clients may recognize the above link as a web address and automatically add **http://** in front of it. This would then be <u>incorrect</u>. It should be entered in like the following:



licensing.labcenter.com:8884/pcls/UNI_NAME/

Where UNI_NAME is replaced with the above name.

Once Proteus is installed you can open Proteus and you will be presented with a login box:



Proteus Login

User Name:
Password:
Organization:

□ Store login details

Your Proteus Username is:
**Vanier**

The Proteus Login password is:
**ef_EjAg8=!**

## Part 2: A to D Converter

1. Read the ADC0804 data sheet: http://www.ti.com/lit/ds/symlink/adc0804-n.pdf
2. Explain the pins of A-to-D.

- The ADC0804 is an 8-bit analog-to-digital converter (ADC) which has a total of 20 pins and can handle a 0-5V analog input voltage (done on Vcc or Vref - pin 20). The table below describes all the pin functions:

| **Pins** | | **Input or Output** | **Description** |
|---|---|---|---|
| **Number** | **Name** | | |
| 1 | CS | Input | Chip select |
| 2 | RD | Input | Read |
| 3 | WR | Input | Write |
| 4 | CLK IN | Input | External Clock input or use internal clock generator with external RC elements |
| 5 | INTR | Output | Interrupt request |
| 6 | Vin + | Input | Differential analog input + |
| 7 | Vin - | Input | Differential analog input - |
| 8 | A GND | Input | Analog ground pin |
| 9 | Vref/2 | Input | Reference voltage input for adjustment to correct full scale reading |
| 10 | D GND | Input | Digital ground pin |
| 11 | DB7 *(MSB)* | Output | Data bit 7 |
| 12 | DB6 | Output | Data bit 6 |
| 13 | DB5 | Output | Data bit 5 |
| 14 | DB4 | Output | Data bit 4 |
| 15 | DB3 | Output | Data bit 3 |
| 16 | DB2 | Output | Data bit 2 |
| 17 | DB1 | Output | Data bit 1 |
| 18 | DB0 *(LSB)* | Output | Data bit 0 |
| 19 | CLK R | Input | RC timing resistor input pin for internal clock generator |
| 20 | Vcc or Vref | Input | +5V supply voltage, also upper reference input to the ladder |

*Information above taken directly from the ADC0804 datasheet. Datasheet can be found here: http://www.ti.com/lit/ds/symlink/adc0804-n.pdf

3. Make a project A-to-D and build the following ADC Circuit on the proteus:

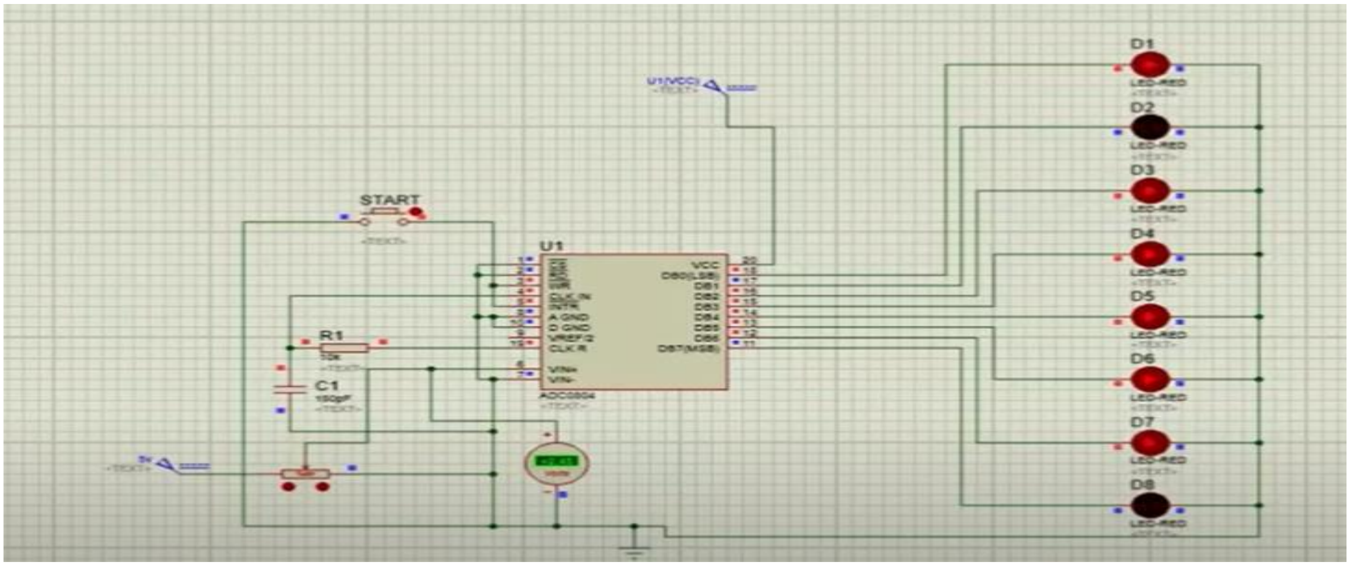
   Vcc 5V

   V pot 5V

   Note that setup is in free running mode where pins 1 and 2 are connected to ground, pin 3 is connected to pin 5.

Components:

- a) ADC0804.
- b) Pushbutton.
- c) Ceramic 150P capacitor.
- d) LED-RED.
- e) Res 4.7KΩ, 10KΩ.
- f) Potentiometer 1KΩ POT-HG.
- g) DC voltmeter, DC power supply.

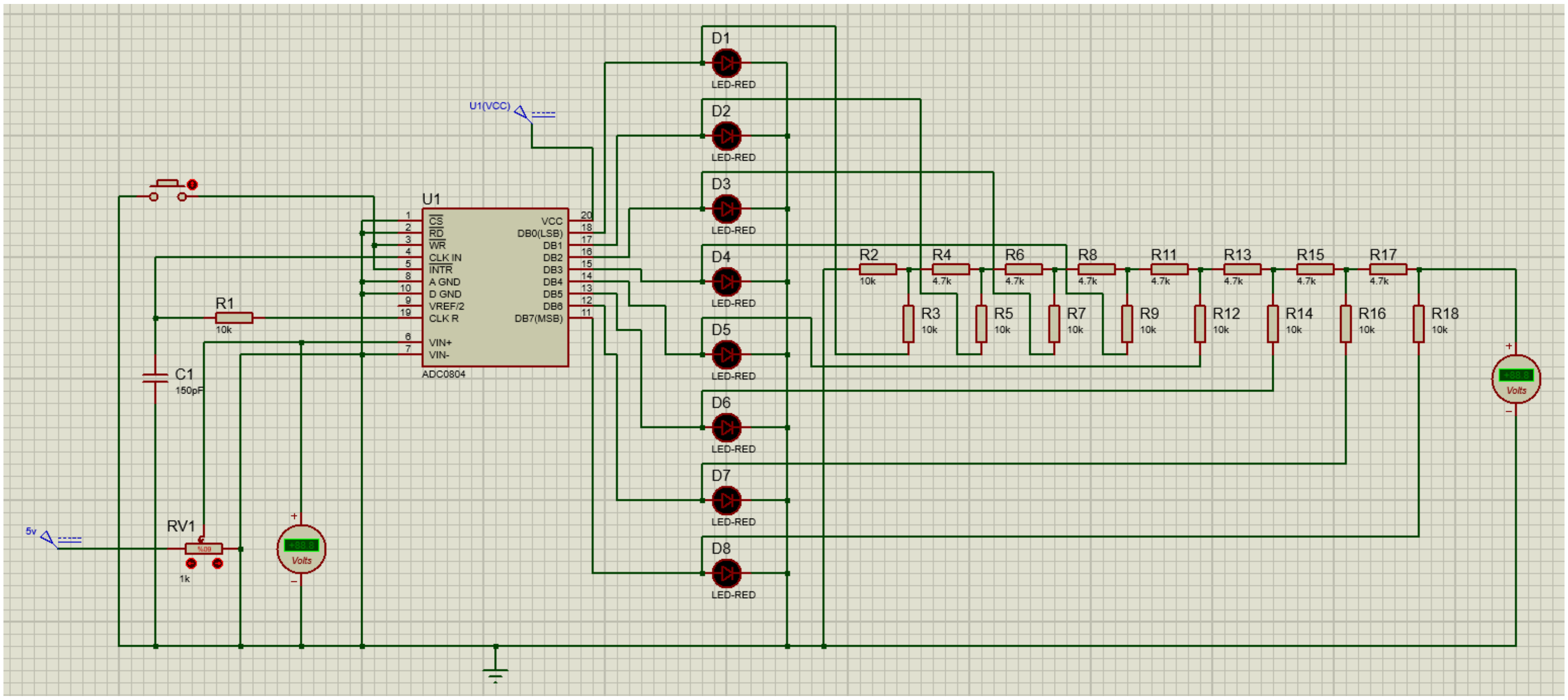


4. Monitor Vin of A to D. Vary 10kΩ potentiometer for 0V – 5V in 0.5V steps. For each voltage settings record the digital values seen on DB0-DB7.
    a) Show the input voltages and the corresponding 8-bit binary value in a table in your report.
    b) Convert the outputs to decimal and compare these values to theoretical values that you will calculate. Comment on your results.

| **Voltage input** | **Measured binary output**<br>(D8 – D7) | **Measured decimal output** | **Theoretical (calculated) decimal value**<br>$Number\ of\ increments = 2^8 - 1 = 254$ |
|---|---|---|---|
| 0V | 00000000 | 0 | $Output = \frac{254 * 0V}{5V} = 0$ |
| 0.5V | 00011001 | 25 | $Output = \frac{254 * 0.5V}{5V} = \sim 25$ |
| 1V | 00110011 | 51 | $Output = \frac{254 * 1V}{5V} = \sim 51$ |
| 1.5V | 01001100 | 76 | $Output = \frac{254 * 1.5V}{5V} = \sim 76$ |
| 2V | 01100110 | 102 | $Output = \frac{254 * 2V}{5V} = \sim 102$ |
| 2.5V | 01111111 | 127 | $Output = \frac{254 * 2.5V}{5V} = 127$ |
| 3V | 10011001 | 153 | $Output = \frac{254 * 3V}{5V} = \sim 153$ |
| 3.5V | 10110010 | 178 | $Output = \frac{254 * 3.5V}{5V} = \sim 178$ |
| 4V | 11001100 | 204 | $Output = \frac{254 * 4V}{5V} = \sim 204$ |
| 4.5V | 11100101 | 229 | $Output = \frac{254 * 4.5V}{5V} = \sim 229$ |
| 5V | 11111111 | 255 | $\frac{254 * 5V}{5} = 254$ |

Based on the results in the table above, the theoretical and measured decimal outputs match. For each analog input, the corresponding output matches more or less what the theoretical value is (see text in yellow above). Therefore, the circuit is wired correctly, and the ADC is working as it should.

5. Perform a research on R-2R resistor ladder DAC. Build a R-2R Resistor Ladder DAC circuit (using 10KΩ and 4.7KΩ resistors) on your breadboard and connect DB0-DB7 (data bits) from the ADC to the corresponding points on the DAC. Show your schematic of your DAC design.



*Schematic of my ADC and DAC shown above. ADC is to the left and DAC is to the right.*

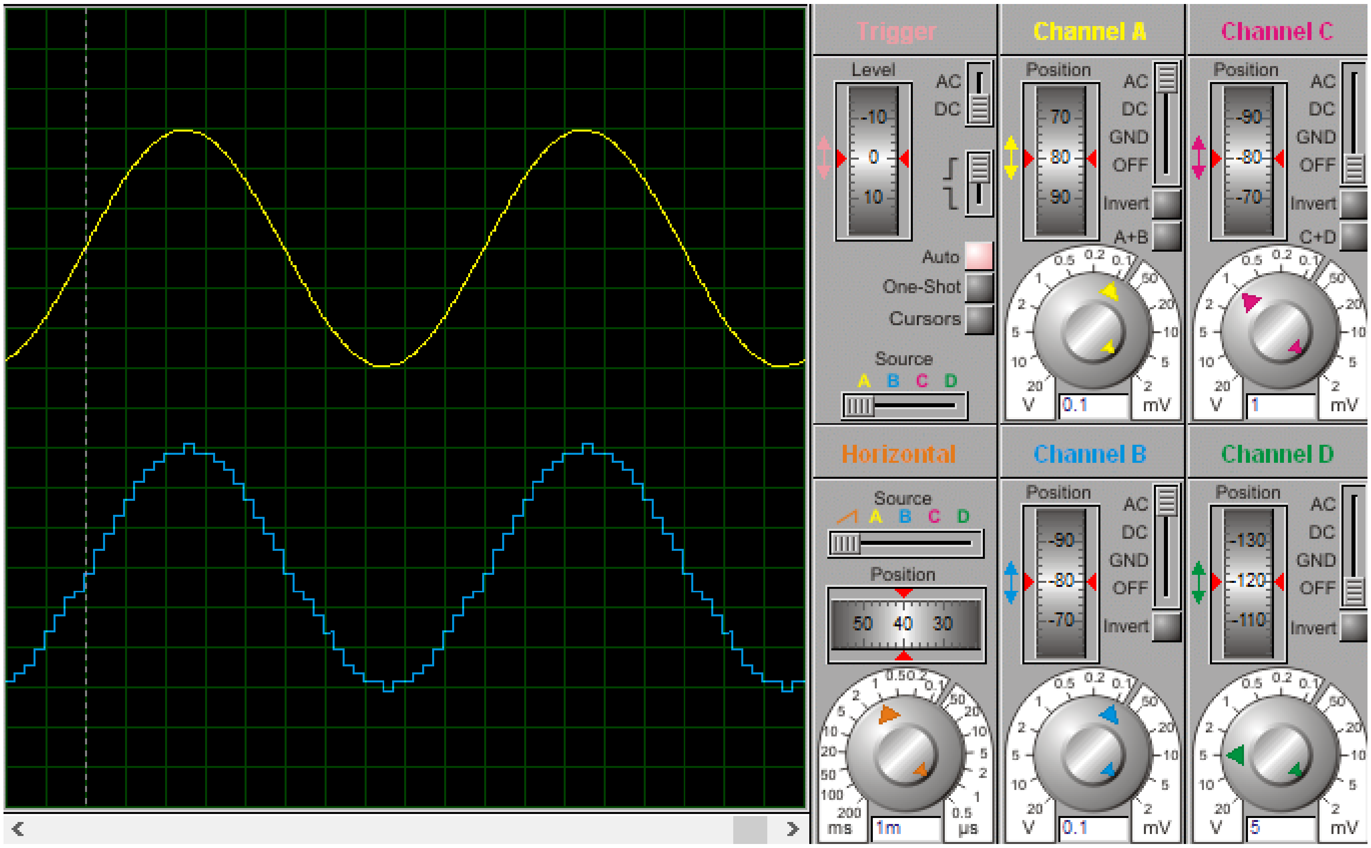
6. Repeat step 4 above, but this time include the measurement of the DC voltage at the output of the DAC.
   a) Show the input voltages (Vin) and the corresponding Analog Out voltages in a table in your report.
   b) Calculate the quantization error for each measurement. Comment on your results.

| **Voltage input** | **Measured binary output**<br>(D8 – D7) | **Measured decimal output** | **Theoretical (calculated) decimal value**<br>$Number\ of\ increments = 2^8 - 1 = 254$ | **Analog out voltages** | **Quantization error**<br>$V_q = V_{OUT} - V_{IN}$ |
|---|---|---|---|---|---|
| 0V | 00000000 | 0 | $Output = \frac{254 * 0V}{5V} = 0$ | 0V | $V_q = 0V - 0V = 0$ |
| 0.5V | 00011001 | 25 | $Output = \frac{254 * 0.5V}{5V} = \sim 25$ | 0.51V | $V_q = 0.51V - 0.5V = 0.01$ |
| 1V | 00110011 | 51 | $Output = \frac{254 * 1V}{5V} = \sim 51$ | 1.03V | $V_q = 1.03V - 1V = 0.03$ |
| 1.5V | 01001100 | 76 | $Output = \frac{254 * 1.5V}{5V} = \sim 76$ | 1.5V | $V_q = 1.5V - 1.5V = 0$ |
| 2V | 01100110 | 102 | $Output = \frac{254 * 2V}{5V} = \sim 102$ | 2.02V | $V_q = 2.02V - 2V = 0.02$ |
| 2.5V | 01111111 | 127 | $Output = \frac{254 * 2.5V}{5V} = 127$ | 2.53V | $V_q = 2.53V - 2.5V = 0.03$ |
| 3V | 10011001 | 153 | $Output = \frac{254 * 3V}{5V} = \sim 153$ | 2.96V | $V_q = 2.96V - 3V = -0.04$ |
| 3.5V | 10110010 | 178 | $Output = \frac{254 * 3.5V}{5V} = \sim 178$ | 3.45V | $V_q = 3.45V - 3.5V = -0.05$ |
| 4V | 11001100 | 204 | $Output = \frac{254 * 4V}{5V} = \sim 204$ | 3.95V | $V_q = 3.95V - 4V = -0.05$ |
| 4.5V | 11100101 | 229 | $Output = \frac{254 * 4.5V}{5V} = \sim 229$ | 4.44V | $V_q = 4.44V - 4.5V = -0.06$ |
| 5V | 11111111 | 255 | $\frac{254 * 5V}{5} = 254$ | 4.98V | $V_q = 4.98V - 5V = -0.02$ |

Based on the results in the table above, the input voltages of the ADC and the output voltages of the DAC match each other. For each voltage input to the ADC, the corresponding voltage output from the DAC matches what the theoretical value is (see text in yellow above). Therefore, the circuit is wired correctly and is working as it should. Also, the quantization error is calculated for each of the different possibilities.

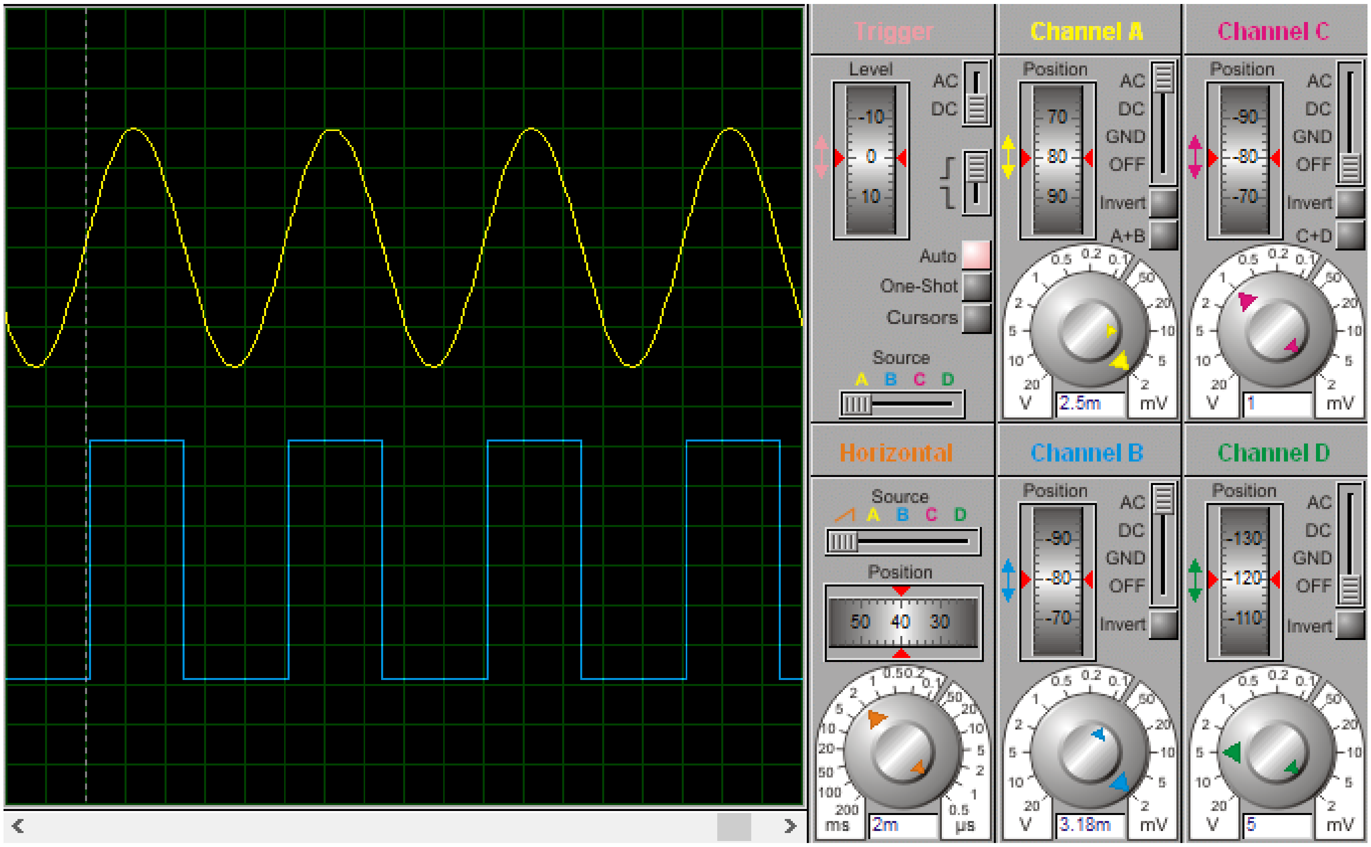
## Part 3: AC input

7. Set the potentiometer such that the voltage at Vin+ is about 2.5 volts. Connect a function generator through a 1.0 µF capacitor (to block the DC bias voltage) to Vin+. Connect an oscilloscope probe to the Analog Output of the DAC.
8. Add a clock generator and connect to WR and intr near the push button. Set it to 4KHz.
9. Set the function generator frequency to 100Hz sine wave with amplitude of 4 Vpp. Take a screen shot of the input waveform and DAC output waveform. Comment on your observation.



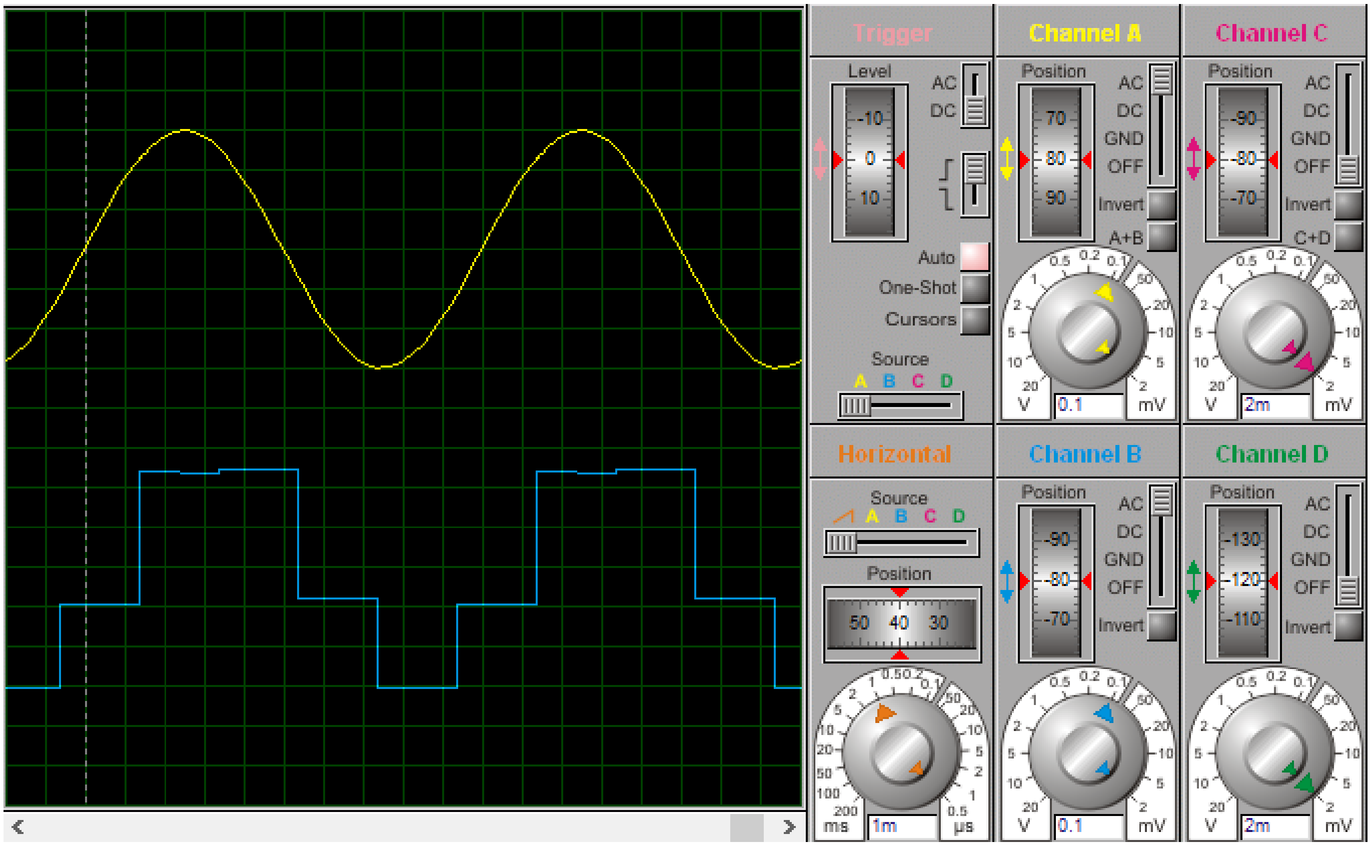
*Yellow signal: original sine wave from ADC and blue signal: sampled signal from original sine wave from DAC shown above. The two signals look the same from first glance but there is a slight difference with the blue signal. If you look closely, the blue signal is not quite a sine wave, but a bunch of pulses put together to form a sine wave. This is because this is an ADC and DAC circuit. The yellow signal is sampled at unique times at the output of the DAC to attempt to reconstruct the original sine wave (shown in the blue signal above). Both signals have a frequency of 100Hz, and an amplitude of 600mV peak-to-peak. This is how a typical ADC and DAC works.*

10. Now change the function generator amplitude to 100 mVpp. Take a screen shot of the input waveform and DAC output waveform. Explain the reason for any difference in waveform shape.

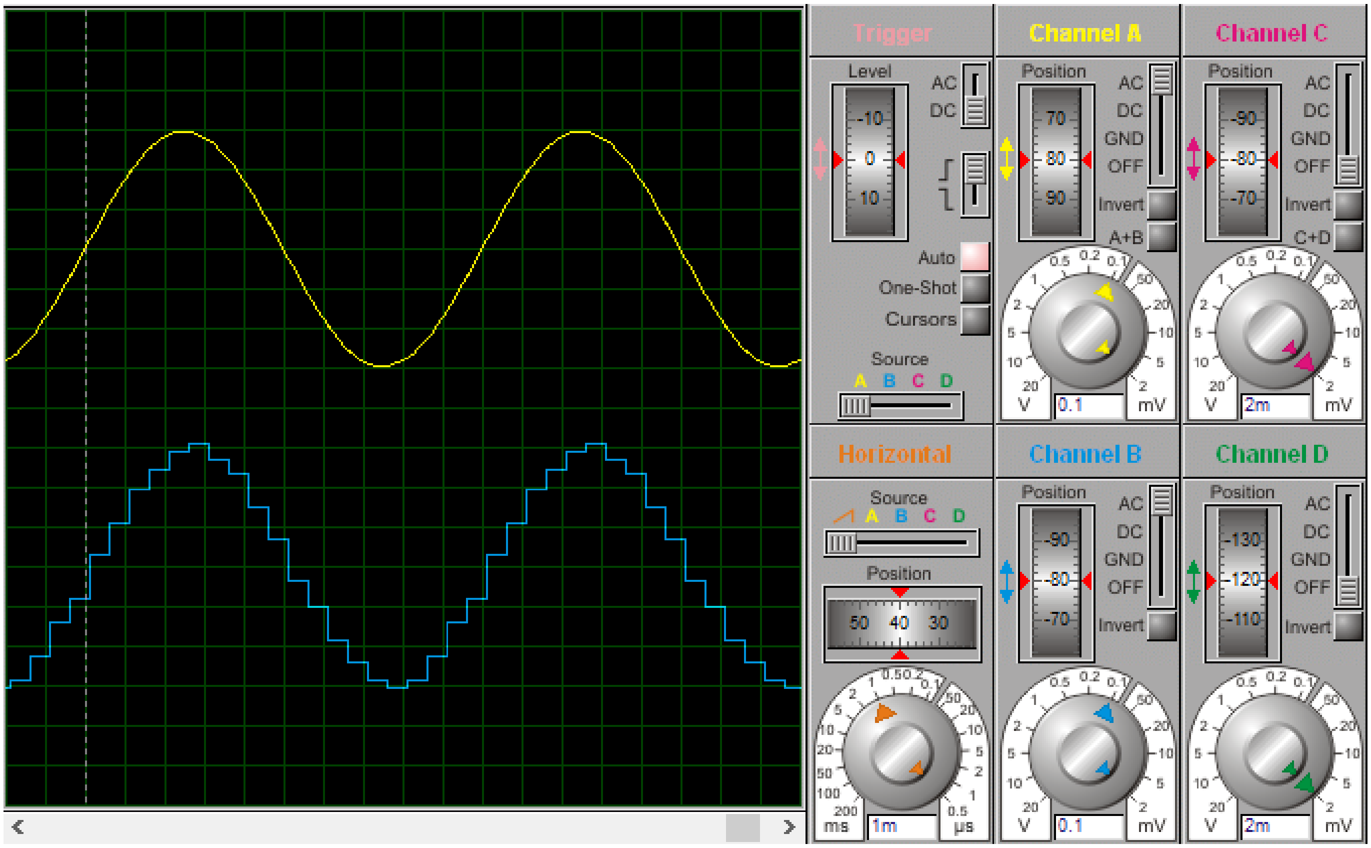


*Original ADC input sine wave (in yellow) and DAC output waveform (in blue) shown above. When the amplitude of the function generator is dropped to 100 mVpp, it seems that the output of the DAC just becomes a square wave instead of a properly sampled signal off the original yellow signal (like what was shown in the previous screenshot). If the amplitude of the function generator is not adequately set, then the resulting output from the DAC will be just a square wave instead of a proper reconstruction of the original signal from the ADC.*

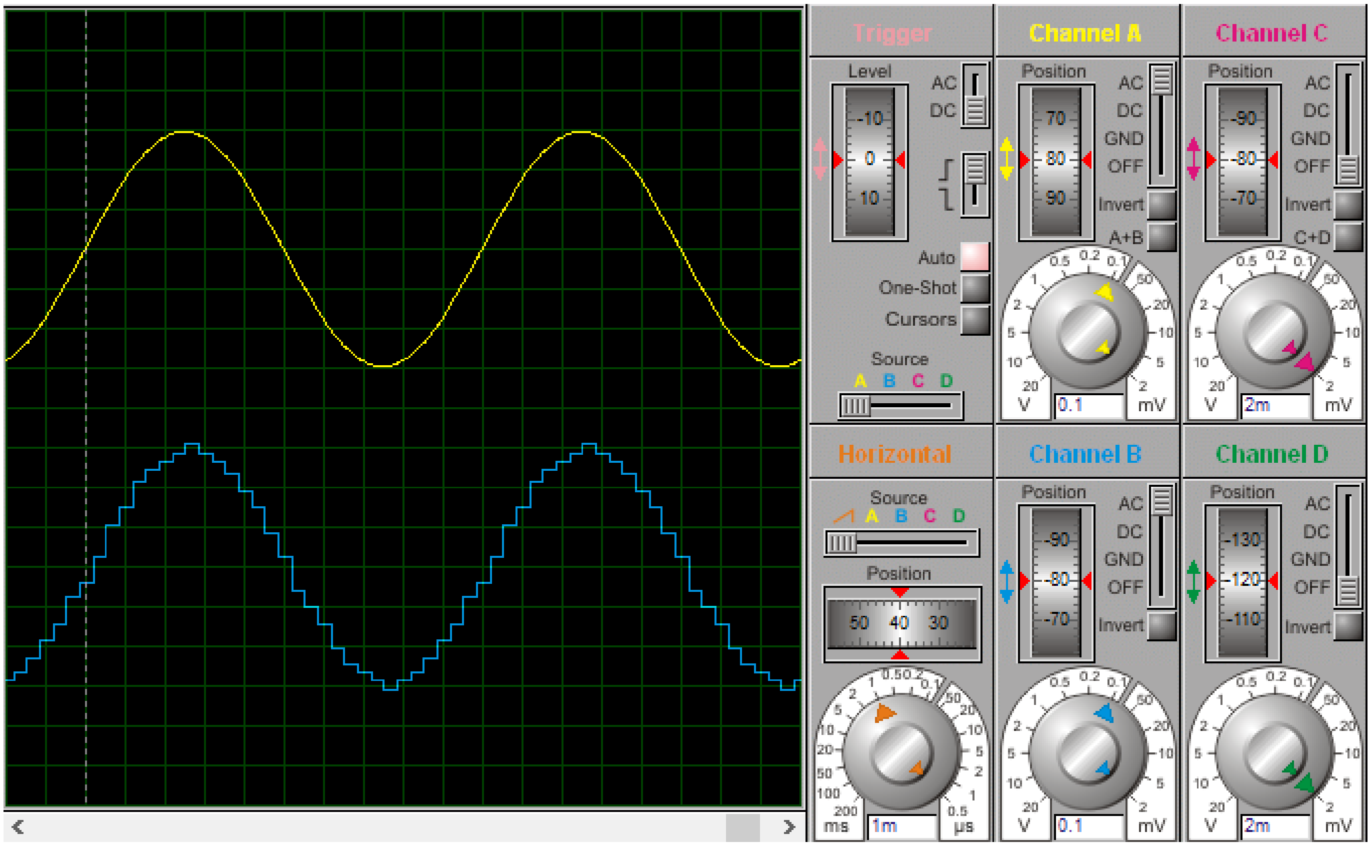
11. Set the function generator amplitude back to 4 Vpp. Repeat step 9 with clock generator frequency of 500 Hz, 2 kHz, 3 kHz, 4 KHz. Perform necessary screen shots. Explain the reason for any difference in waveform shape.



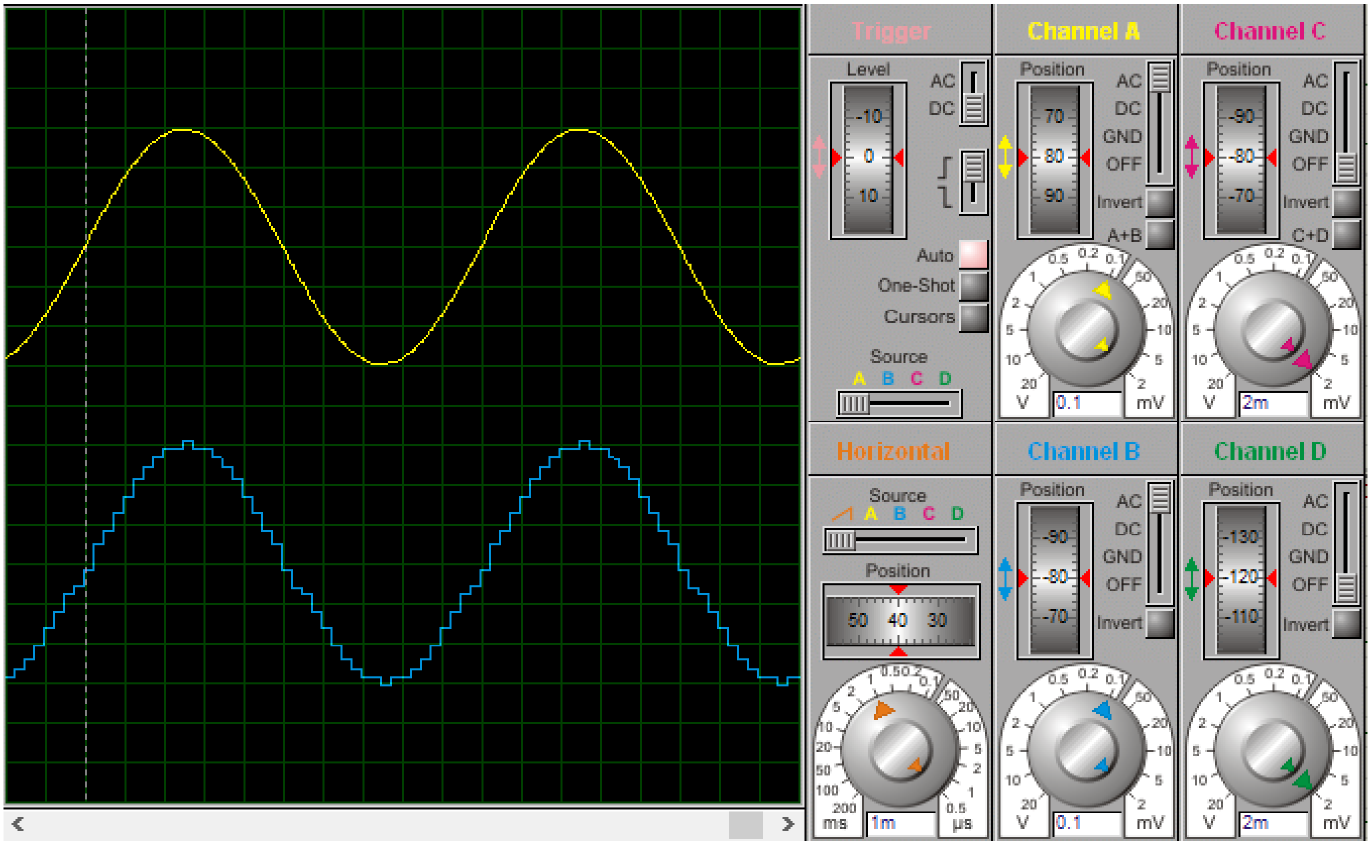
*Result of dropping the clock generator frequency to 500Hz (other parameters remained the same as before). Yellow signal: original sine wave from ADC and blue signal: sampled signal from original sine wave from DAC shown above. Here, it is shown that when the frequency of the clock generator is too low, the original signal from the ADC cannot be reconstructed properly on the DAC. The result, a poorly reconstructed signal that is far from the original signal (this is shown above on the blue signal). What would need to be done for this to work is that the sampling frequency needs to be high enough so that the reconstruction process (sampling) is done properly and that the resulting signal looks as close to as the original. This is shown on the next few pages. The actual frequency of the original signal from the ADC does not have much impact on the output from the DAC.*



*Result of increasing the clock generator frequency to 2kHz (other parameters remained the same as before). Yellow signal: original sine wave from ADC and blue signal: sampled signal from original sine wave from DAC shown above. Here, it is shown that when the frequency of the clock generator is set higher, the original signal from the ADC can be reconstructed properly on the DAC. The result, a reconstructed signal that is closer to the original signal (this is shown above on the blue signal). Even though the reconstructed signal is better than what was shown in the previous screenshot, the reconstructed signal can be sampled even more to look closer to the original signal from the ADC. What would need to be done for this to work is that the sampling frequency needs to be set higher so that more samples can be done. This is shown on the next few pages. Still, the actual frequency of the original signal from the ADC does not have much impact on the output from the DAC.*



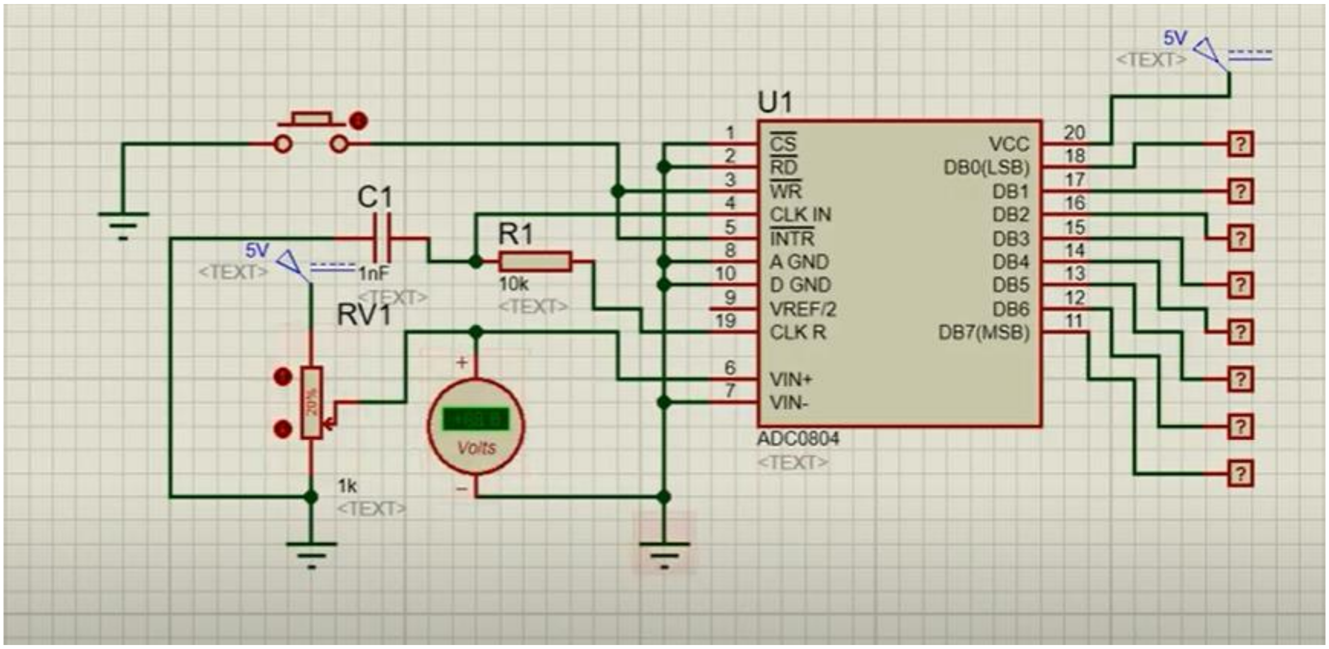
*Result of increasing the clock generator frequency to 3kHz (other parameters remained the same as before). Yellow signal: original sine wave from ADC and blue signal: sampled signal from original sine wave from DAC shown above. Here, it is shown that when the frequency of the clock generator is set even higher, the original signal from the ADC can be reconstructed properly on the DAC. The result, a reconstructed signal that is even closer to the original signal (this is shown above on the blue signal). Even though the reconstructed signal is better than what was shown in the previous screenshots, the reconstructed signal can be sampled even more to look even closer to the original signal from the ADC. What would need to be done for this to work is that the sampling frequency needs to be set even higher so that more samples can be done. This is shown on the next few pages. Still, the actual frequency of the original signal from the ADC does not have much impact on the output from the DAC.*



*Result of increasing the clock generator frequency to 4kHz. Yellow signal: original sine wave from ADC and blue signal: sampled signal from original sine wave from DAC shown above. Here, it is shown that when the frequency of the clock generator is set even higher, the original signal from the ADC can be reconstructed properly on the DAC. The result, a reconstructed signal that is very close to the original signal (this is shown above on the blue signal). This is as best as how the reconstructed signal will get. An even higher sampling frequency will lead to no output from the DAC. Still, the actual frequency of the original signal from the ADC does not have much impact on the output from the DAC.*

# Appendix

*A clear version of the circuit*



*R-2R ladder D to A converter*

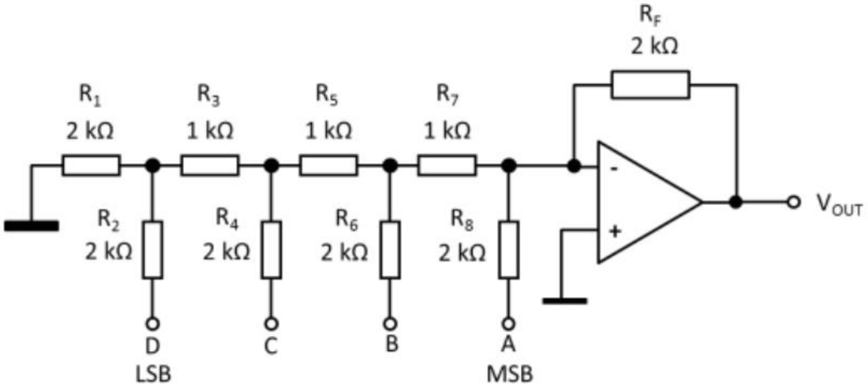


Figure 3