Leonardo Fusser (1946995)
Computational Logic
Subash Handa
April 30th, 2020

FSM Homework

- Finite State Machines:

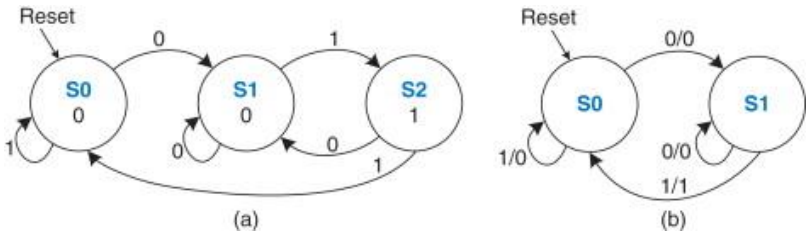
➢ **A *state machine* is a sequential circuit having a limited (finite) number of sates occurring in a prescribed order. A counter is an example of a state machine; the number of states is called the *modulus*. Two basic types of state machines are the Moore and the Mealy. The <u>Moore state machine</u> is one where the outputs depend only on the internal present state where the <u>Mealy state machine</u> is one where the outputs depend on both the internal present state and on the inputs. Both of these types have a timing input (clock) that is not considered a controlling input. Examples are shown below.**

Key points	
Moore machine	***Mealy machine***
➢ **Output depends only upon the present state.**	➢ **Output depends on both present state and present input.**
➢ **Has more states than Mealy machine.**	➢ **Has fewer states than Moore machine.**

- Example, snail with an FSM brain:

➢ **Alyssa P. Hacker owns a pet robotic snail with an FSM brain. The snail crawls from left to right along a paper tape containing a sequence of 1's and 0's. On each clock cycle, the snail crawls to the next bit. The snail smiles when the last two bits that it has crawled over are 01. The input A is the bit underneath the snail's antennae. The output Y is TRUE when the snail smiles. Alyssa's snail crawls along the sequence 0100110111.**

<u>State transition diagrams:</u>



(a) Moore state diagram & (b) Mealy state diagram.
***Note the difference in the amount of states between the two.**
(<u>hint</u>: look at the key points table above.)

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Moore state transition table:

Input (A)	*Current State (S)*		*Next State (S')*		*Output (Y)*
	S1	*S0*	*(S1)'*	*(S0)'*	
0	**0**	**0**	**0**	**1**	**0**
1	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**1**	**0**
1	**0**	**1**	**1**	**0**	**0**
0	**1**	**0**	**0**	**1**	**1**
1	**1**	**0**	**0**	**0**	**1**

***Note that these equations are simplified using the fact that state 11 does not exist. Thus, the corresponding next state and output for the non-existent state are don't cares (not shown in the tables). The Moore machine requires at least two bits of state.**

- **$S'_1 = S_0A$**
- **$S'_0 = A'$**
- **$Y = S_1$**

Mealy state transition table:

Input (A)	*Current State (S)*	*Next State (S')*	*Output (Y)*
	S0	*(S0)'*	
0	**0**	**1**	**0**
1	**0**	**0**	**0**
0	**1**	**1**	**0**
1	**1**	**0**	**1**

***Note the Mealy machine requires only one bit of state.**

- **$S'_0 = A'$**
- **$Y = S_0A$**

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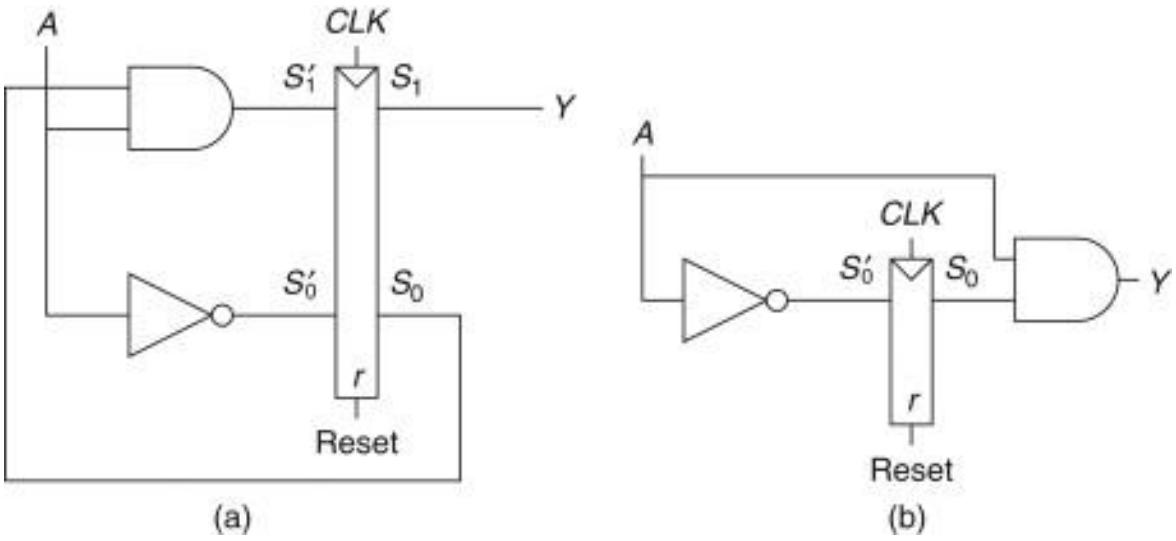
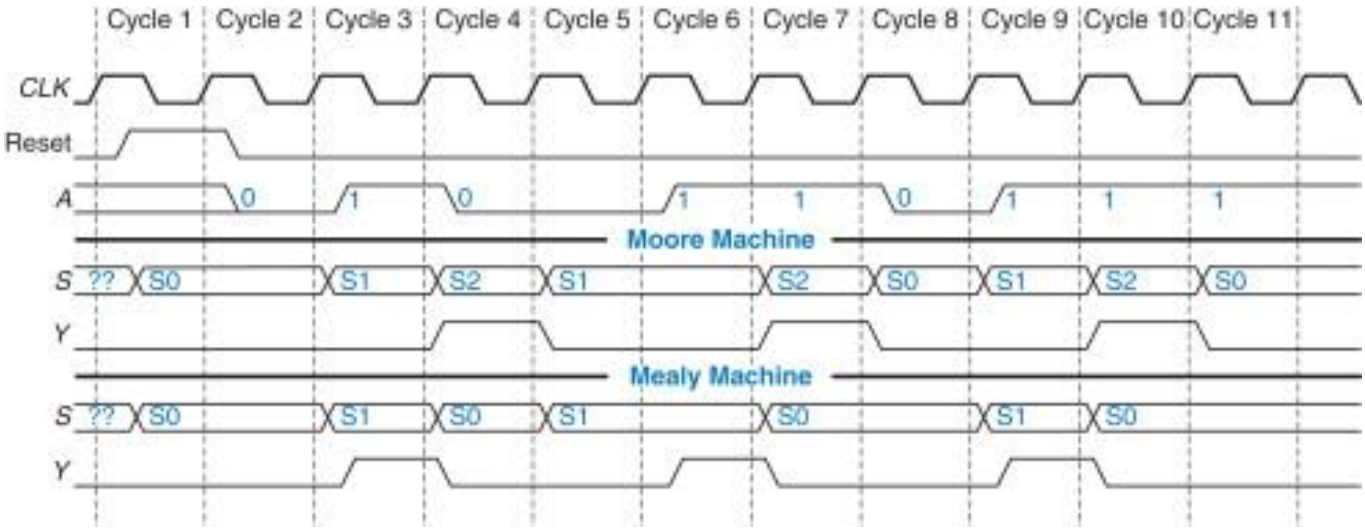
Logic diagrams:



(a) Moore circuit & (b) Mealy circuit.
***Note the difference in the number of gates between the two.**
(hint: look at the key points table above.)

Timing diagram:



***Note the two machines follow a different sequence of states. Moreover, the Mealy machine's output rises a cycle sooner because it responds to the input rather than waiting for the state change. If the Mealy output were delayed through a flip-flop, it would match the Moore output.**

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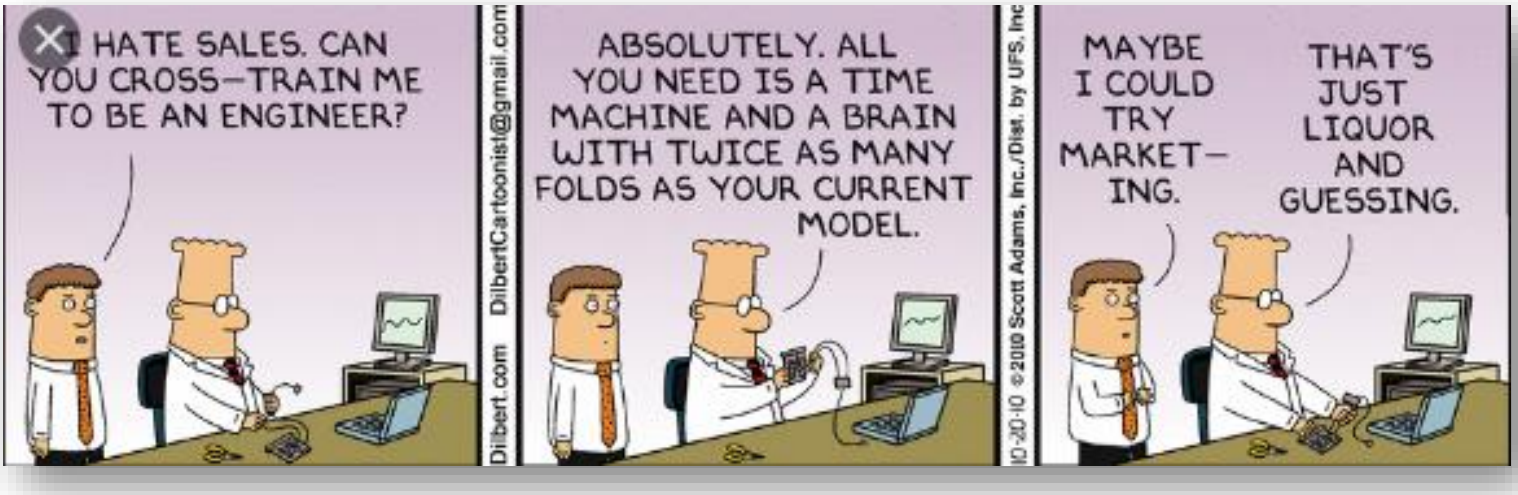
Sources:

- Digital Fundamentals, Eleventh Edition, Thomas L. Floyd, 2015.
- Snail with an FSM brain: https://www.sciencedirect.com/topics/computer-science/moore-machine

Take a look at this!...



I hope all is well with you and your family! I thought I ought to throw in a little something to make us all a little happier. I hope you liked the joke!

As always, take care and stay safe!

-Leonardo