Computational Logic Circuits (Online Lab 3)

Custom Sequencer

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Computational Logic Circuits
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OBJECTIVES

- To understand the function of sequencers.
- To understand how to design a dual sequence sequencer.
- To verify and simulate the function of a 3-bit dual sequence sequencer.

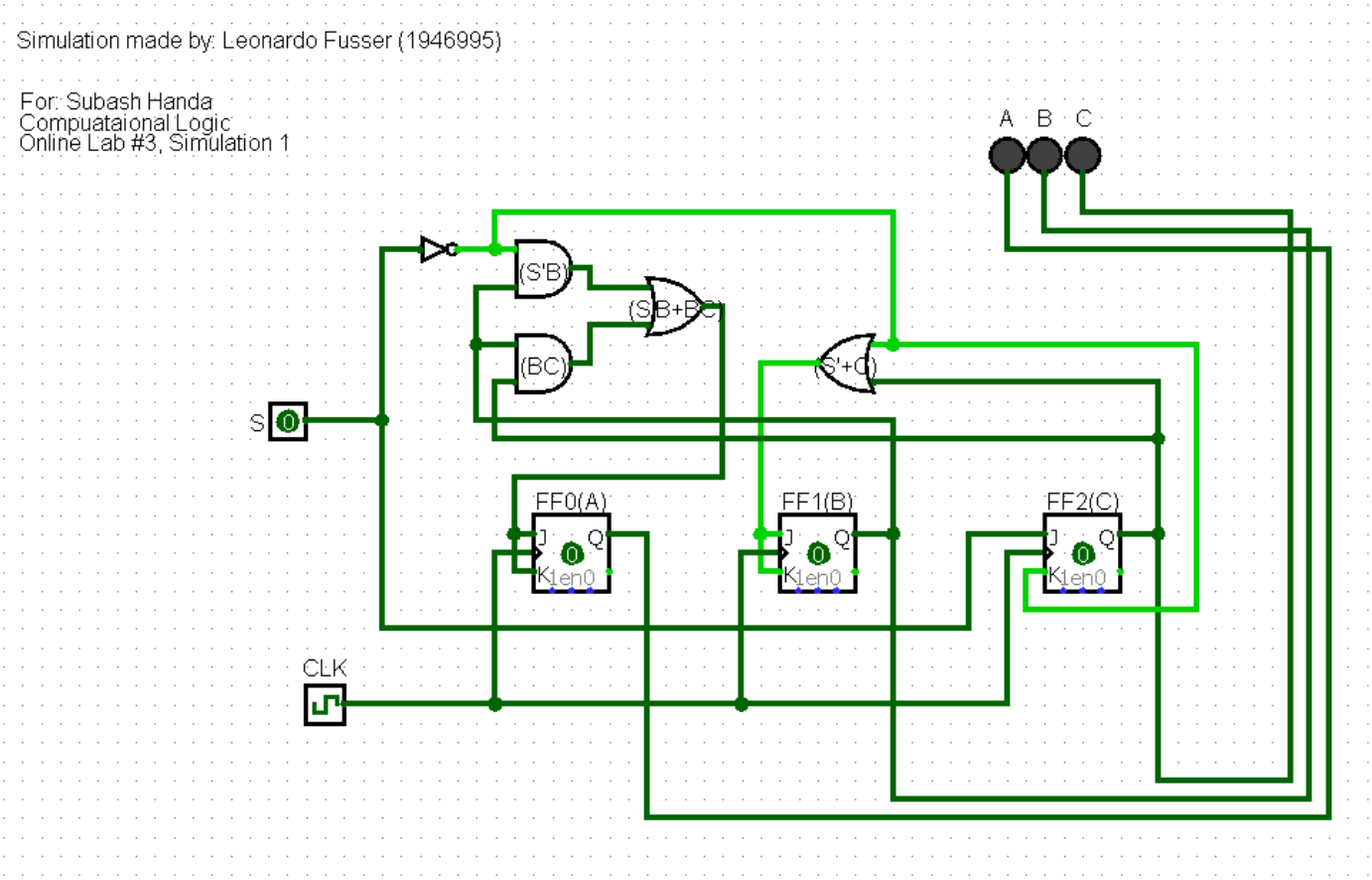
DESIGN

Experiment

- There was one simulation done in this lab. We used the same fundamentals from the last lab. We were asked to create a dual sequence sequencer, where there was an even and odd cycle (an external mode switch was used to select which one). The sequence was in 3-bits so 3 JK flip-flops were used in the simulation. Proper design and testing were done as well. The simulations were done in "Logisim". Below outlines the work done in the lab.

SIMULATIONS

Simulations from the Experiment



Custom 3-bit dual sequence sequencer simulation (above)

Custom 3-bit dual sequence sequencer transition table

Selector	(PRESENT)			(NEXT)			J-K Flip Flops		
	A_N	B_N	C_N	A_{N+1}	B_{N+1}	C_{N+1}	JA/KA	JB/KB	JC/KC
0	0	0	0	0	1	0	0 X	1 X	0 X
1	0	0	0	0	0	0	0 X	0 X	1 X
0	0	0	1	0	1	0	0 X	1 X	X 1
1	0	0	1	0	1	1	0 X	1 X	X 0
0	0	1	0	1	0	0	1 X	X 1	0 X
1	0	1	0	0	1	1	0 X	X 0	1 X
0	0	1	1	1	0	0	1 X	X 1	X 1
1	0	1	1	1	0	1	1 X	X 1	X 0
0	1	0	0	1	1	0	X 0	1 X	0 X
1	1	0	0	1	0	1	X 0	0 X	1 X
0	1	0	1	1	1	0	X 0	1 X	X 1
1	1	0	1	1	1	1	X 0	1 X	X 0
0	1	1	0	0	0	0	X 1	X 1	0 X
1	1	1	0	1	1	1	X 0	X 0	1 X
0	1	1	1	0	0	0	X 1	X 1	X 1
1	1	1	1	0	0	1	X 1	X 1	X 0

FF0: output = A

FF1: output = B

FF2: output = C

Custom 3-bit dual sequence sequencer k-maps

(S)A\BC	*00*	*01*	*11*	*10*
00	0	0	1	1
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

JA = (S'B + BC)

(S)A\BC	*00*	*01*	*11*	*10*
00	X	X	X	X
01	0	0	1	1
11	0	0	1	0
10	X	X	X	X

KA = (S'B + BC)

(S)A\BC	*00*	*01*	*11*	*10*
00	1	1	X	X
01	1	1	X	X
11	0	1	X	X
10	0	1	X	X

JB = (S' + C)

(S)A\BC	*00*	*01*	*11*	*10*
00	X	X	1	1
01	X	X	1	1
11	X	X	1	0
10	X	X	1	0

KB = (S' + C)

(S)A\BC	*00*	*01*	*11*	*10*
00	0	X	X	0
01	0	X	X	0
11	1	X	X	1
10	1	X	X	1

JC = (S)

(S)A\BC	*00*	*01*	*11*	*10*
00	X	1	1	X
01	X	1	1	X
11	X	0	0	X
10	X	0	0	X

KC = (S')

Custom 3-bit dual sequence sequencer state diagram