Computational Logic Circuits (Online Lab 1)

4-bit ripple counter & MOD-10/12 ripple counter

Leonardo Fusser, 1946995

Experiment Performed on **3 April 2020**
Report Submitted on **3 April 2020**

Department of Computer Engineering Technology
Computational Logic Circuits
Subash Handa

VANIER
CÉGEP / COLLEGE
Learning today Leading tomorrow

Table of Contents

OBJECTIVES

- To understand the function of asynchronous and asynchronous decade counters.
- To understand the function of the 4-bit and MOD-10/12 ripple counters.
- To verify and simulate the function of the 4-bit and MOD-10/12 ripple counters.

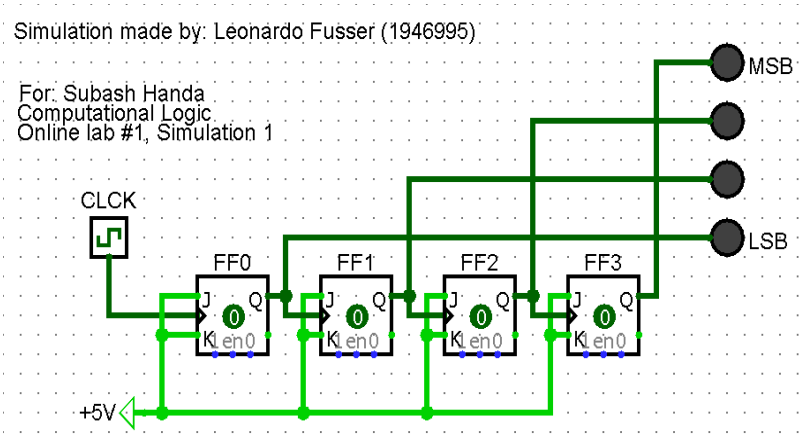
DESIGN

Experiment

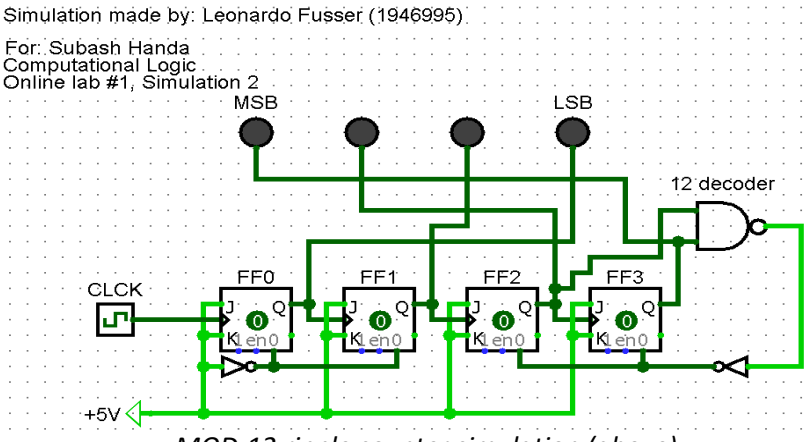
- There were two simulations done in this lab. First, we asked to simulate and verify a 4-bit ripple counter. The second simulation was a MOD-12 (modulus 12) ripple counter. We simulated and verified both simulations with a truth table. The simulations were done in "Logisim". Before this was done, general research was done on asynchronous and asynchronous decade counters. Below outlines the work done in the lab.

SIMULATIONS

Simulations from the Experiment



4-bit ripple counter simulation (above)



MOD-12 ripple counter simulation (above)

4-bit ripple counter truth table

State	Outputs (QA, QB, QC, QD)			
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

MOD-12 ripple counter truth table

State	Outputs (QA, QB, QC, QD)				Decimal Output
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
10	1	0	1	0	10
11	1	0	1	1	11
12	0	0	0	0	Reset *(Recycles back to state "0")*

QUESTIONS

Questions from the Experiment

What is a ripple counter?

- A ripple counter is an asynchronous counter used in digital logic circuits. An asynchronous counter is a type of counter in which each stage is clocked from the output of the preceding stage.

Applications of the ripple counter?

- An example of an application of a ripple counter is in automobile parking control. This counter example illustrates the use of an up/down counter to solve an everyday problem. The problem is to devise a means of monitoring available places in a 100-space parking garage and provide for an indication of a full condition by illuminating a display sign and lowering a gate bar at the entrance. Below explains in greater detail.

A system that solves this problem consists of optoelectronic sensors at the entrance and exit of the garage, an up/down counter and associated circuitry, and an interface circuit that uses the counter output to turn the FULL sign on or off as required and lower or raise the gate bar at the entrance. A general block diagram of this system is shown in Figure 9–51.

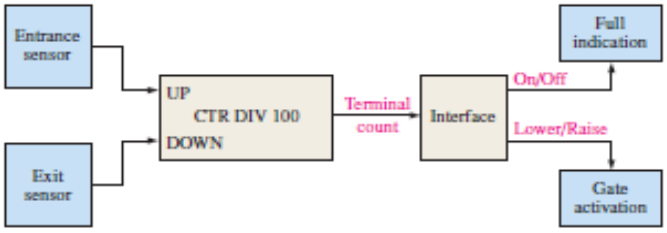


FIGURE 9–51 Functional block diagram for parking garage control.

A logic diagram of the up/down counter is shown in Figure 9–52. It consists of two cascaded up/down decade counters. The operation is described in the following paragraphs.

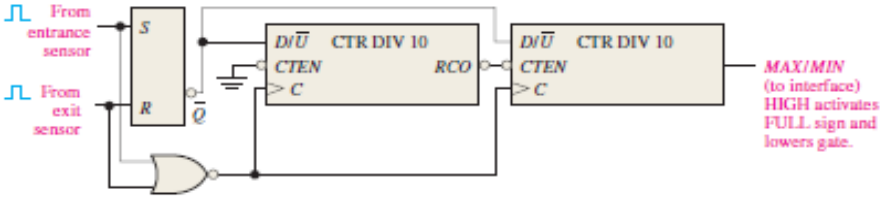


FIGURE 9–52 Logic diagram for modulus-100 up/down counter for automobile parking control.

The counter is initially preset to 0 using the parallel data inputs, which are not shown. Each automobile entering the garage breaks a light beam, activating a sensor that produces an electrical pulse. This positive pulse sets the S-R latch on its leading edge. The LOW on the $\overline{Q}$ output of the latch puts the counter in the UP mode. Also, the sensor pulse goes through the NOR gate and clocks the counter on the LOW-to-HIGH transition of its trailing edge. Each time an automobile enters the garage, the counter is advanced by one (**incremented**). When the one-hundredth automobile enters, the counter goes to its last state (100_{10}). The *MAX/MIN* output goes HIGH and activates the interface circuit (no detail), which lights the FULL sign and lowers the gate bar to prevent further entry.

Incrementing a counter increases its count by one.

When an automobile exits, an optoelectronic sensor produces a positive pulse, which resets the S-R latch and puts the counter in the DOWN mode. The trailing edge of the clock decreases the count by one (**decremented**). If the garage is full and an automobile leaves, the *MAX/MIN* output of the counter goes LOW, turning off the FULL sign and raising the gate.

Decrementing a counter decreases its count by one.

Source: Digital Fundamentals, Eleventh Edition, Thomas L. Floyd, 2015.