Computational Logic Circuits (Online Lab 5)

Decoder with output

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Table of Contents

OBJECTIVES

- To understand the function of decoders.
- To understand how to design a decoder.
- To verify and simulate the function of a 3-bit decoder with a custom output.

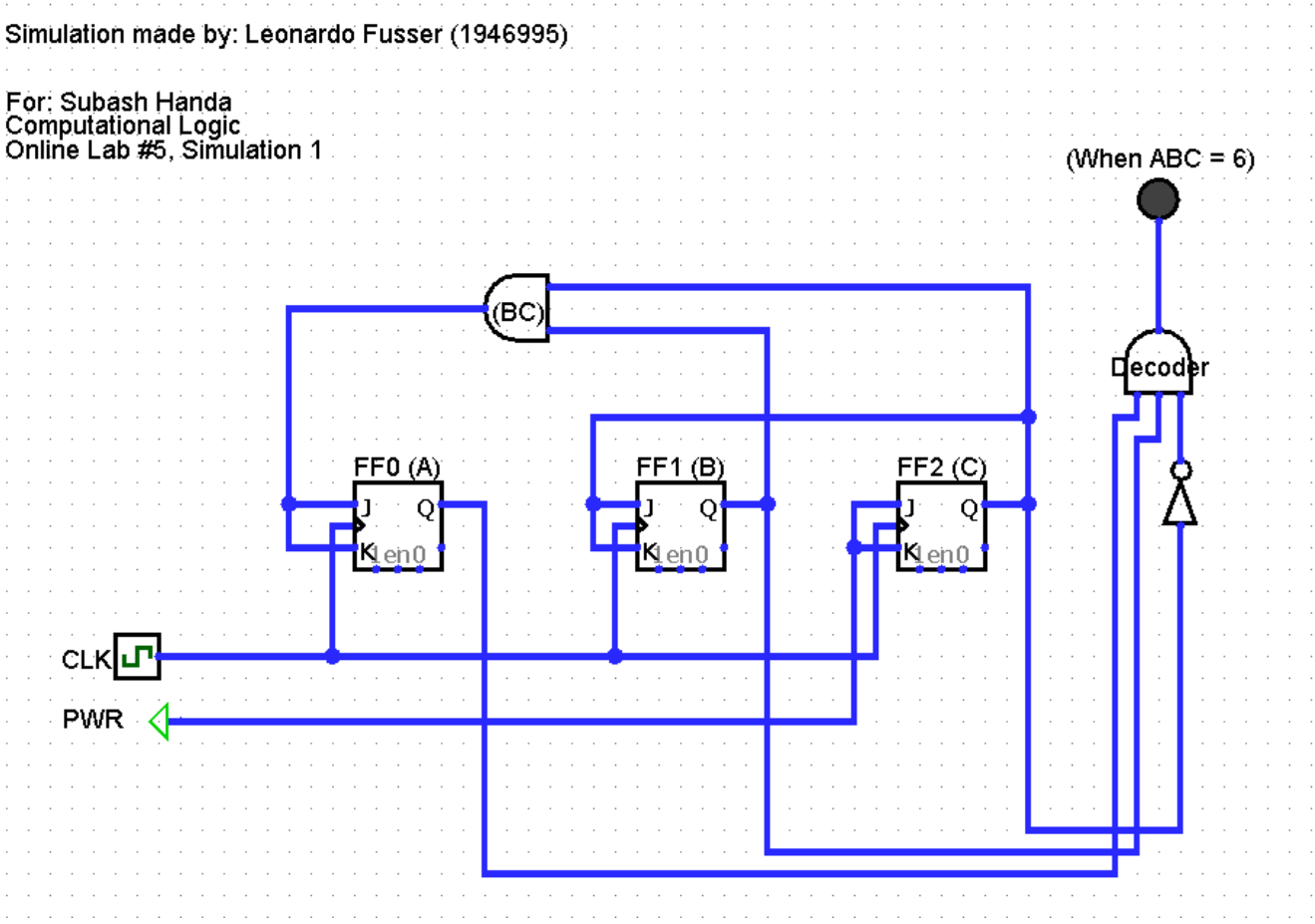
DESIGN

Experiment

- There was one simulation done in this lab. We used the same fundamentals from the last lab. We were asked to create a decoder, where there will be an output (LED) of 1 (on) when the sequence reaches 6 (110), otherwise the output will be 0 (off). The sequence was in 3-bits, so 3 JK flip-flops were used in the simulation (8 states from 000 to 111). Proper design and testing were done as well. The simulations were done in "Logisim". Below outlines the work done in the lab.

SIMULATIONS

Simulations from the Experiment



Decoder with output high when ABC is 6 (above)

Decoder transition table

(Output) Z	(PRESENT)			(NEXT)			J-K Flip Flops		
	A_N	B_N	C_N	A_{N+1}	B_{N+1}	C_{N+1}	JA/KA	JB/KB	JC/KC
0	0	0	0	0	0	1	0 X	0 X	1 X
0	0	0	1	0	1	0	0 X	1 X	X 1
0	0	1	0	0	1	1	0 X	X 0	1 X
0	0	1	1	1	0	0	1 X	X 1	X 1
0	1	0	0	1	0	1	X 0	0 X	1 X
0	1	0	1	1	1	0	X 0	1 X	X 1
1	1	1	0	1	1	1	X 0	X 0	1 X
0	1	1	1	0	0	0	X 1	X 1	X 1

FF0: output = A

FF1: output = B

FF2: output = C

Decoder k-maps

A\BC	*00*	*01*	*11*	*10*
0	0	0	1	0
1	X	X	X	X

JA = (BC)

A\BC	*00*	*01*	*11*	*10*
0	X	X	X	X
1	0	0	1	0

KA = (BC)

A\BC	*00*	*01*	*11*	*10*
0	0	1	X	X
1	0	1	X	X

JB = (C)

A\BC	*00*	*01*	*11*	*10*
0	X	X	1	0
1	X	X	1	0

KB = (C)

A\BC	*00*	*01*	*11*	*10*
00	1	X	X	1
01	1	X	X	1

JC = (1)

A\BC	*00*	*01*	*11*	*10*
00	X	1	1	X
01	X	1	1	X

KC = (1)

A\BC	*00*	*01*	*11*	*10*
0	0	0	0	0
1	0	0	0	1

Z = (ABC')

Decoder state diagram