Gates (Lab 4)

More complex experiments with Logic Gates

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OBJECTIVES

- To further enhance understanding with ICs.
- To further enhance understanding with logic gates.
- To further enhance understanding with the pencil box.

DESIGN

Experiment 4a

- Experiment 4a consisted of checking for proper connections on the ICs for the next experiments (4b, 4c & 4d) in the pencil box and reminded that XOR and XNOR gate are short for exclusive OR and exclusive NOR respectively.

Experiment 4b

- Experiment 4b consisted of taking four NAND gates and manipulating them to behave similar to an exclusive OR (XOR) gate. This comes in handy when there are no XOR gates and only NAND gates are available. Below is the truth table simulating this function. Refer to logic design #1 under Schematics for reference.

a	b	XOR
0	0	0
0	1	1
1	0	1
1	1	0

Experiment 4c

- Experiment 4b consisted of taking five NAND gates and manipulating them to behave similar to an exclusive NOR (XNOR) gate. This comes in handy when there are no XNOR gates and only NAND gates are available. Below is the truth table simulating this function. Refer to logic design #2 under Schematics for reference.

a	b	XNOR
0	0	0
0	1	0
1	0	0
1	1	1

Experiment 4d

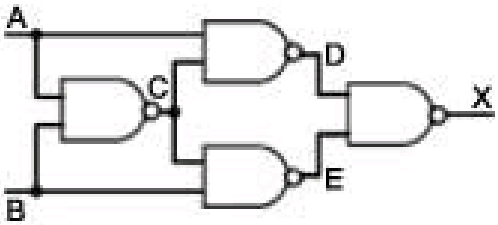
- Experiment 4c consisted of testing our knowledge on gates but also introduced us to the procedures of wiring schematics. The following schematic consists of XOR, NOR, NAND and AND gates. Below is the truth table simulating the schematic created using these gates. Refer to logic design #3 under Schematics for reference.

A (s0)	B (s1)	C (s2)	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

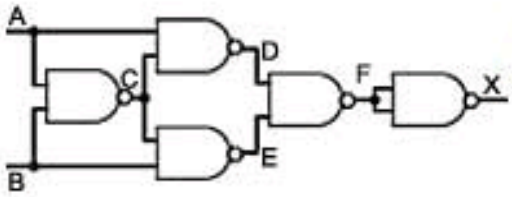
What is the output of this circuit?
F = (A+B)(A+B)(A*B*C)(A*B*C)

SCHEMATICS

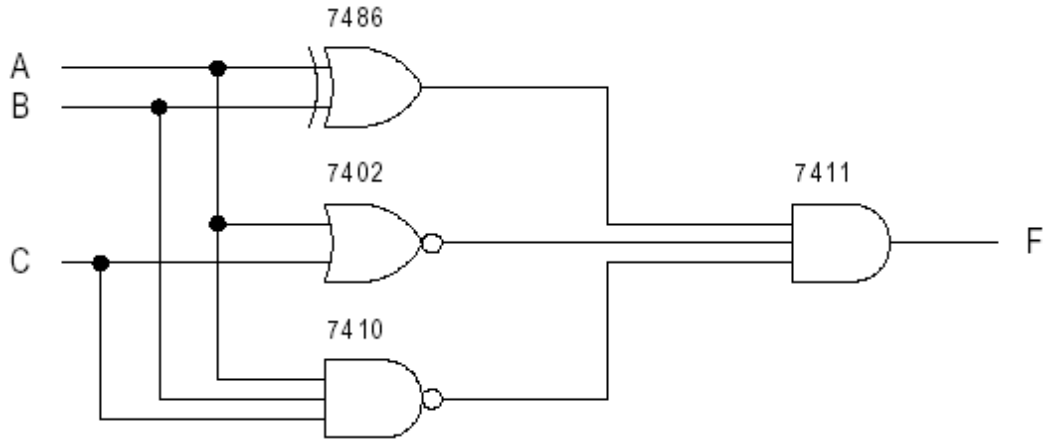
Logic Design #1



Logic Design #2

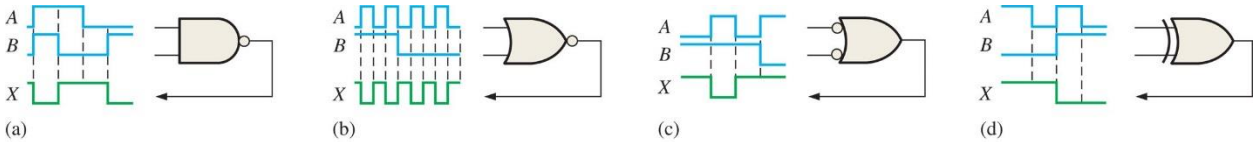


Logic Design #3



QUESTIONS

Determine the faulty gates in Figure 2 by analyzing the timing diagrams



- (a) is not faulty.
- (b) is not faulty.
- (c) is not faulty.
- (d) is faulty.

[truth table from (d)]

a	b	XOR
0	0	1
1	1	0

[correct truth table for (d)]

a	b	XOR
0	0	0
1	1	0