Computational Logic Circuits (Lab 5)

zyBooks & odd/even parity checker

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OBJECTIVES

- To understand the topics covered in zyBooks for this week's lab.
- To design and implement a 9-bit odd/even parity checker using XOR gates.
- Understand 74180 and 74280 chips.

DESIGN

Experiment

- There were two parts in this lab. First, we asked to read from chapter 5.1 to 5.3 in our zyBooks. Then, we had to observe the output of a 9-bit parity checker using only XOR gates. We had our instructor verify our circuit. Before this was done, general research was done to determine what a parity bit, parity checker and chip was. Below outlines the work done in the lab.

SCHEMATICS

Schematics from the Experiment

The schematic for the 9-bit parity checker is on the attached paper of this report.

QUESTIONS

Questions from the Experiment

What is a parity bit?

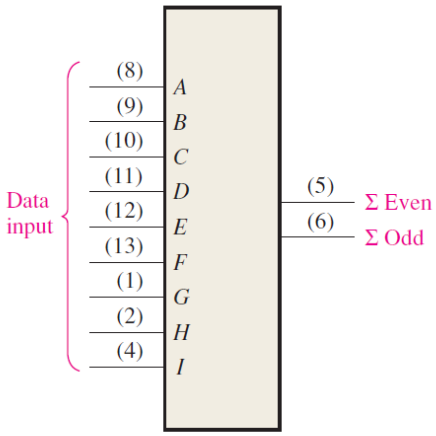
- A parity bit indicates if the number of 1s in a code is even or odd for the purpose of error detection.

What is a parity checker?

- A parity checker is the process that ensures accurate data transmission between nodes during communication.

What are the functions of the 74280 chips?

- This particular device can be used to check for odd or even parity on a 9-bit code (eight data bits and one parity bit), or it can be used to generate a parity bit for a binary code with up to nine bits. The inputs are *A* through *I*; when there is an even number of 1s on the inputs, the ∑ Even output is HIGH and the ∑ Odd output is LOW.



(a) Traditional logic symbol

Number of Inputs *A–I* that Are High	Outputs Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

(b) Function table

Source: Digital Fundamentals, Eleventh Edition, Thomas L. Floyd, 2015.