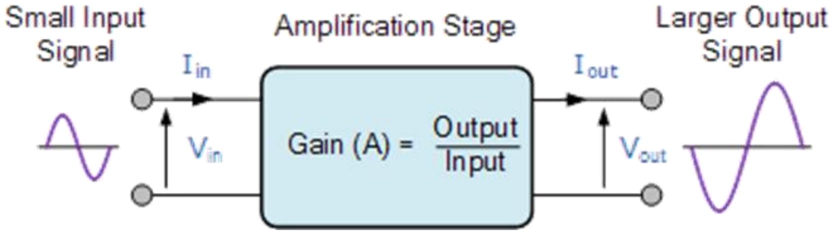
ITMO

# Introduction to the Amplifier


Nikolay Nikolaev (nanikolaev@itmo.ru)
Nikolai Poliakov (polyakov_n_a@itmo.ru)

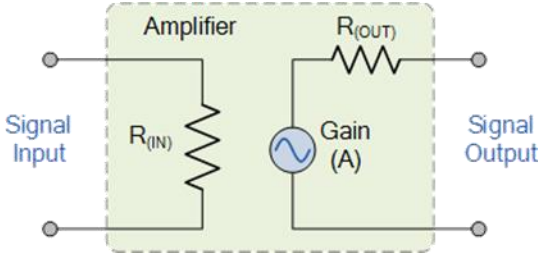
# Introduction to the Amplifier




$$Voltage\,Gain\,(A_v) = \frac{Output\ Voltage}{Input\ Voltage} = \frac{Vout}{Vin}$$

$$Current\,Gain\,(A_i) = \frac{Output\ Current}{Input\ Current} = \frac{Iout}{Iin}$$

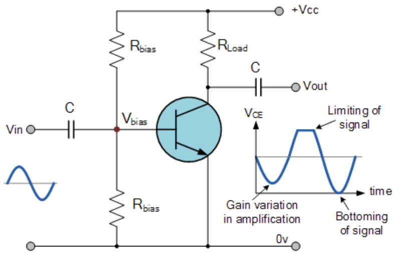
$$Power\,Gain\,(A_p) = A_v\ x\ A_i$$

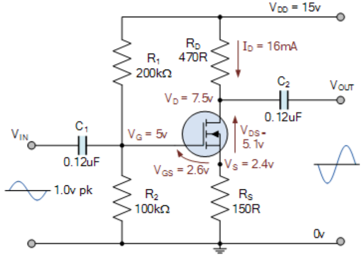



Voltage Gain in dB: $a_v = 20\,log(A_v)$

Current Gain in dB: $a_i = 20\,log(A_i)$

Power Gain in dB: $a_p = 10\,log\left(A_p\right)$



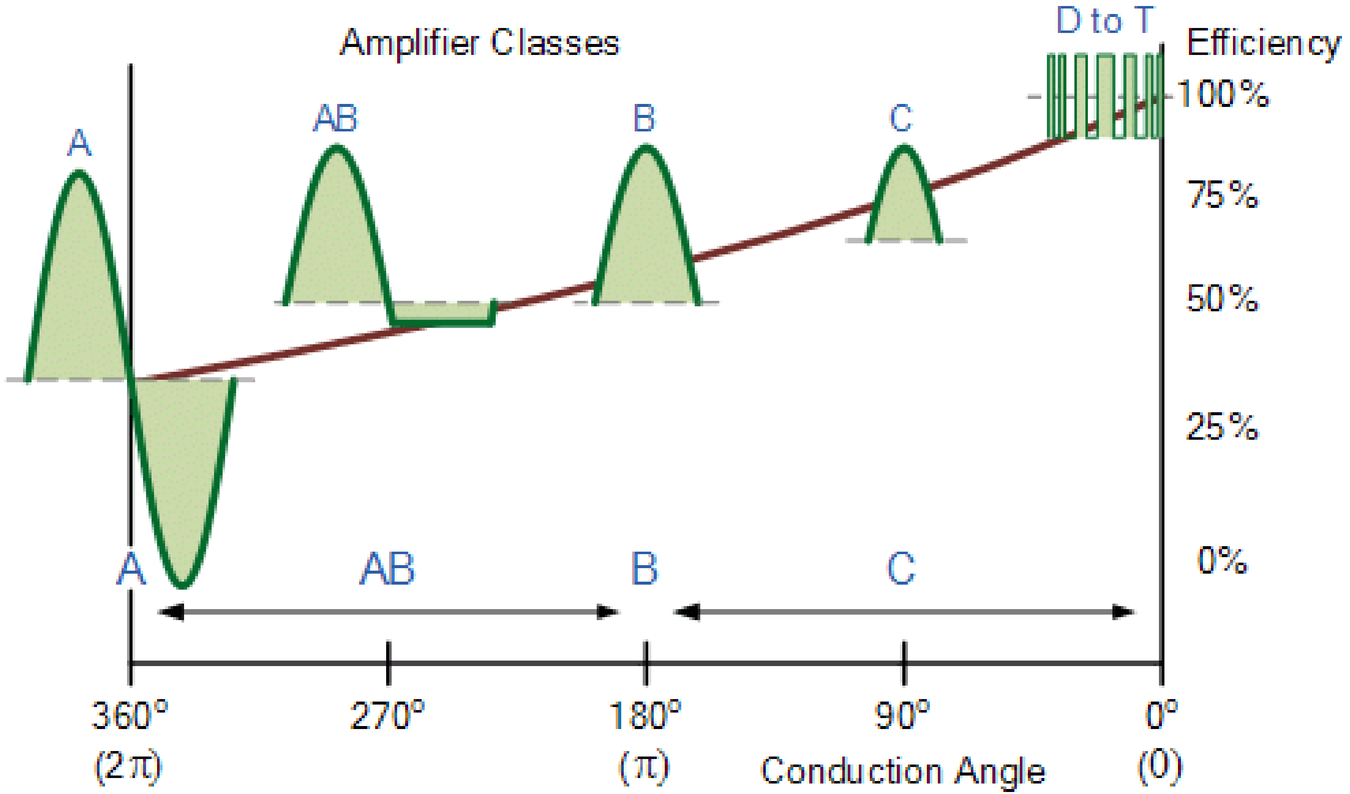
# Classification of Signal Amplifier

| Type of Signal | Type of Configuration | Classification | Frequency of Operation |
|---|---|---|---|
| Small Signal | Common Emitter | Class A Amplifier | Direct Current (DC) |
| Large Signal | Common Base | Class B Amplifier | Audio Frequencies (AF) |
| | Common Collector | Class AB Amplifier | Radio Frequencies (RF) |
| | | Class C Amplifier | VHF, UHF and SHF Frequencies |

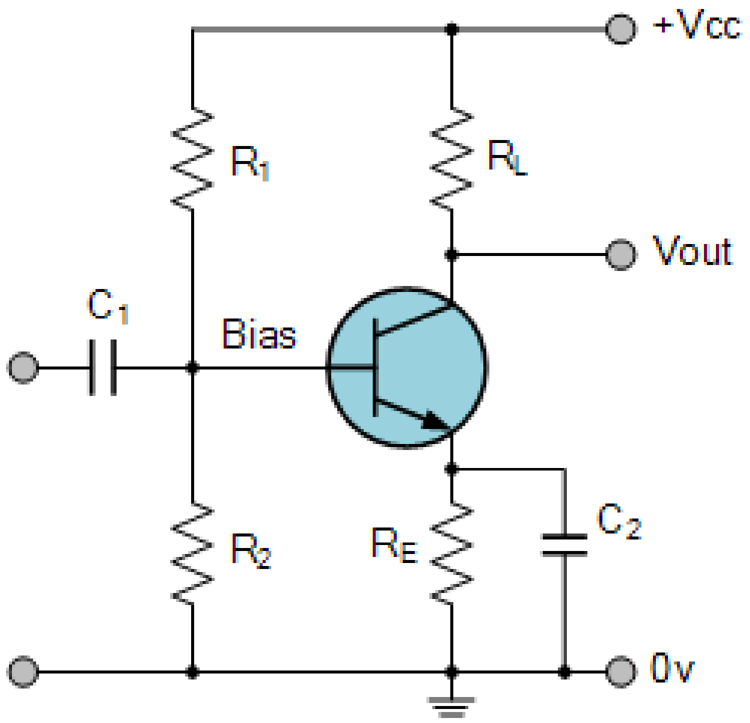
# Ideal Amplifier

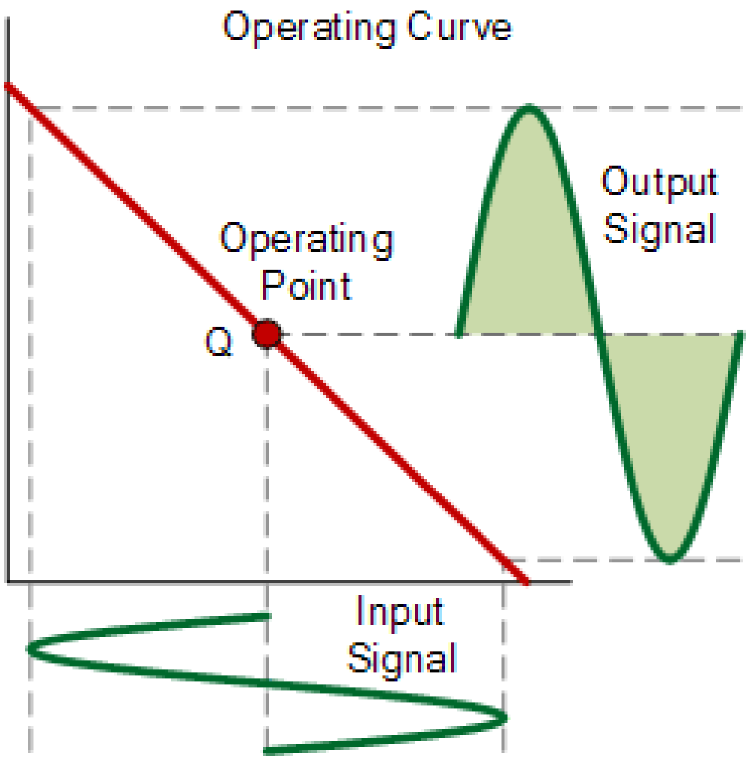
- ✓ The amplifiers gain, ( A ) should remain constant for varying values of input signal.
- ✓ Gain is not be affected by frequency. Signals of all frequencies must be amplified by exactly the same amount.
- ✓ The amplifiers gain must not add noise to the output signal. It should remove any noise that is already exists in the input signal.
- ✓ The amplifiers gain should not be affected by changes in temperature giving good temperature stability.
- ✓ The gain of the amplifier must remain stable over long periods of time.

# Amplifier Classes

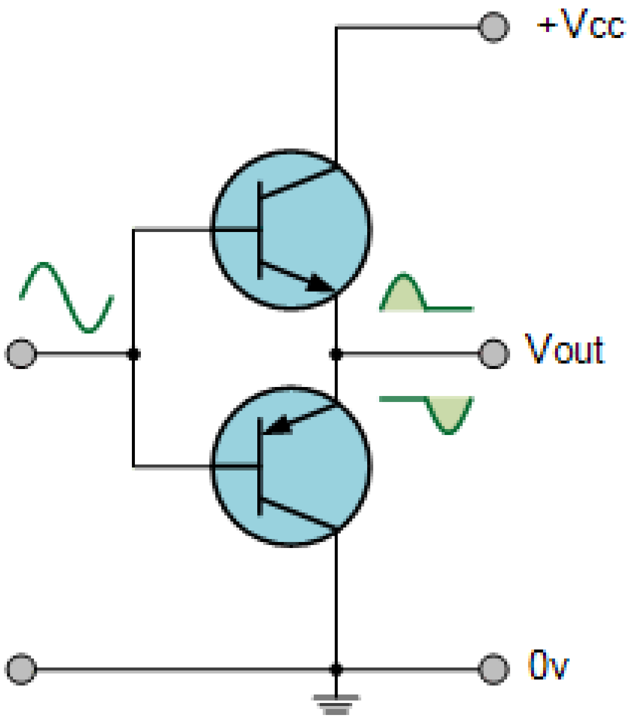


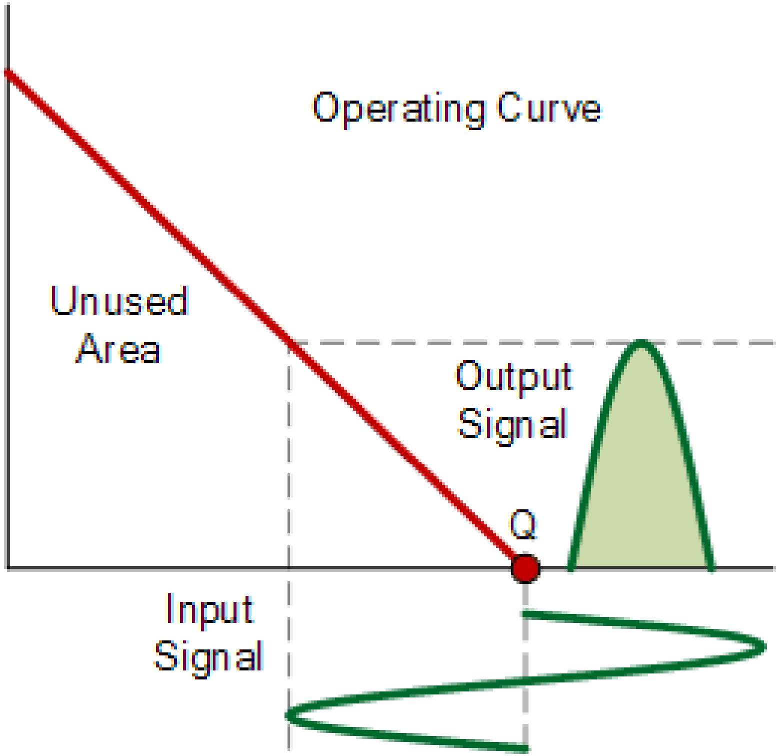
# Class A Amplifier



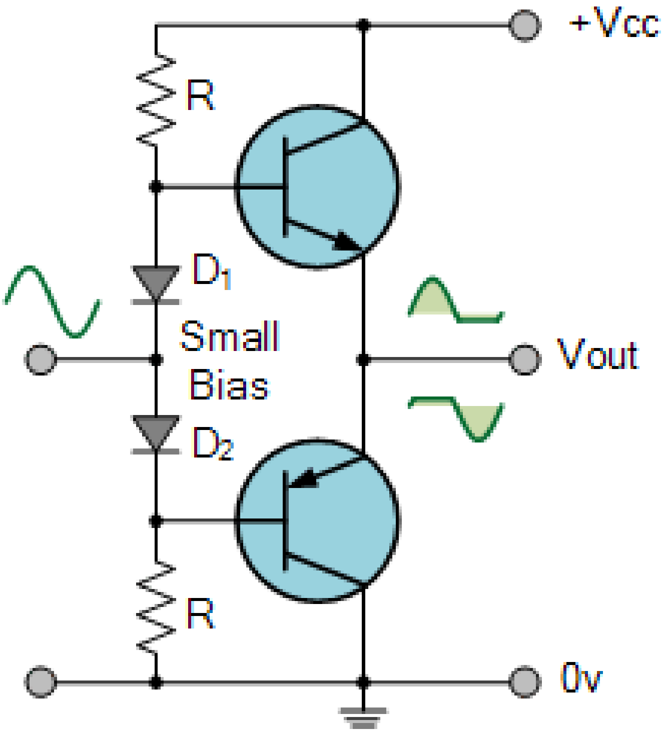



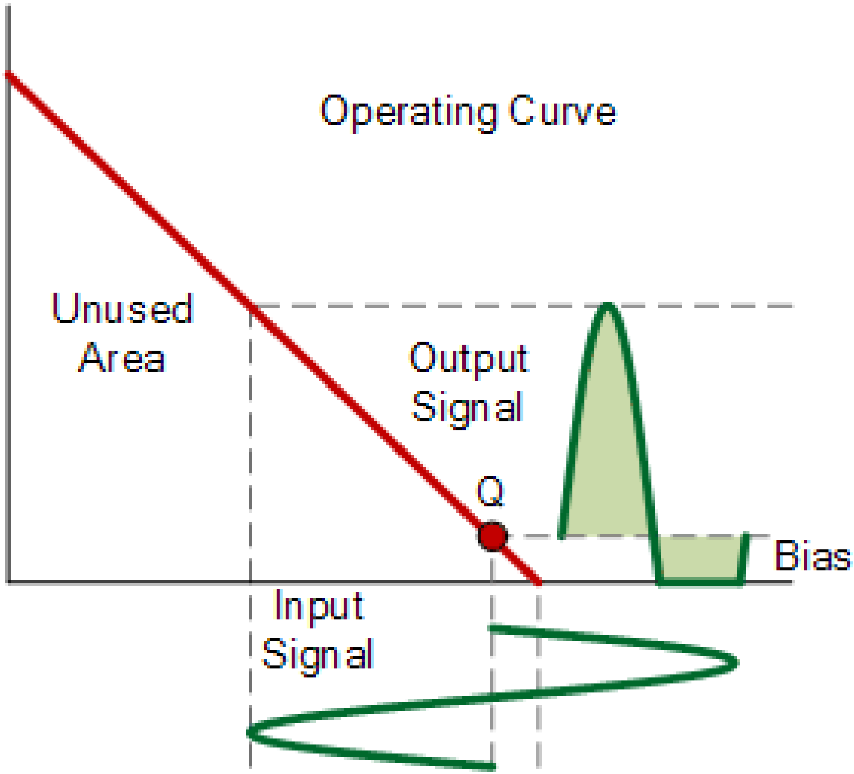
# Class B Amplifier



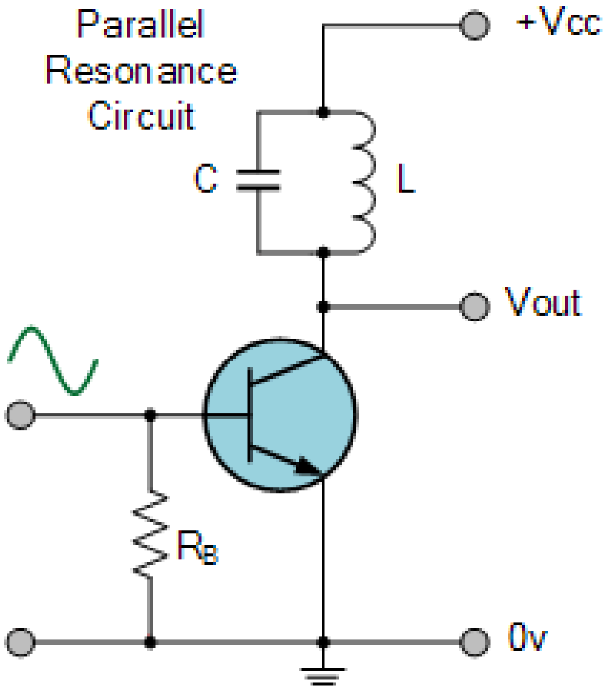



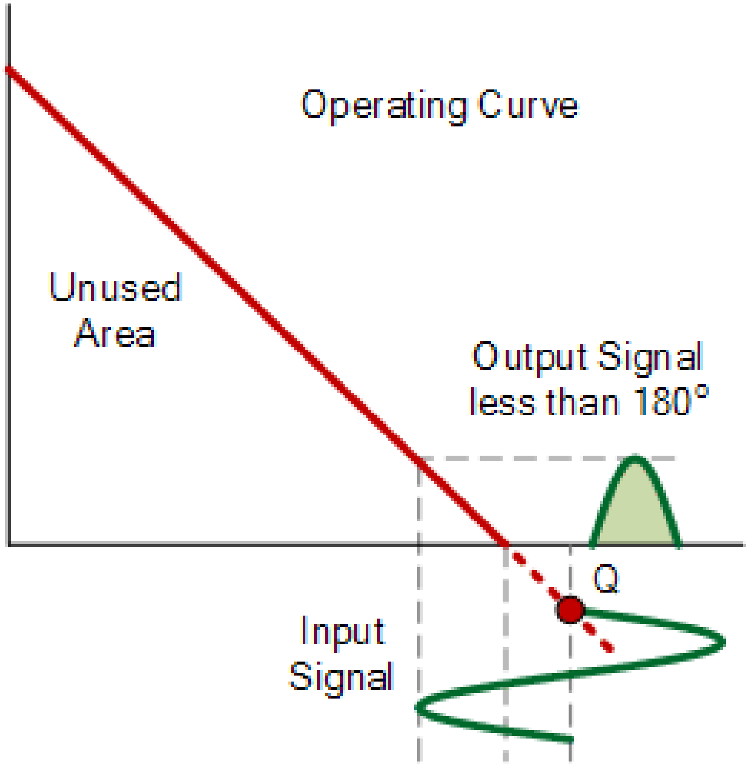
# Class AB Amplifier



# Class C Amplifier



# Other Common Amplifier Classes

- Class D Amplifier – A Class D audio amplifier is basically a non-linear switching amplifier or PWM amplifier. Class-D amplifiers theoretically can reach 100% efficiency, as there is no period during a cycle were the voltage and current waveforms overlap as current is drawn only through the transistor that is on.
- Class F Amplifier – Class-F amplifiers boost both efficiency and output by using harmonic resonators in the output network to shape the output waveform into a square wave. Class-F amplifiers are capable of high efficiencies of more than 90% if infinite harmonic tuning is used.
- Class G Amplifier – Class G offers enhancements to the basic class AB amplifier design. Class G uses multiple power supply rails of various voltages and automatically switches between these supply rails as the input signal changes. This constant switching reduces the average power consumption, and therefore power loss caused by wasted heat.
- Class I Amplifier – The class I amplifier has two sets of complementary output switching devices arranged in a parallel push-pull configuration with both sets of switching devices sampling the same input waveform. One device switches the positive half of the waveform, while the other switches the negative half similar to a class B amplifier. With no input signal applied, or when a signal reaches the zero crossing point, the switching devices are both turned ON and OFF simultaneously with a 50% PWM duty cycle cancelling out any high frequency signals.

# Other Common Amplifier Classes

•Class S Amplifier – A class S power amplifier is a non-linear switching mode amplifier similar in operation to the class D amplifier. The class S amplifier converts analogue input signals into digital square wave pulses by a delta-sigma modulator, and amplifies them to increases the output power before finally being demodulated by a band pass filter. As the digital signal of this switching amplifier is always either fully “ON” or “OFF” (theoretically zero power dissipation), efficiencies reaching 100% are possible.

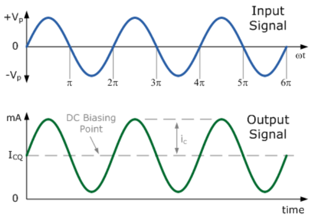
•Class T Amplifier – The class T amplifier is another type of digital switching amplifier design. Class T amplifiers are starting to become more popular these days as an audio amplifier design due to the existence of digital signal processing (DSP) chips and multi-channel surround sound amplifiers as it converts analogue signals into digital pulse width modulated (PWM) signals for amplification increasing the amplifiers efficiency. Class T amplifier designs combine both the low distortion signal levels of class AB amplifier and the power efficiency of a class D amplifier.

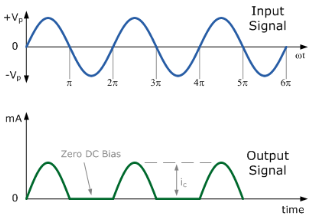
# Amplifier Class by Conduction Angle

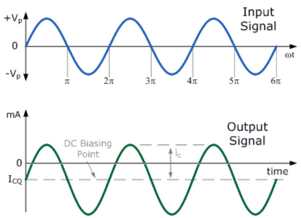
| Amplifier Class | Description | Conduction Angle |
|---|---|---|
| Class-A | Full cycle 360º of Conduction | $\theta = 2\pi$ |
| Class-B | Half cycle 180º of Conduction | $\theta = \pi$ |
| Class-AB | Slightly more than 180º of conduction | $\pi < \theta < 2\pi$ |
| Class-C | Slightly less than 180º of conduction | $\theta < \pi$ |
| Class-D to T | ON-OFF non-linear switching | $\theta = 0$ |

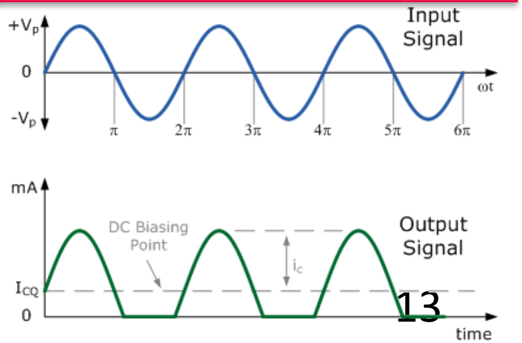
# Power Amplifier Classes

| Class | A | B | C | AB |
|---|---|---|---|---|
| Conduction Angle | 360º | 180º | Less than 90º | 180 to 360º |
| Position of the Q-point | Centre Point of the Load Line | Exactly on the X-axis | Below the X-axis | In between the X-axis and the Centre Load Line |
| Overall Efficiency | Poor 25 to 30% | Better 70 to 80% | Higher than 80% | Better than A but less than B 50 to 70% |
| Signal Distortion | None if Correctly Biased | At the X-axis Crossover Point | Large Amounts | Small Amounts |

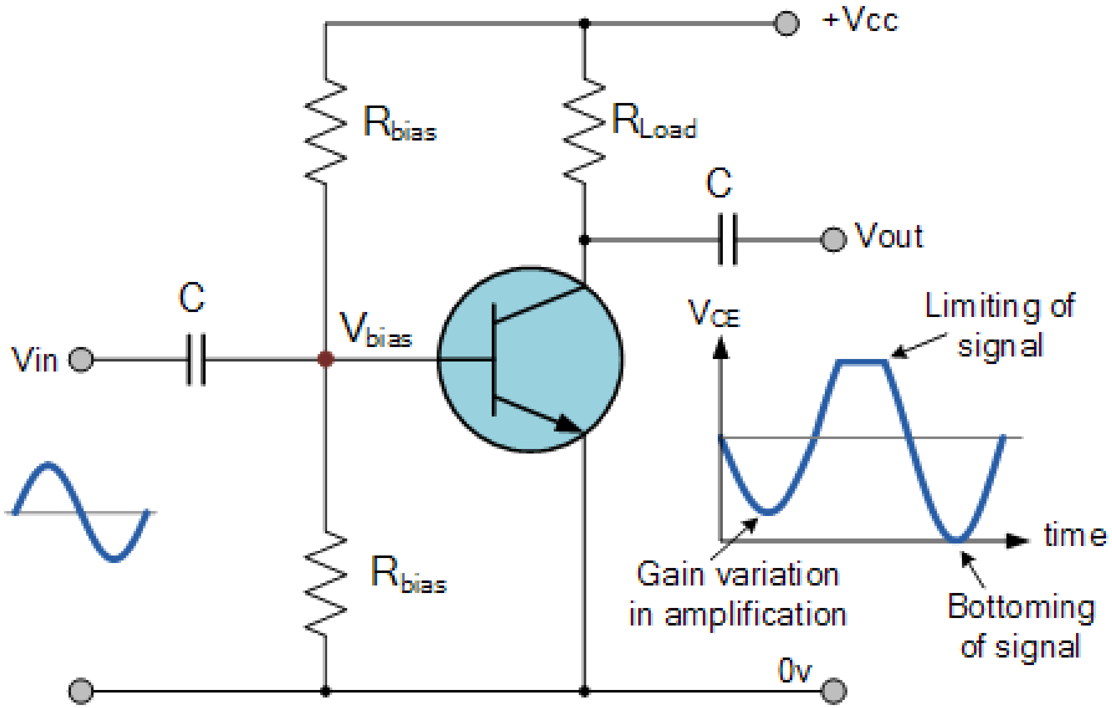


# Common Emitter Amplifier



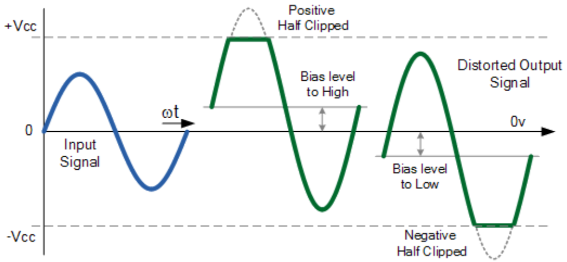

Distortion of the output signal waveform may occur because:

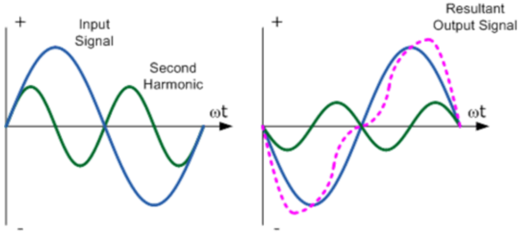
- ✓ Amplification may not be taking place over the whole signal cycle due to incorrect biasing levels.
- ✓ The input signal may be too large, causing the amplifiers transistors to be limited by the supply voltage.
- ✓ The amplification may not be a linear signal over the entire frequency range of inputs.

# Amplifier Distortion

Distortion of the output signal waveform may occur because:

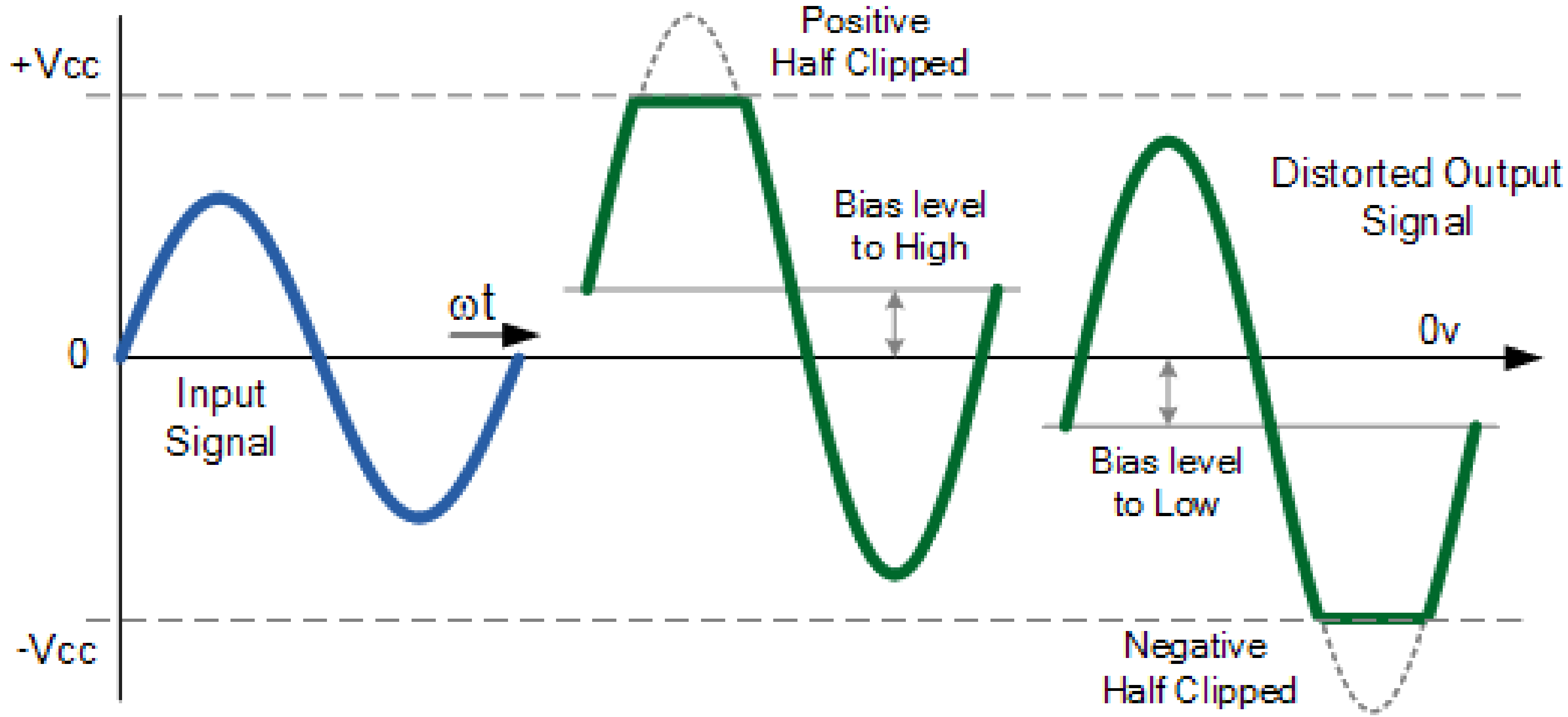
- ✓ Amplification may not be taking place over the whole signal cycle due to incorrect biasing levels.
- ✓ The input signal may be too large, causing the amplifiers transistors to be limited by the supply voltage.
- ✓ The amplification may not be a linear signal over the entire frequency range of inputs.



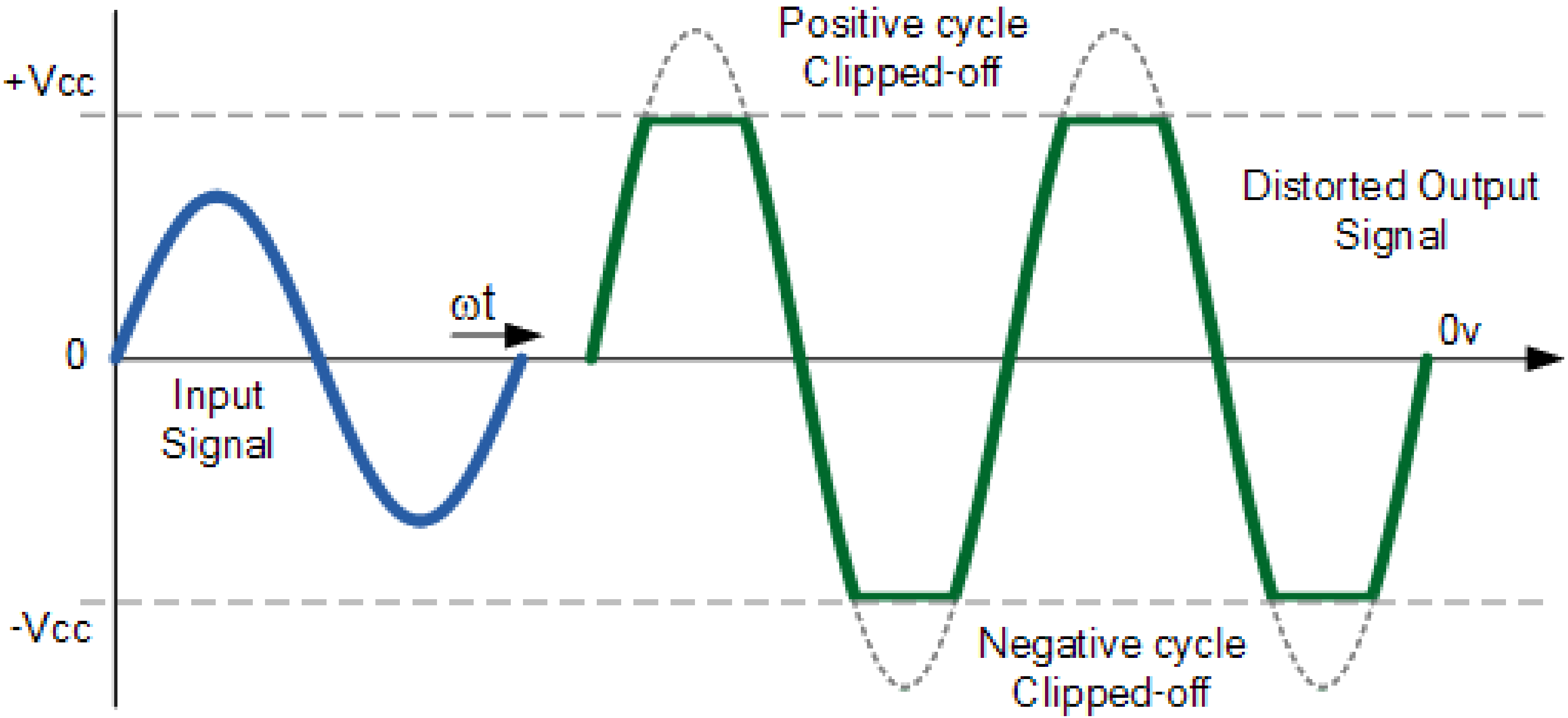




<u>This means then that during the amplification process of the signal waveform, some form of Amplifier Distortion has occurred.</u>

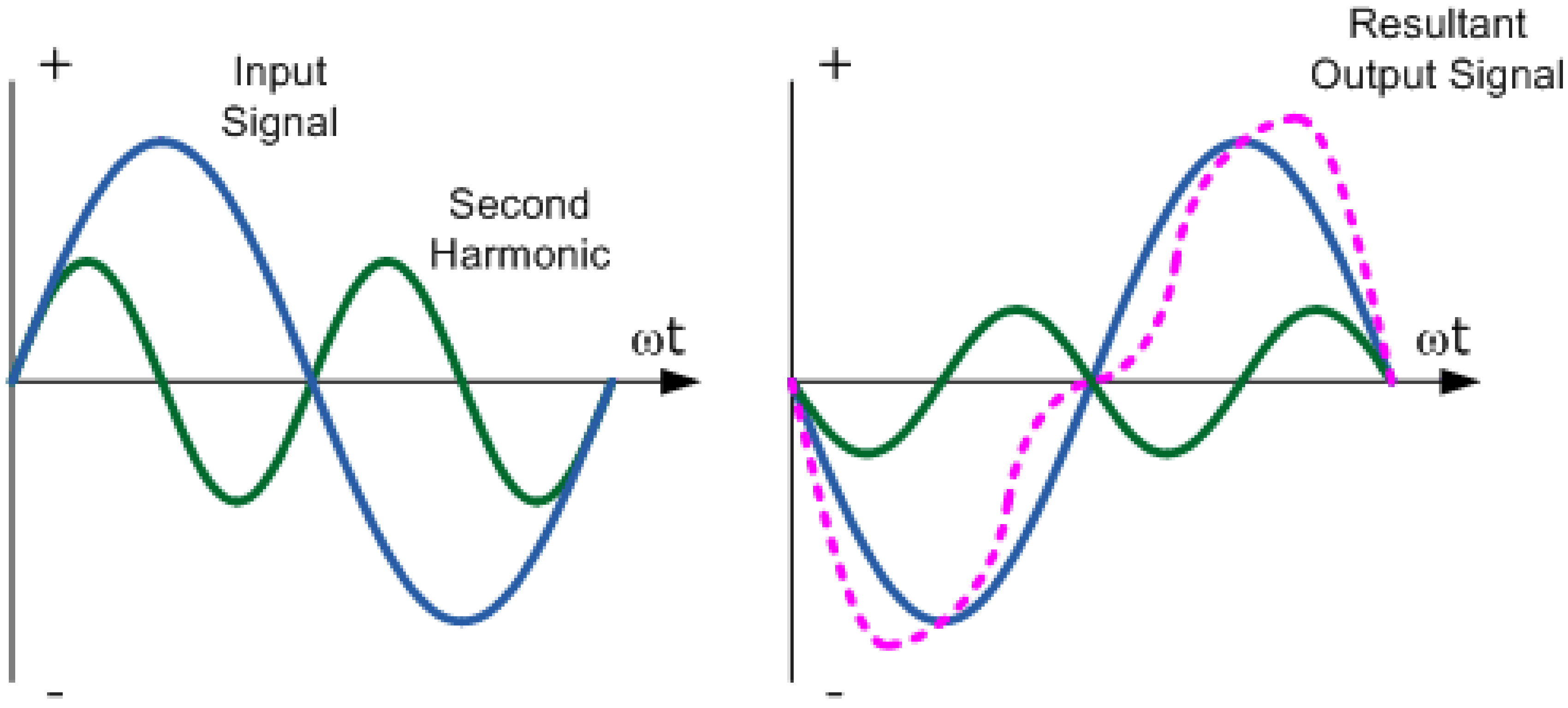
# Amplitude Distortion due to Incorrect Biasing



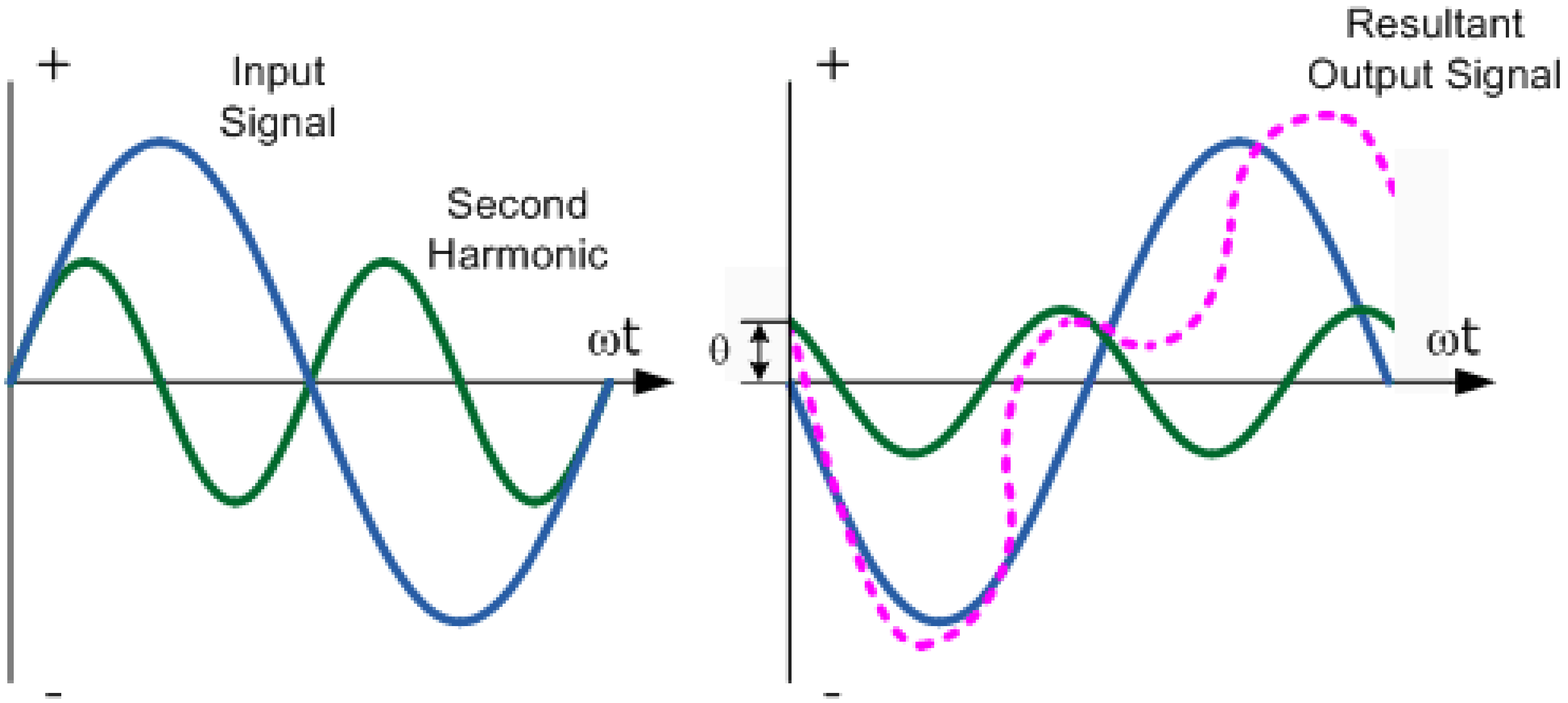
# Amplitude Distortion due to Clipping



# Frequency Distortion due to Harmonics

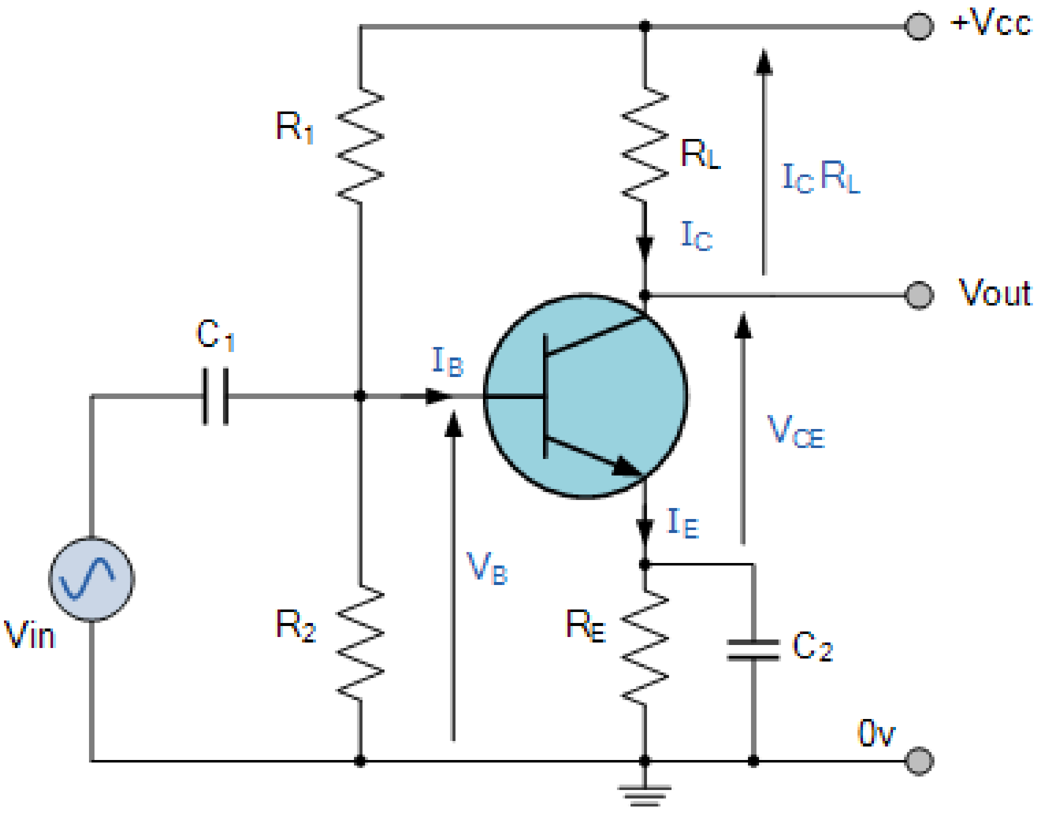


# Phase Distortion due to Delay



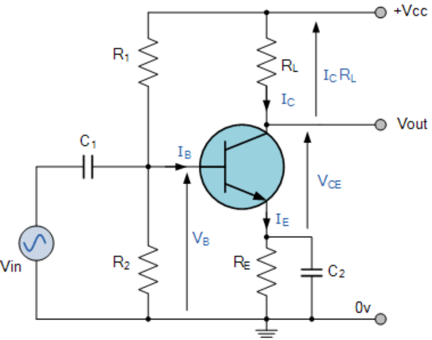
# Common Emitter Amplifier

# Common Emitter Amplifier



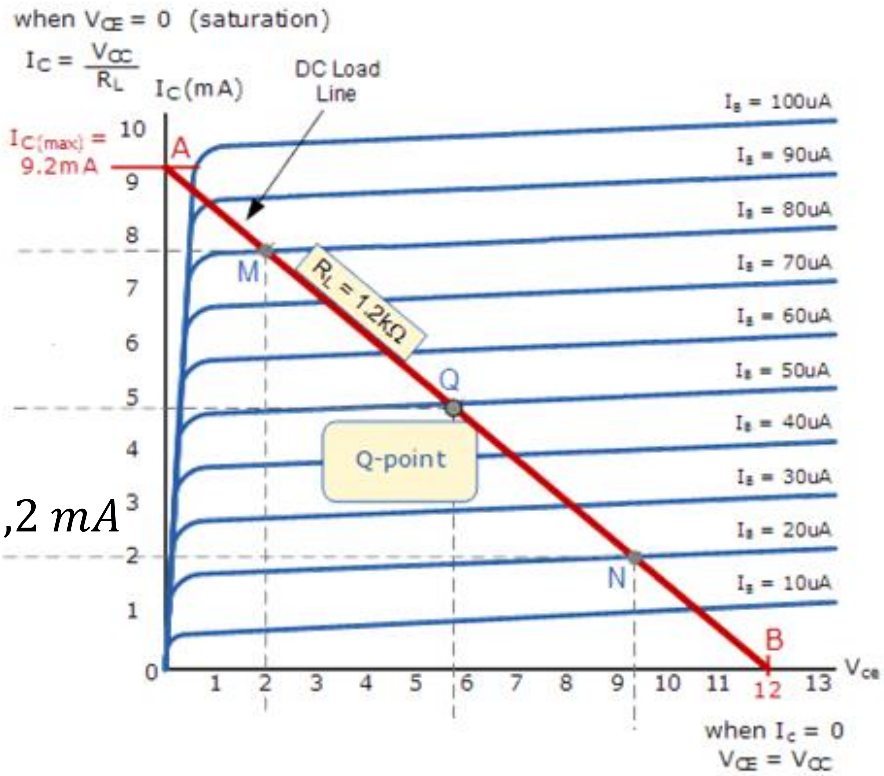

*If*

$$V_{CC} = 12\ V$$
$$V_{RE} = 1\ V$$
$$R_L = 1200\ \Omega$$
$$\beta = 100$$




*If*

$$V_{CC} = 12\ V$$
$$V_{RE} = 1\ V$$
$$R_L = 1200\ \Omega$$



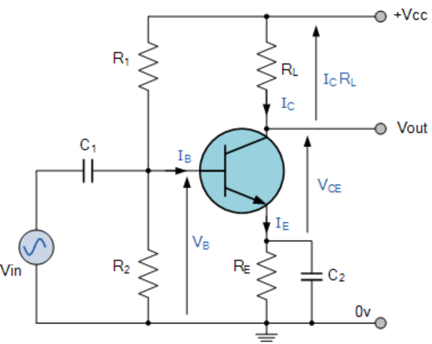

Load line $$V_{CC} = V_{CE} + I_C R_L + V_{RE}$$

$$V_{CC} = 0$$

Saturation (A) $$I_{Cmax} = \frac{V_{CE} - V_{RE}}{R_L} = \frac{12 - 1}{1200} = 9{,}2\ mA$$

Cut-off (B) $$I_C = 0, \Rightarrow V_{RE} = 0V$$
$$V_{CE} = V_{CC}$$

# Common Emitter Amplifier




Q-point

*If*

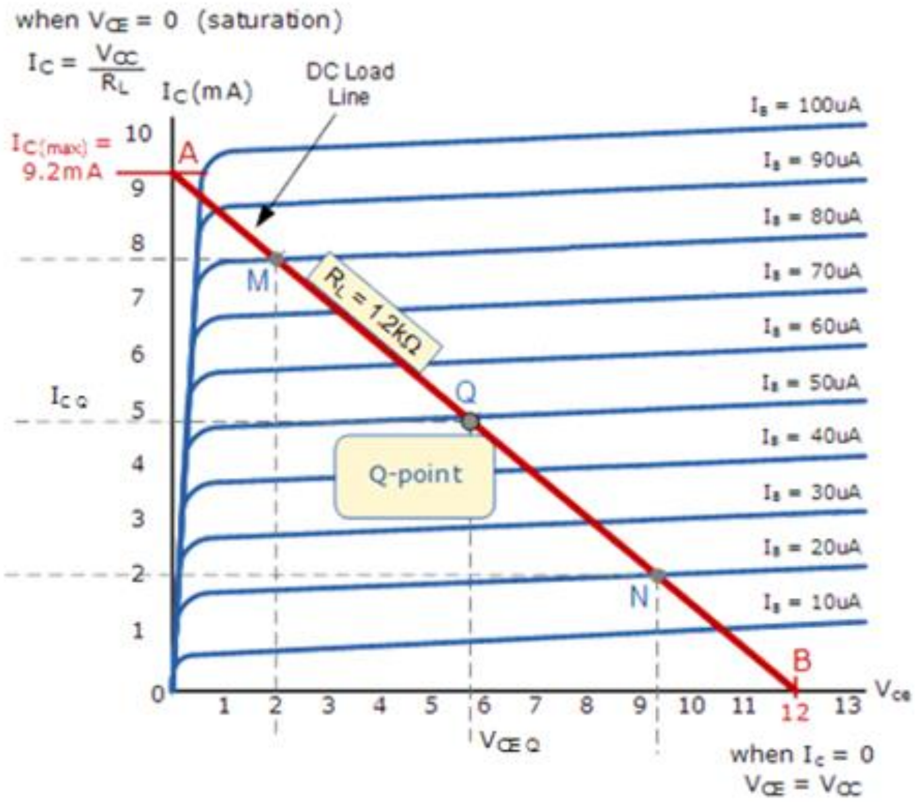
$$V_{CC} = 12\ V$$
$$V_{RE} = 1\ V$$
$$R_L = 1200\ \Omega$$

$$I_{CQ} = \frac{V_{CC} - V_{RE}/2}{R_L}$$

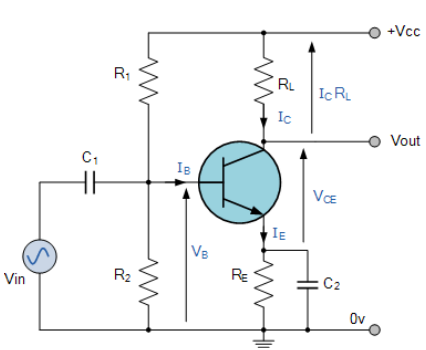
$$I_{CQ} = \frac{12 - 1/2}{1200} = 4{,}58\ mA$$

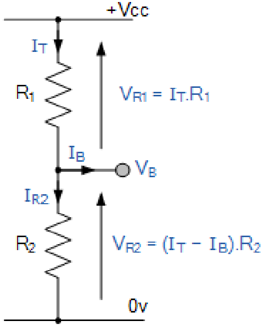
$$I_C = \beta * I_B \Rightarrow I_B = \frac{I_C}{\beta}$$

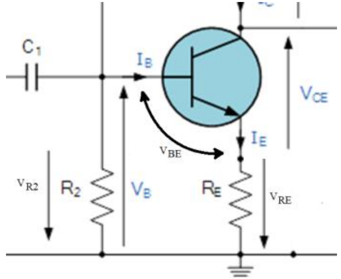
$$I_B = \frac{4{,}58}{100} = 45{,}8\ \mu A$$



# Common Emitter Amplifier



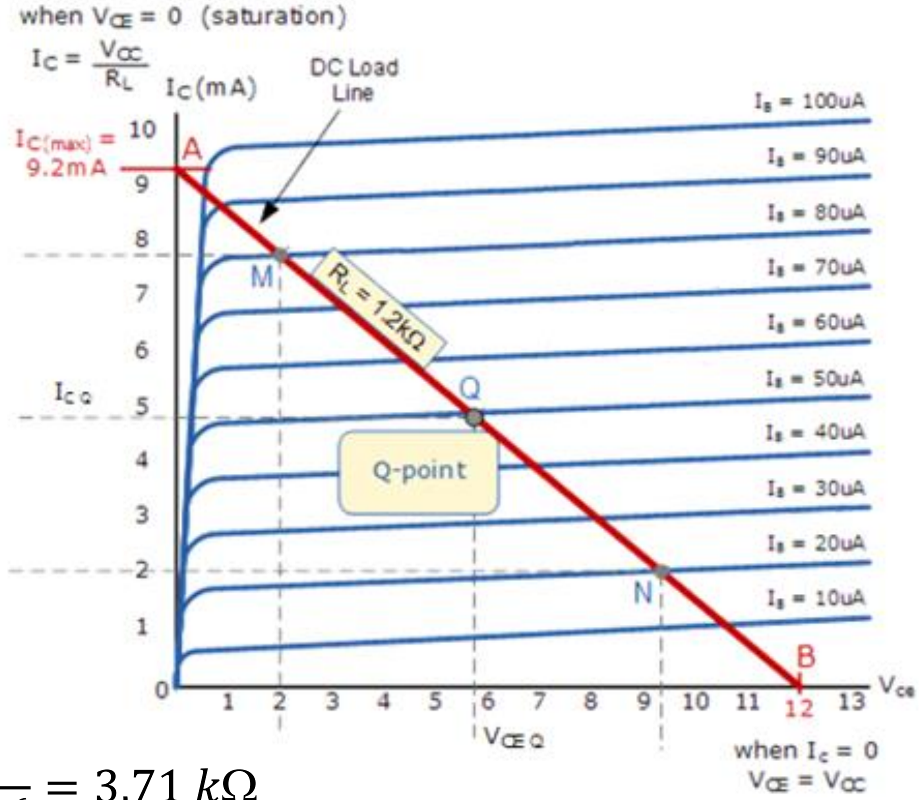

$$V_{R2} = V_{BE} + V_{RE}$$

$$I_{R2} * R_2 = V_{BE} + V_{RE}$$

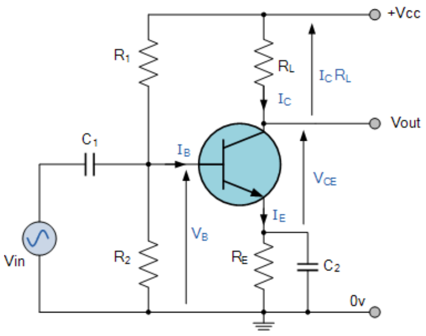
$$I_{R2} \geq 10 * I_B$$

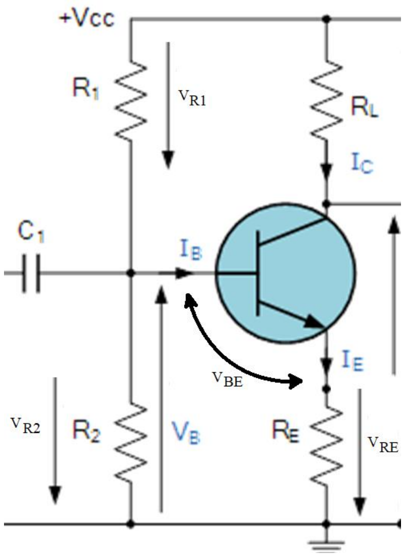
$$10 I_B * R_2 = V_{BE} + V_{RE}$$

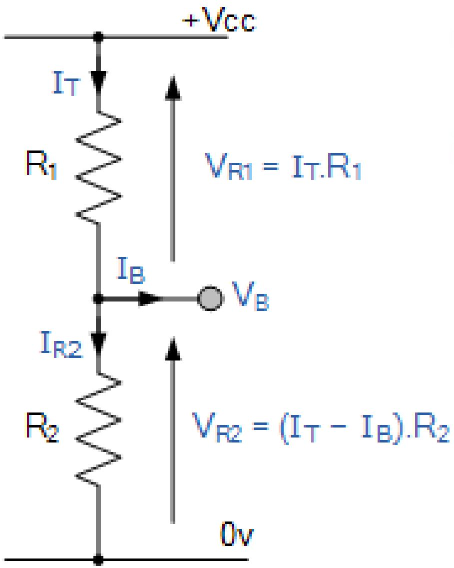
$$R_2 = \frac{V_{BE}+V_{RE}}{10 I_B} = \frac{0.7+1}{10*45{,}8*10^{-6}} = 3{,}71\ k\Omega$$

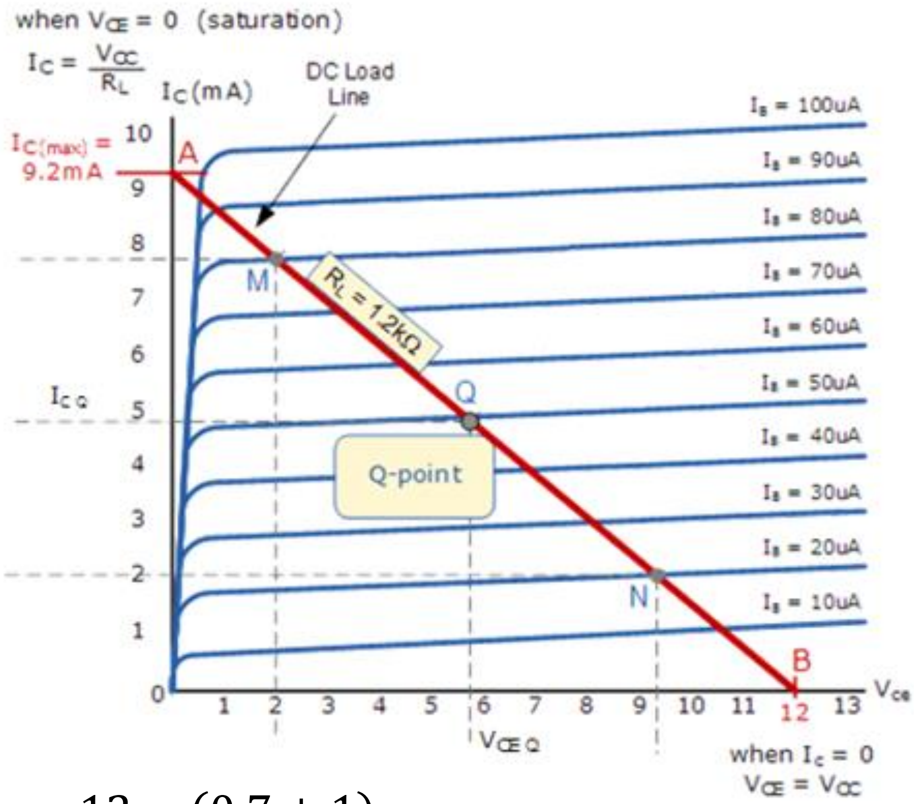


# Common Emitter Amplifier



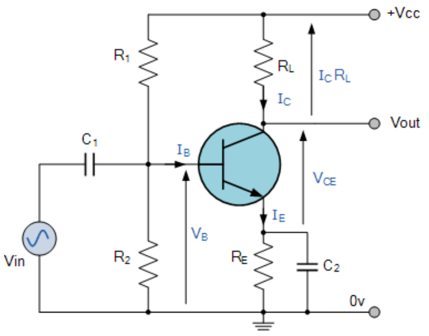



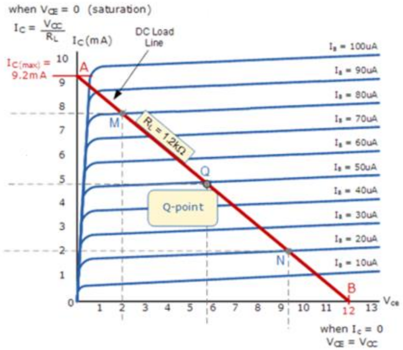

$$I_{R2} \geq 10 * I_B$$

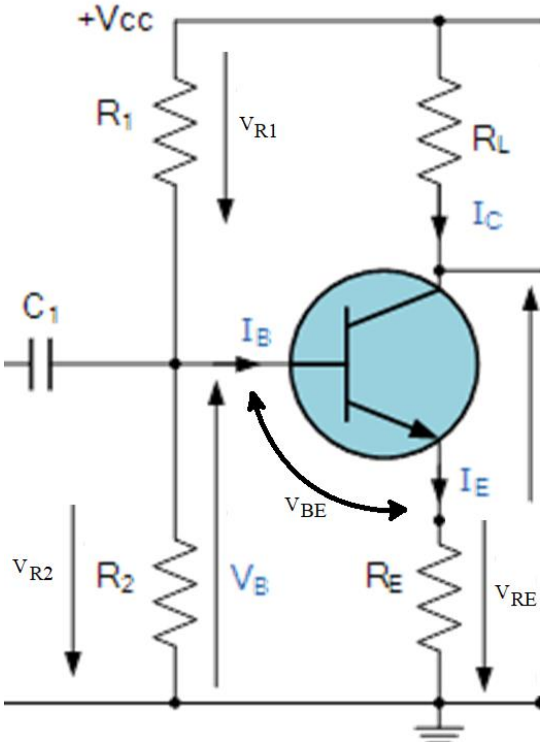
$$I_{R1} \geq I_{R2} + I_B = 11 * I_B$$

$$R_1 = \frac{V_{CC} - (V_{BE} + V_{RE})}{11 I_B} = \frac{12 - (0.7 + 1)}{11 * 45{,}8 * 10^{-6}} = 20{,}45\ k\Omega$$

# Common Emitter Amplifier



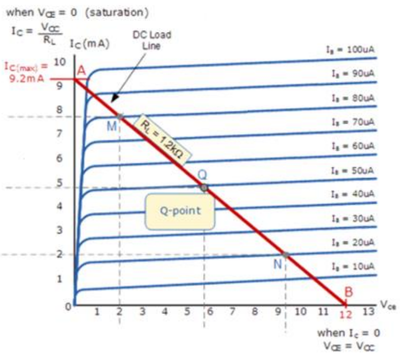

$$R_E = \frac{V_{RE}}{I_{RE}}$$

$$R_E = \frac{V_{RE}}{I_E}$$

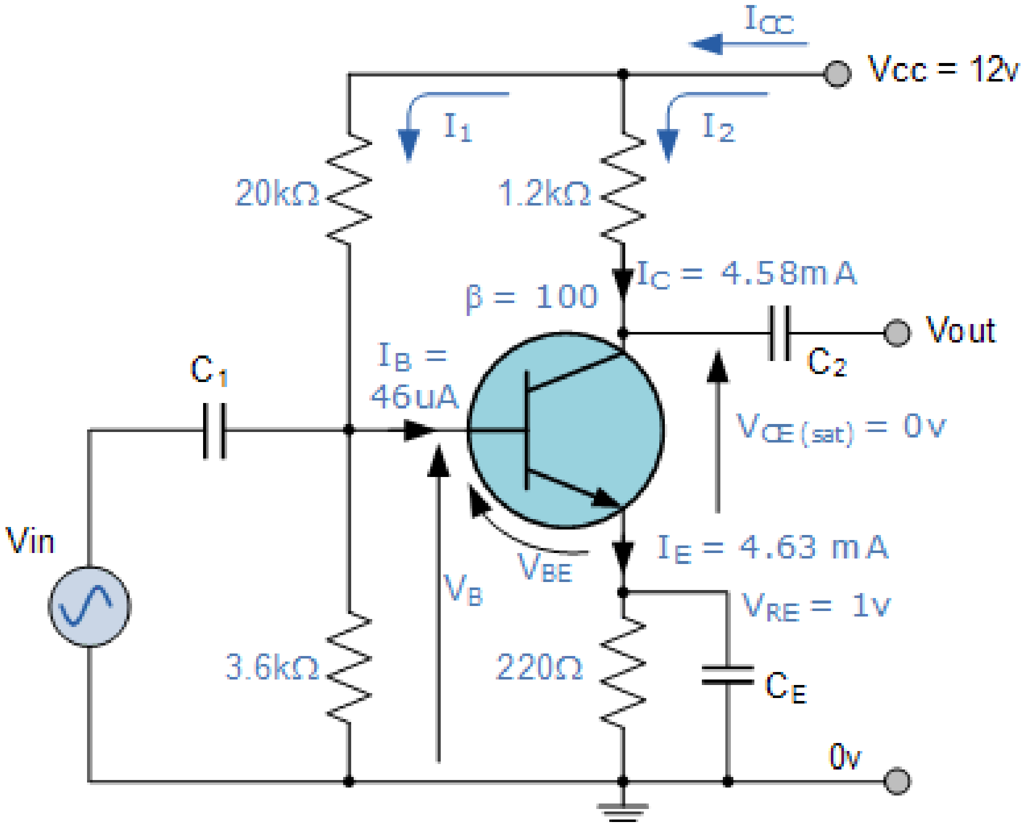
$$I_E = I_C + I_B$$

$$R_E = \frac{1}{4.58 * 10^{-3} + 45.8 * 10^{-6}} = 216\,\Omega$$

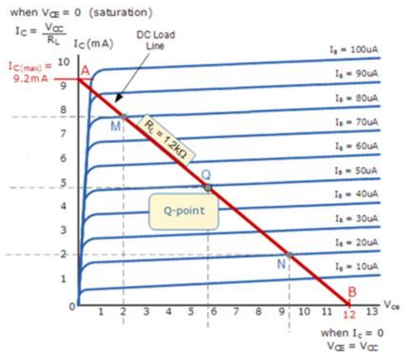
# Common Emitter Amplifier

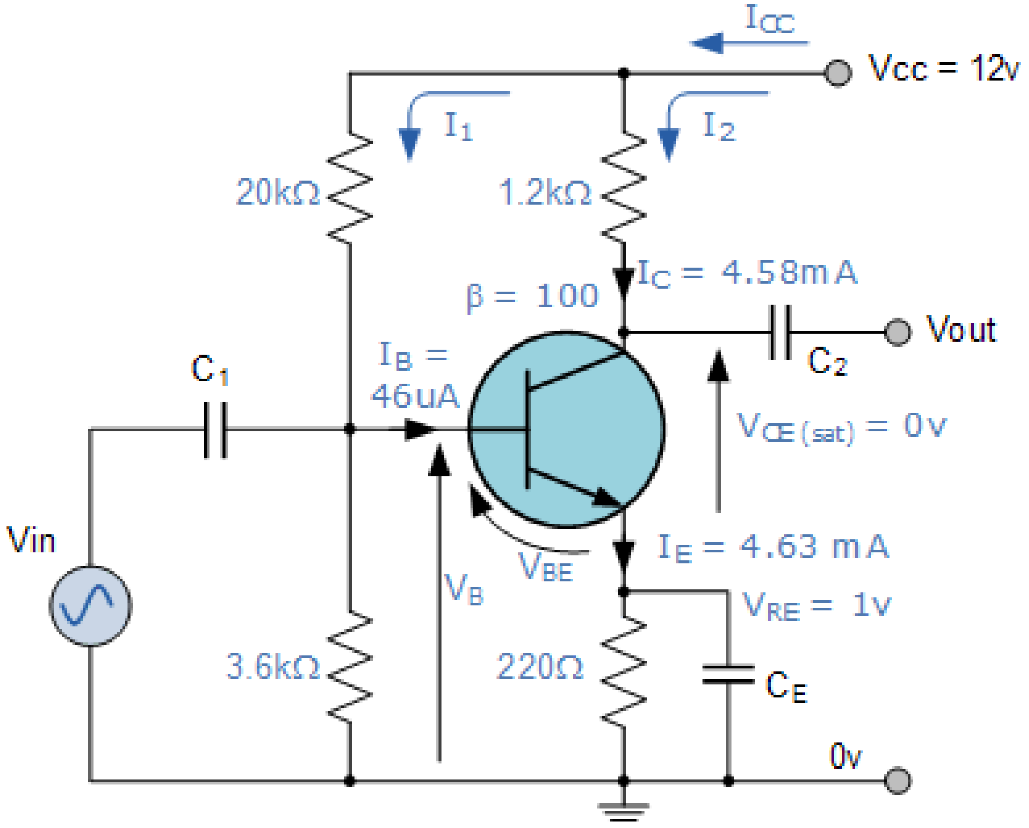



$$R_1 = 20\ k\Omega$$
$$R_2 = 3.6\ k\Omega$$
$$R_E = 220\ \Omega$$

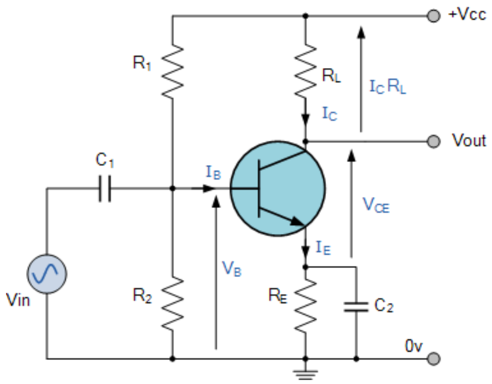


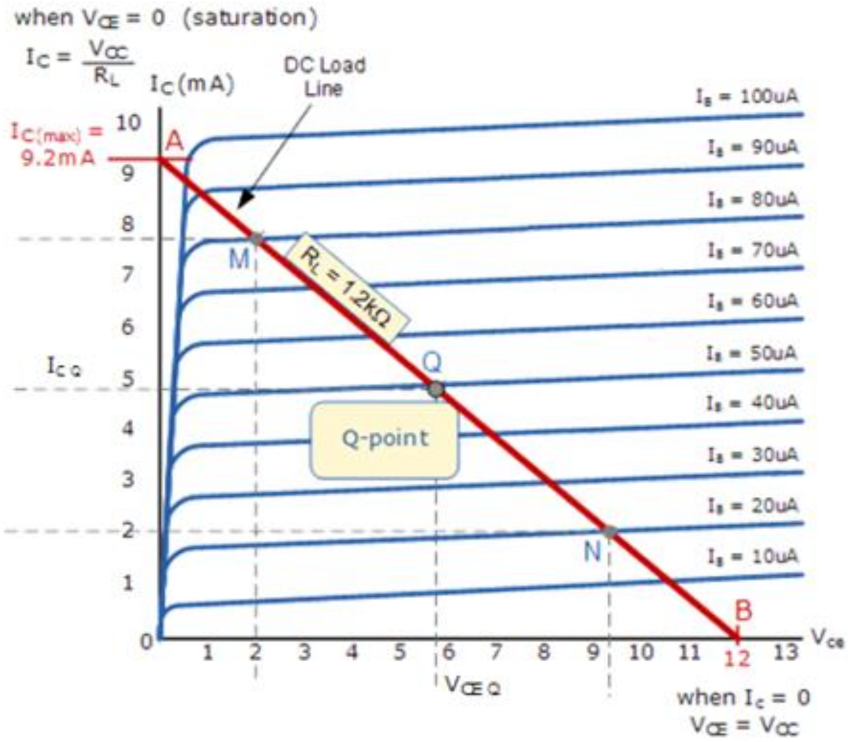
# Capacitors in Common Emitter Amplifier



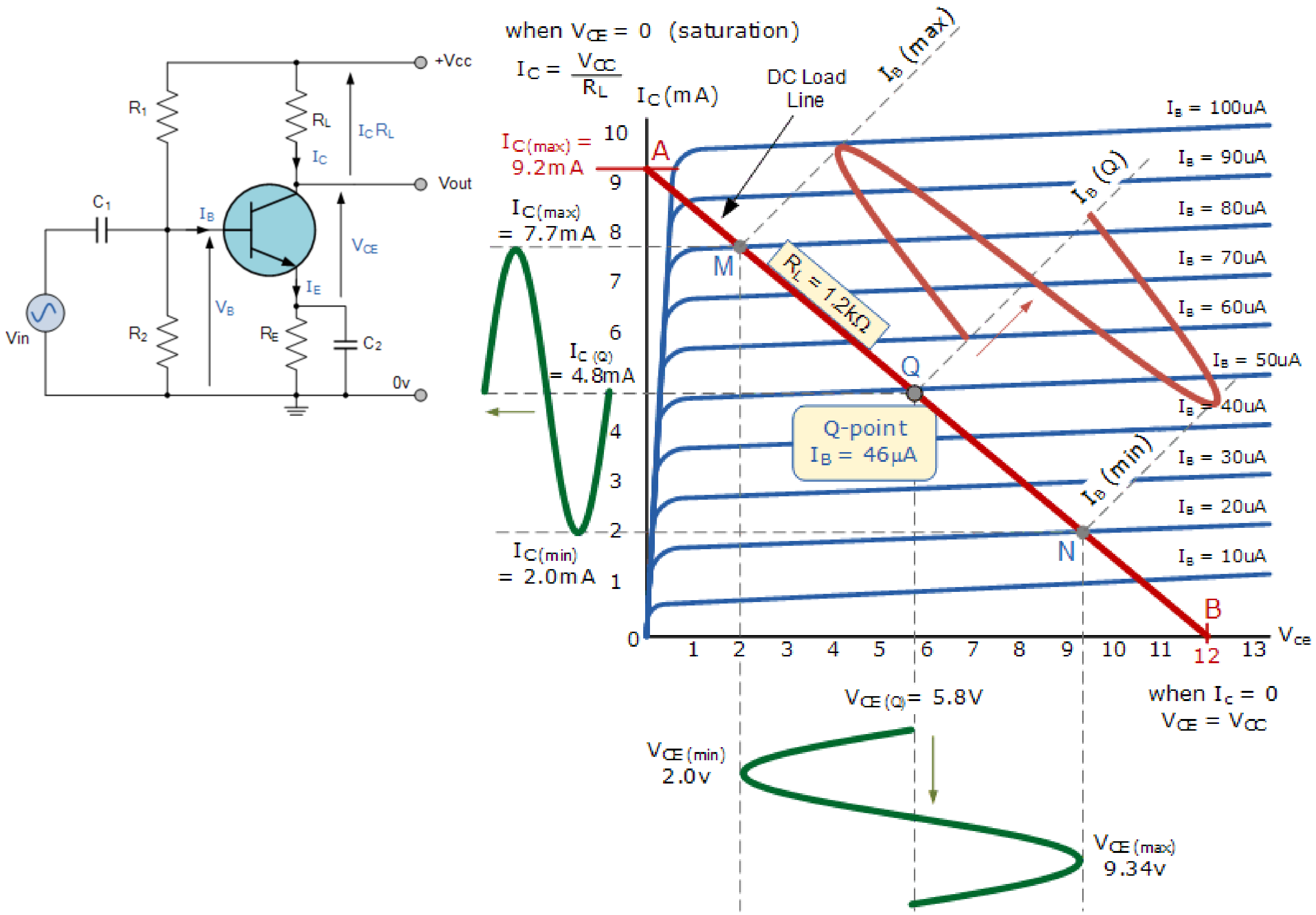


# Common Emitter Amplifier

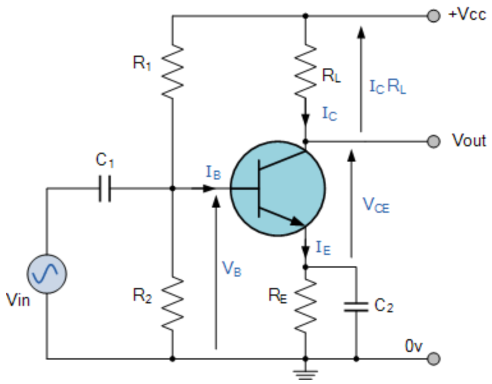


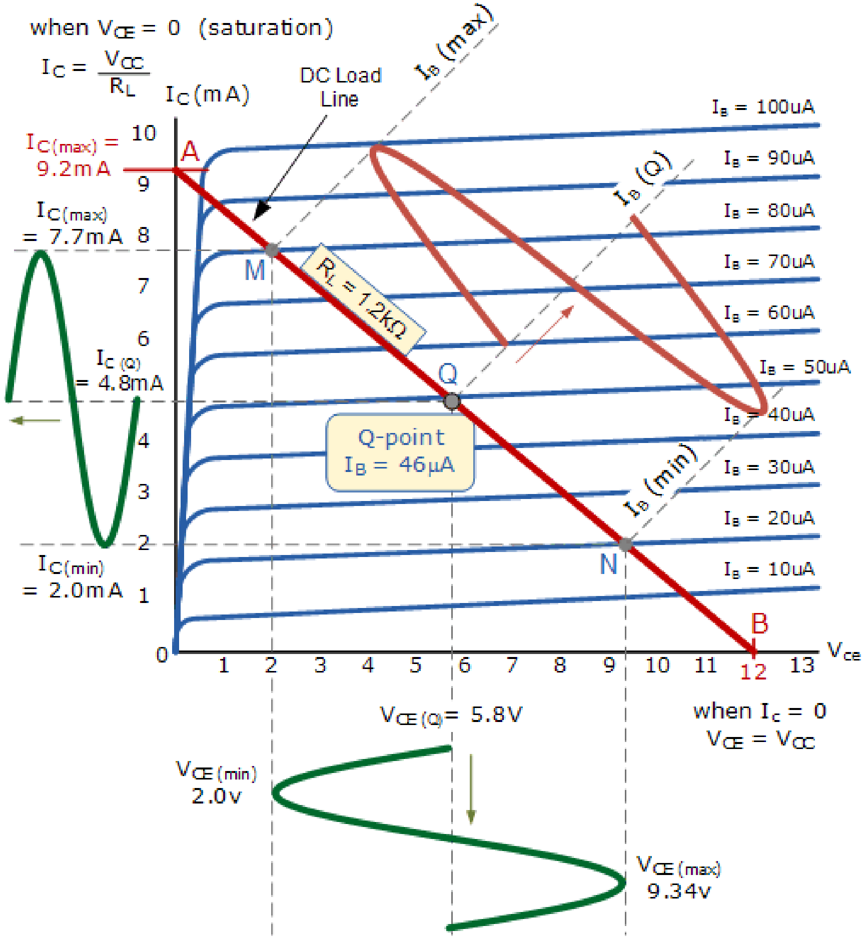



# Common Emitter Amplifier



# Common Emitter Amplifier



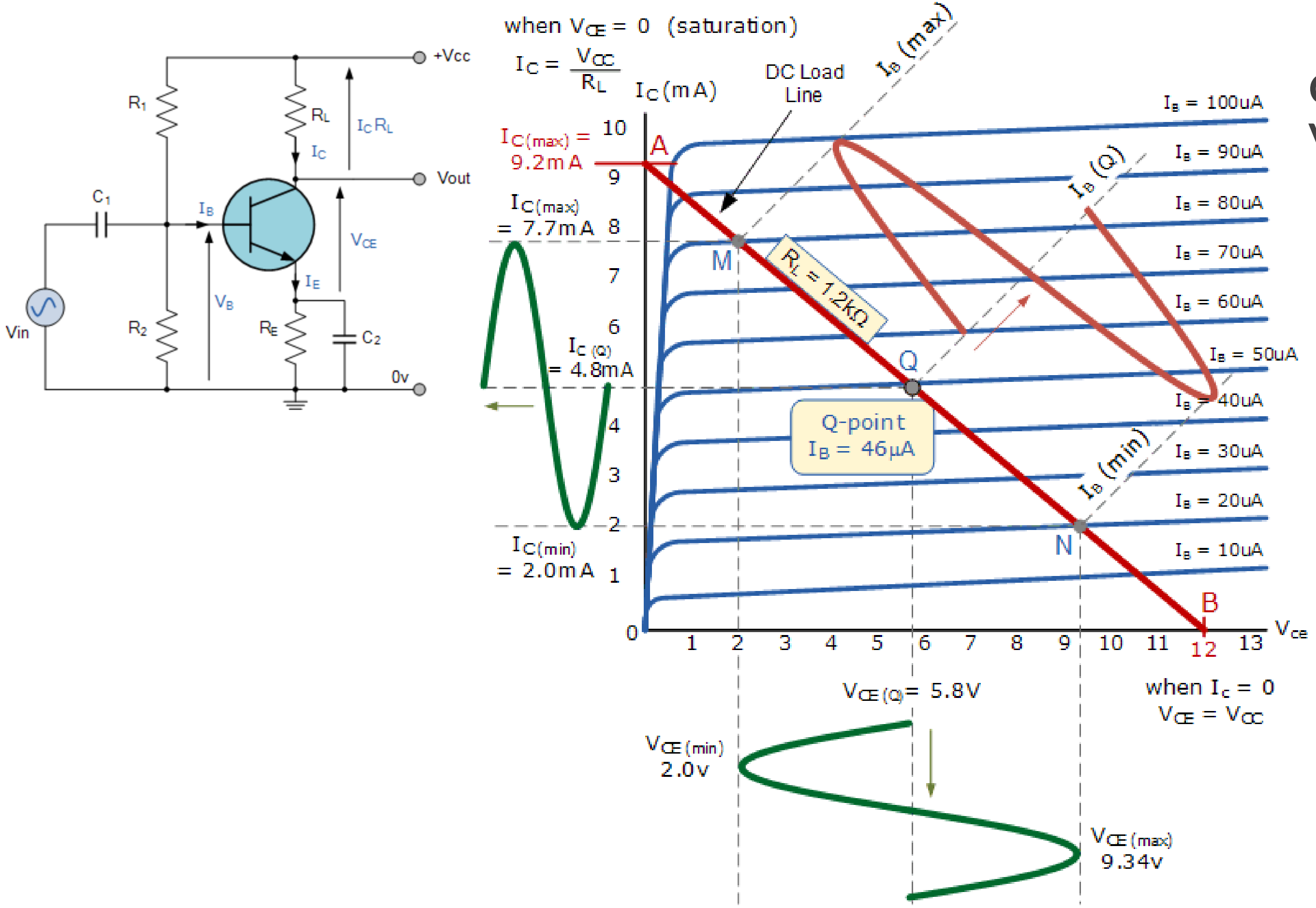

## Common Emitter Voltage Gain

$$A_v = \frac{V_{OUT}}{V_{IN}} = \frac{\Delta V_L}{\Delta V_B}$$

also

$$A_v = \frac{V_{OUT}}{V_{IN}} = -\frac{R_L}{R_E}$$

# Common Emitter Amplifier




## Common Emitter Voltage Gain

$$A_v = -\frac{R_L}{(R_E + r_e)}$$

$$r_e = \frac{25\ mV}{I_E}$$

*Gain at Low Frequencies*

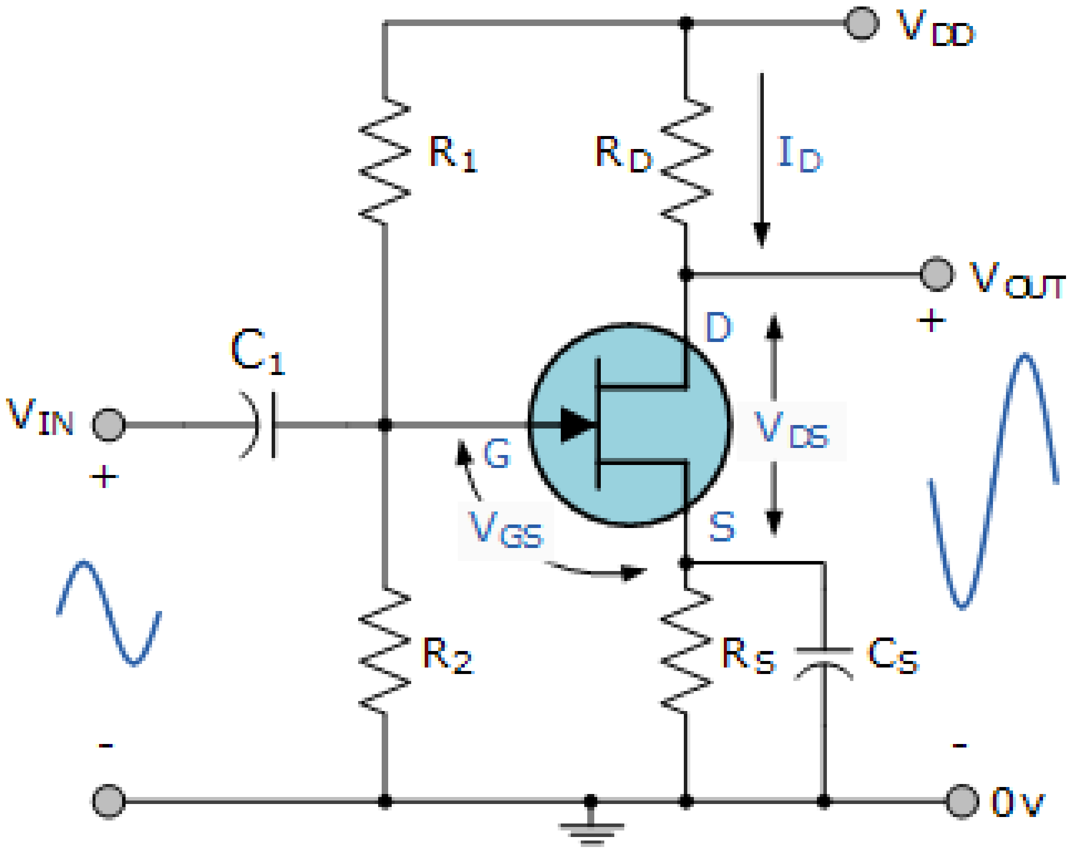
$$A_v = -\frac{1200}{(220 + 5.5)} = -5.32$$

*Gain at High Frequencies*

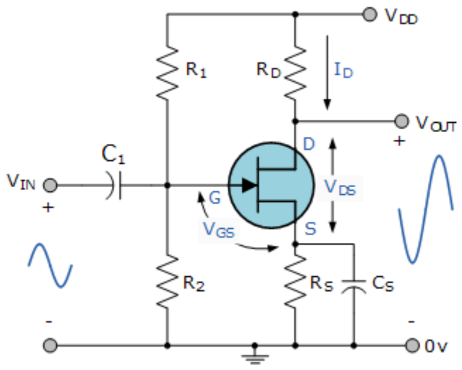
$$A_v = -\frac{1200}{5.5} = -218$$

# Common Source JFET Amplifier

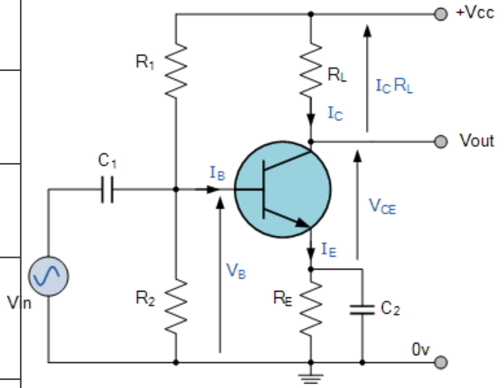
# Common Source JFET Amplifier



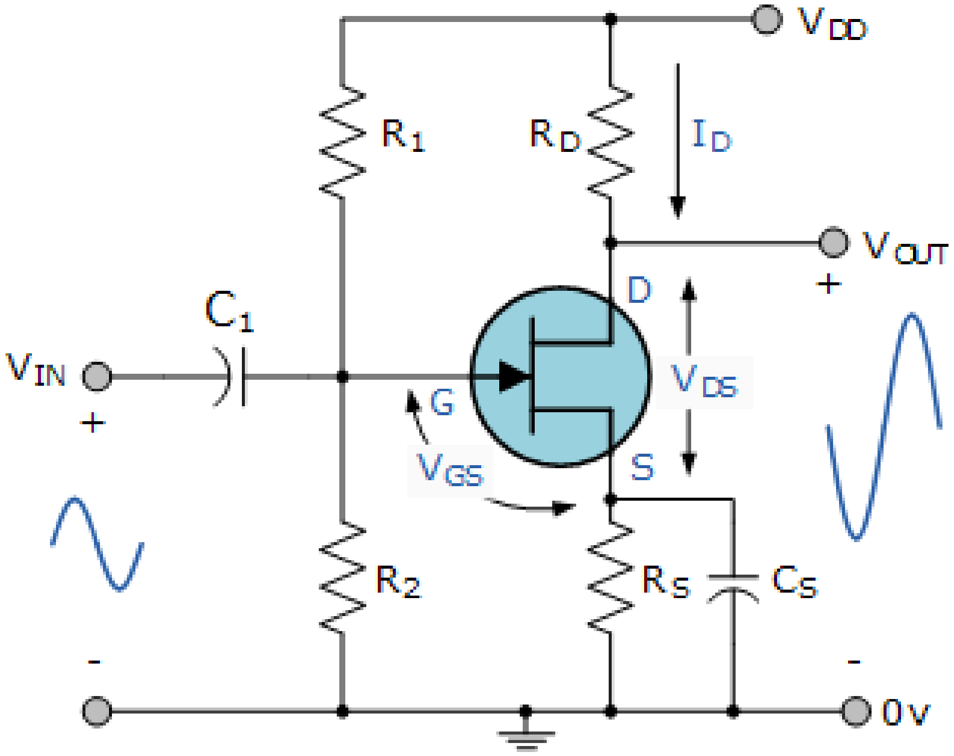
# Common Source JFET Amplifier




| Junction FET | Bipolar Transistor |
|---|---|
| Gate ( G ) | Base ( B ) |
| Drain ( D ) | Collector ( C ) |
| Source ( S ) | Emitter ( E ) |
| Gate Supply ( $V_G$ ) | Base Supply ( $V_B$ ) |
| Drain Supply ( $V_{DD}$ ) | Collector Supply ( $V_{CC}$ ) |
| Drain Current ( $I_D$ ) | Collector Current ( $I_C$ ) |

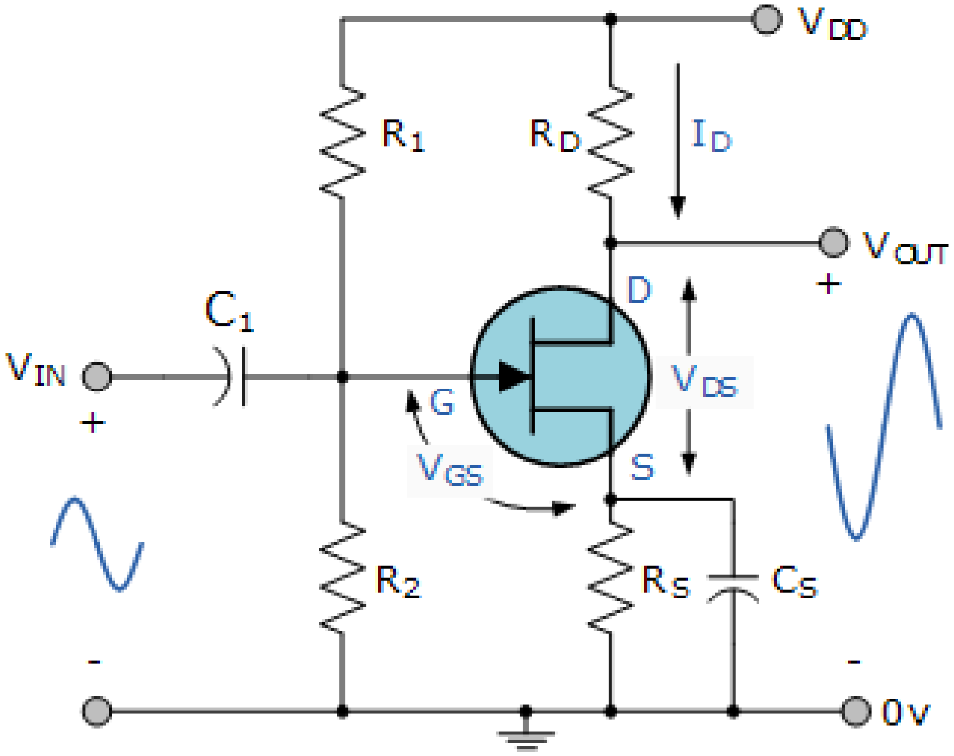


# Common Source JFET Amplifier




$$V_G = V_{DD}\frac{R_2}{R_1 + R_2}$$

# Common Source JFET Amplifier




$$V_G = V_{DD}\frac{R_2}{R_1 + R_2}$$

to keep the gate-source junction reverse biased:

$$V_G > V_S$$

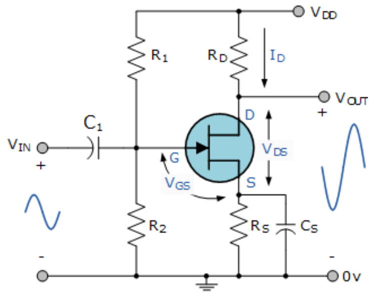
Source voltage

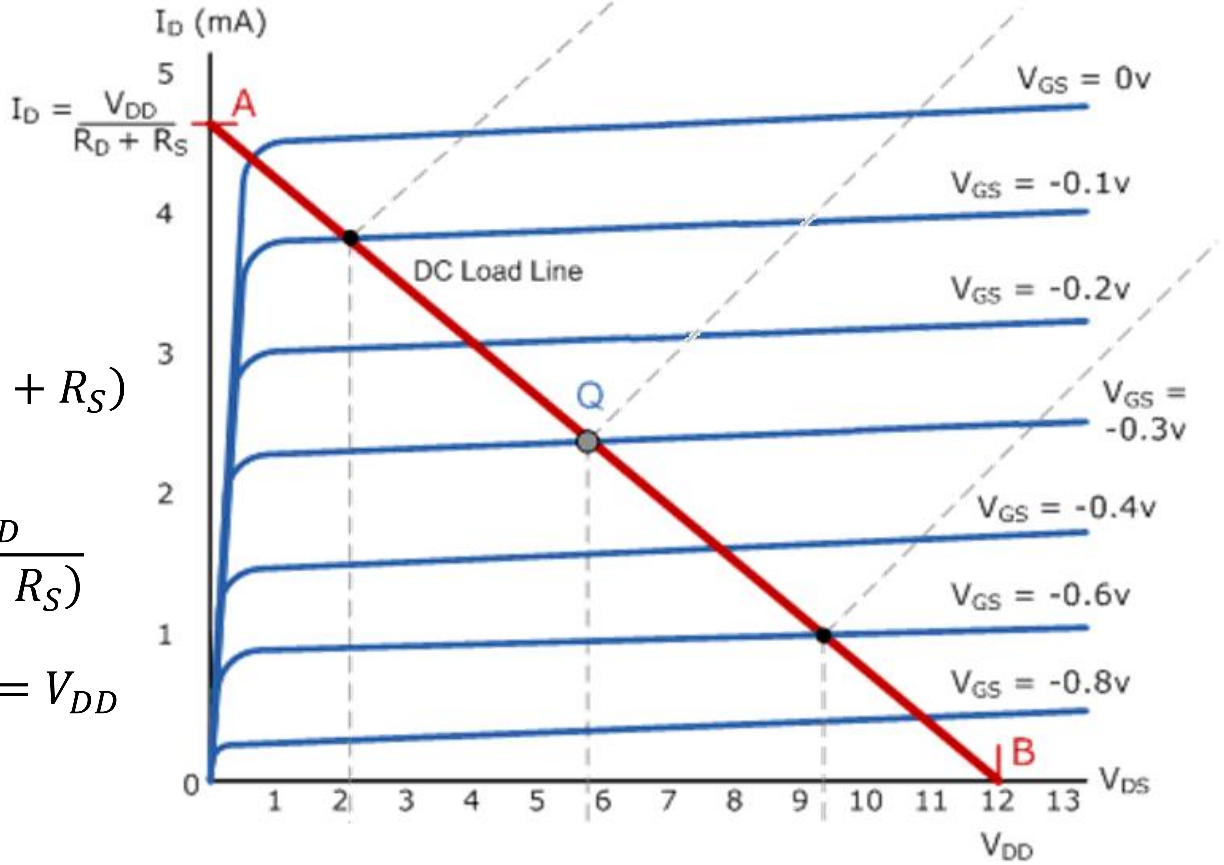
$$V_S = V_G - V_{GS} = I_D * R_S$$

Drain current

$$I_D = \frac{V_S}{R_S} = \frac{V_{DD}}{R_D + R_S}$$

# Common Source JFET Amplifier



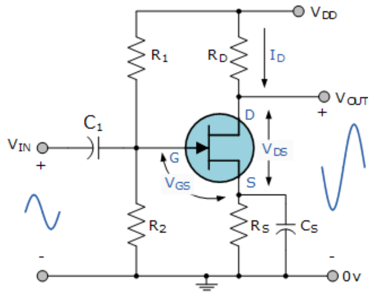

Load line $V_{DD} = V_{DS} + I_D(R_L + R_S)$

Ohmic region (A) $V_{DS} = 0$

$$I_{Dmax} = \frac{V_{DD}}{(R_L + R_S)}$$

Cut-off (B) $I_D = 0, \Rightarrow V_{DS} = V_{DD}$

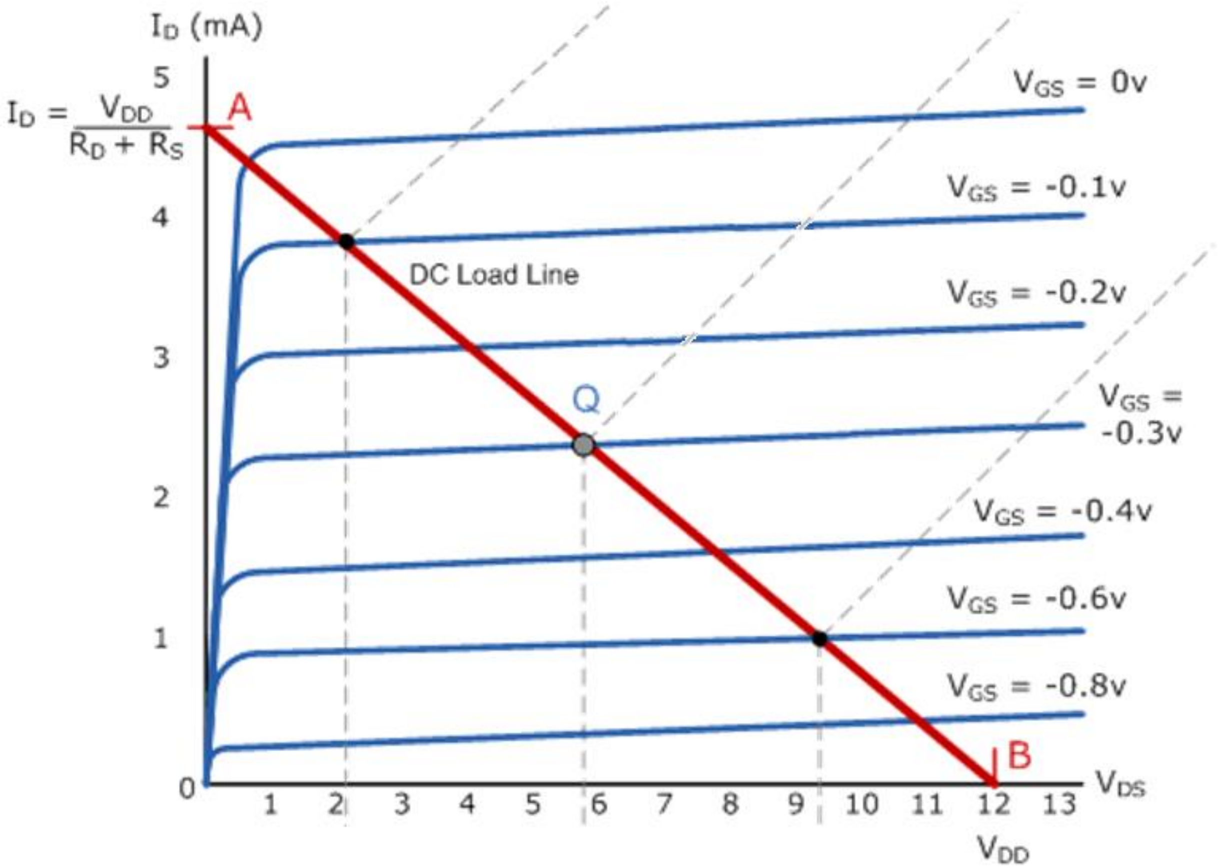
# Common Source JFET Amplifier



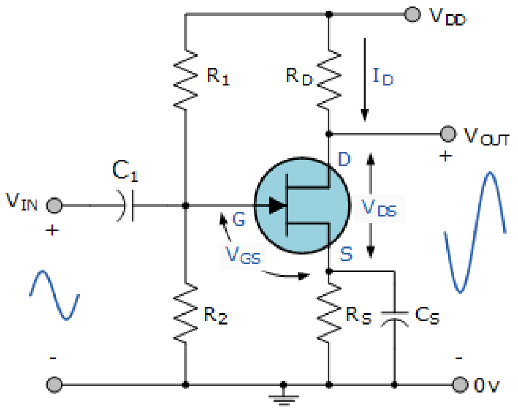

Q-point

$$V_{DSQ} \sim \frac{V_{DD}}{2}$$

$$I_{DQ} \sim \frac{I_{Dmax}}{2}$$



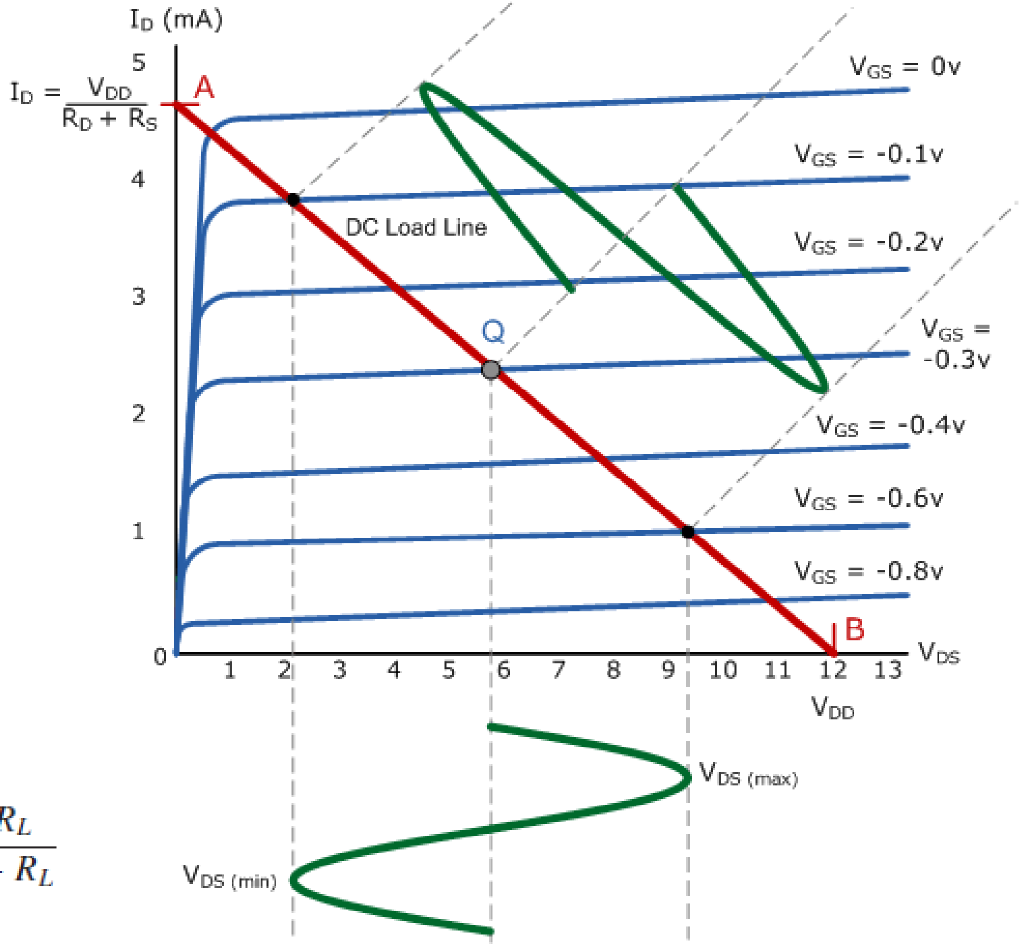
# Common Source JFET Amplifier




$$A_{v_1} = \frac{-g_m r_o R_F}{r_o + R_F}$$

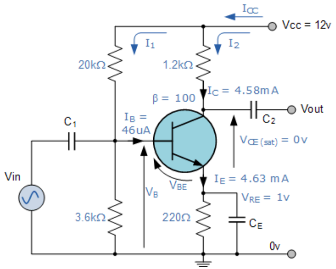
$$A_i = \frac{-g_m r_o R_F R_{\text{in}}}{R_L(r_o + R_F)} = \frac{R_{\text{in}}}{R_L} A_{v_1}$$

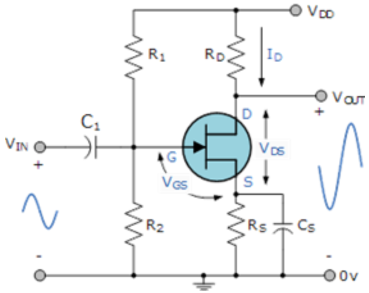
where $\quad R_F = R_D \| R_L = \dfrac{R_D R_L}{R_D + R_L}$

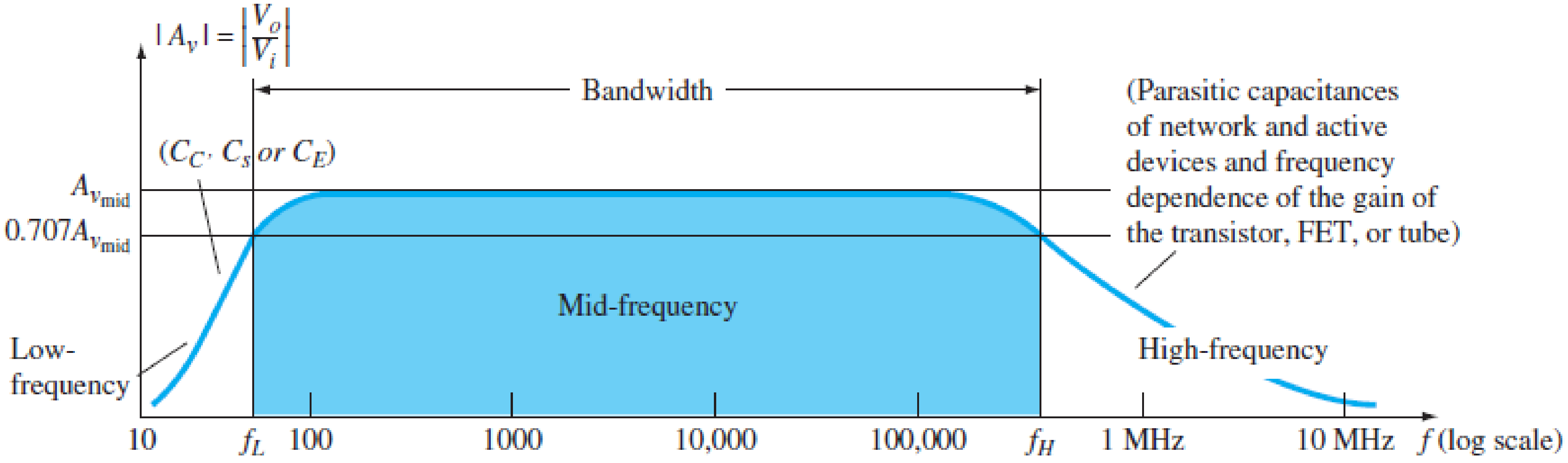


# Frequency Response

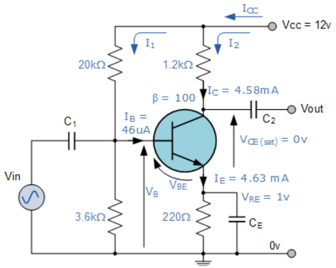
# Typical Frequency Response

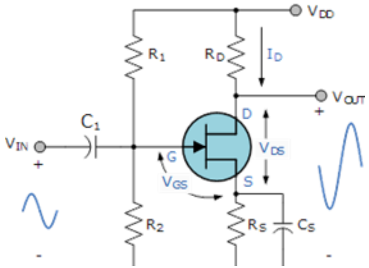


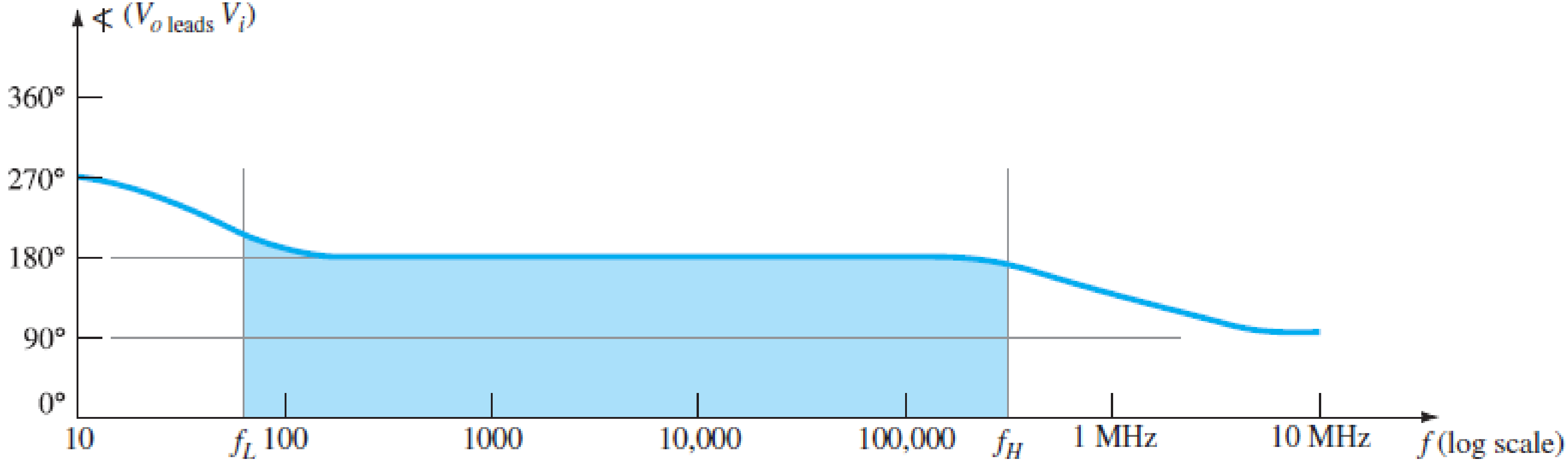



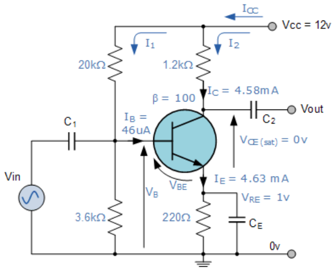
# Typical Frequency Response

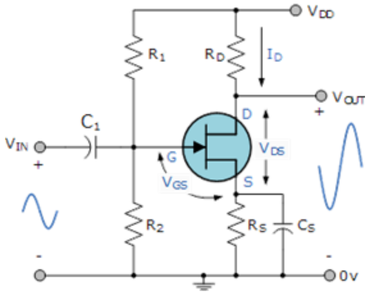


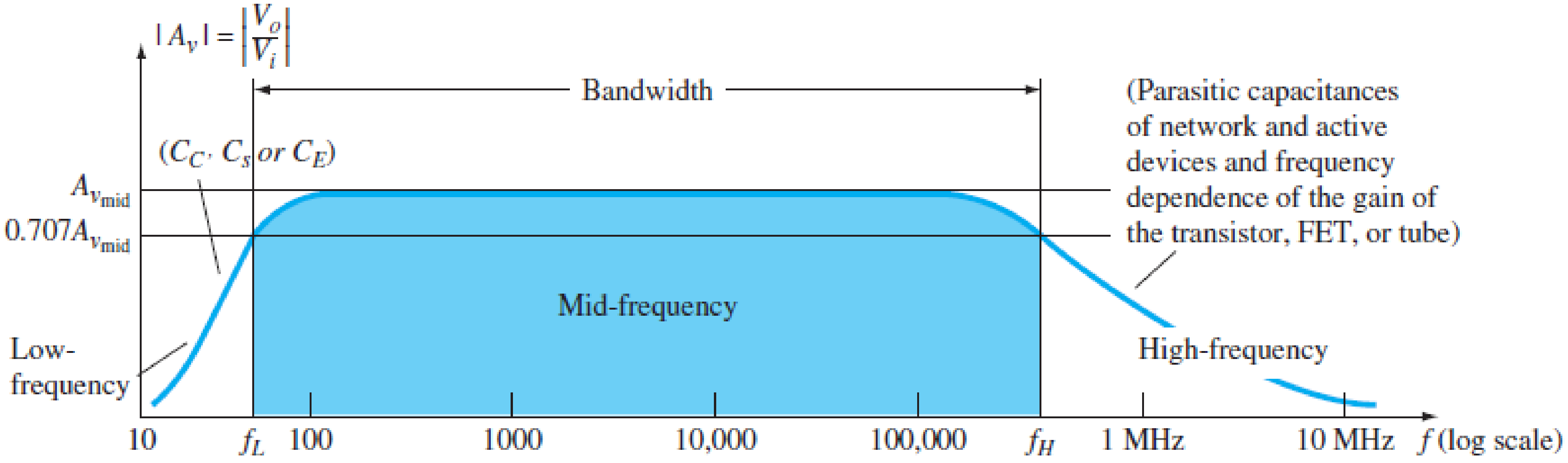



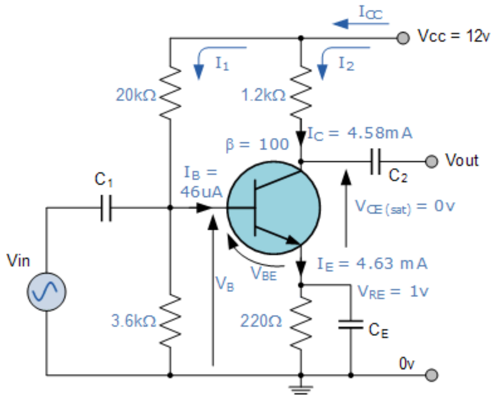
# Typical Frequency Response

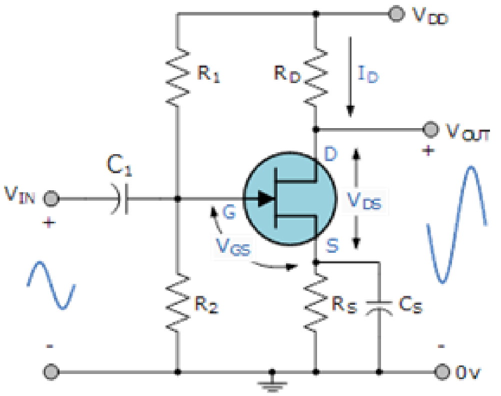


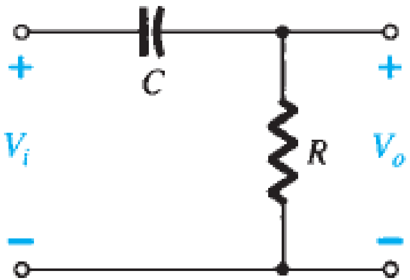



# Low frequency

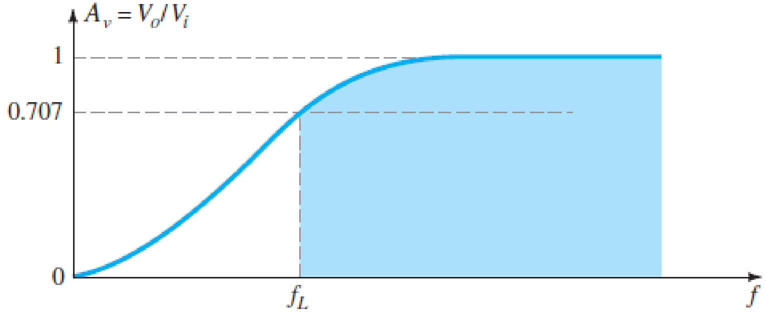



*RC circuit*




*Low-frequency response for the RC circuit*



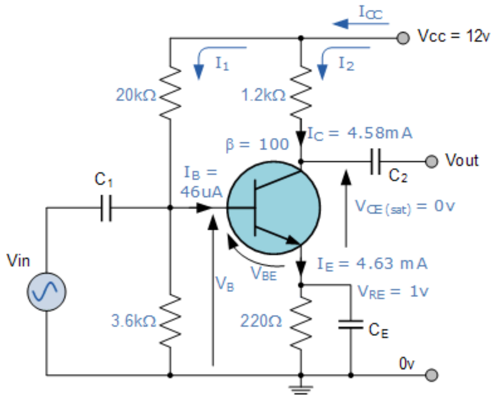

$$V_o = \frac{RV_i}{R + X_C}$$

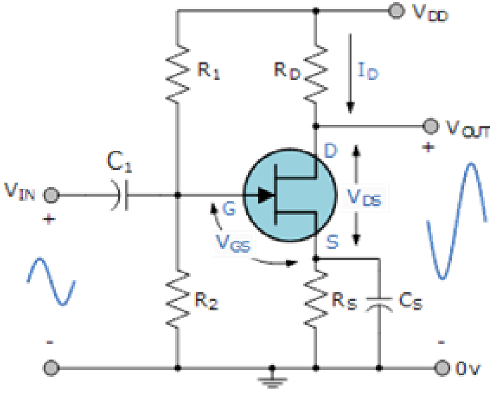
$$|A_v| = \frac{V_o}{V_i} = \frac{1}{\sqrt{2}} = 0.707\Big|_{X_C=R}$$

$$C = \frac{1}{2\pi f_L R}$$

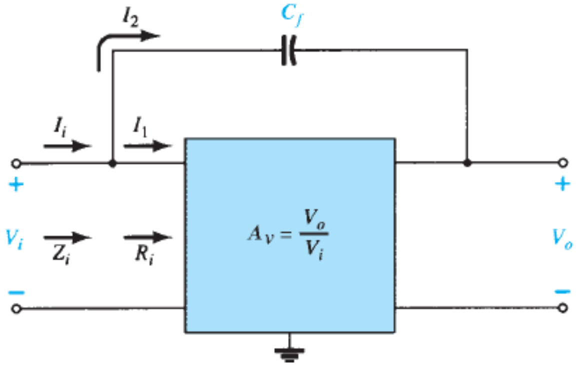
Where *R* is equivalent resistor of input or output circuit, or $R_E$ or $R_S$

# Hi frequency



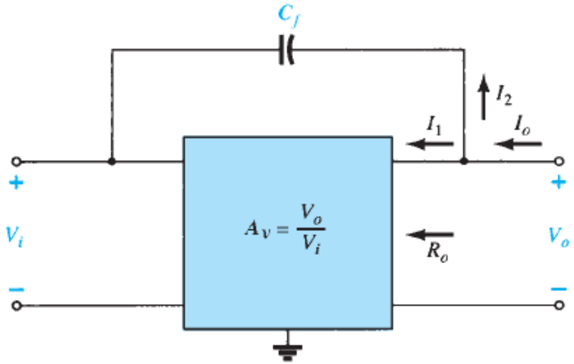




## Miller effect input capacitance




$$C_{M_i} = (1 - A_v)C_f$$

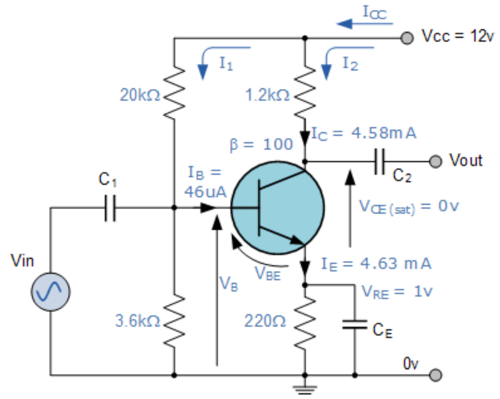
## Miller output capacitance

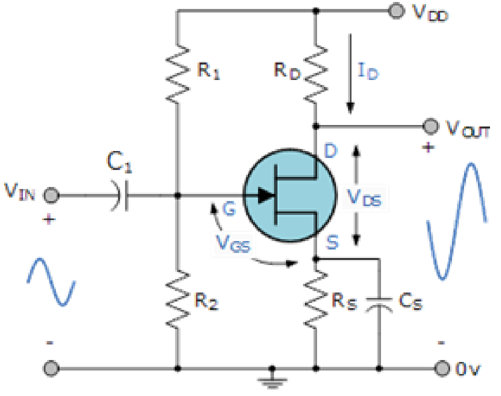


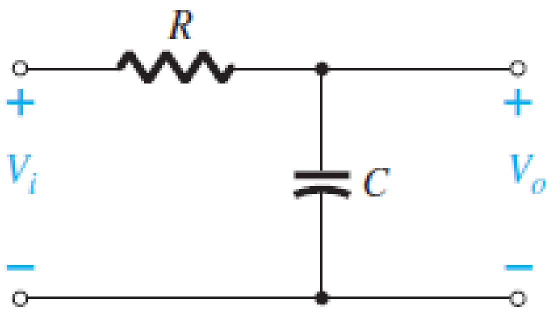

$$C_{M_o} = \left(1 - \frac{1}{A_v}\right)C_f$$

For the usual situation where $A_v \gg 1$

$$C_{M_o} \cong C_f$$



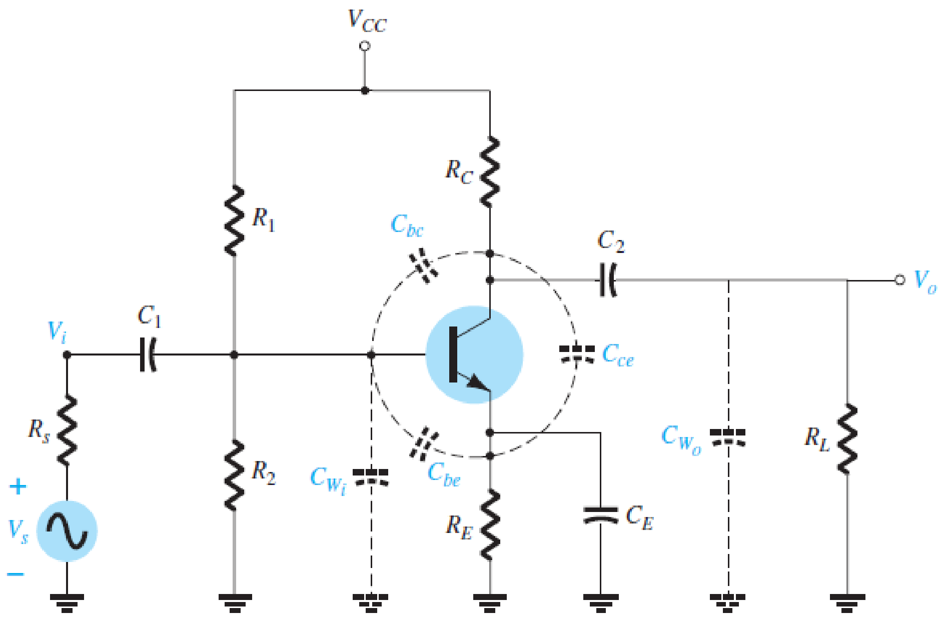




$$f_{Hi} = \frac{1}{2\pi R_{eq} C_{eq}}$$

Where $R_{eq}, C_{eq}$ is equivalent resistor and capacitance of input or output circuit

**Parasitic capacitances**




**$h_{fe}$ (or $\beta$) Variation**

$$h_{fe} = \frac{h_{fe\,mid}}{1 + j\left(f/f_\beta\right)}$$

*where*

$$f_\beta = \frac{1}{h_{fe\,mid}} \frac{1}{2\pi r_e (C_{BE} + C_{BC})}$$

Equation clearly reveals that because $r_e$ is a function of the network design: $f_\beta$ is a function of the bias configuration.

# Hi frequency. BJT

$$h_{fe} = \frac{h_{fe\,mid}}{1 + j\left(f/_{f_\beta}\right)}$$

direct conversion for determining $f_\beta$
if $f_\alpha$ and $\alpha$ are specified

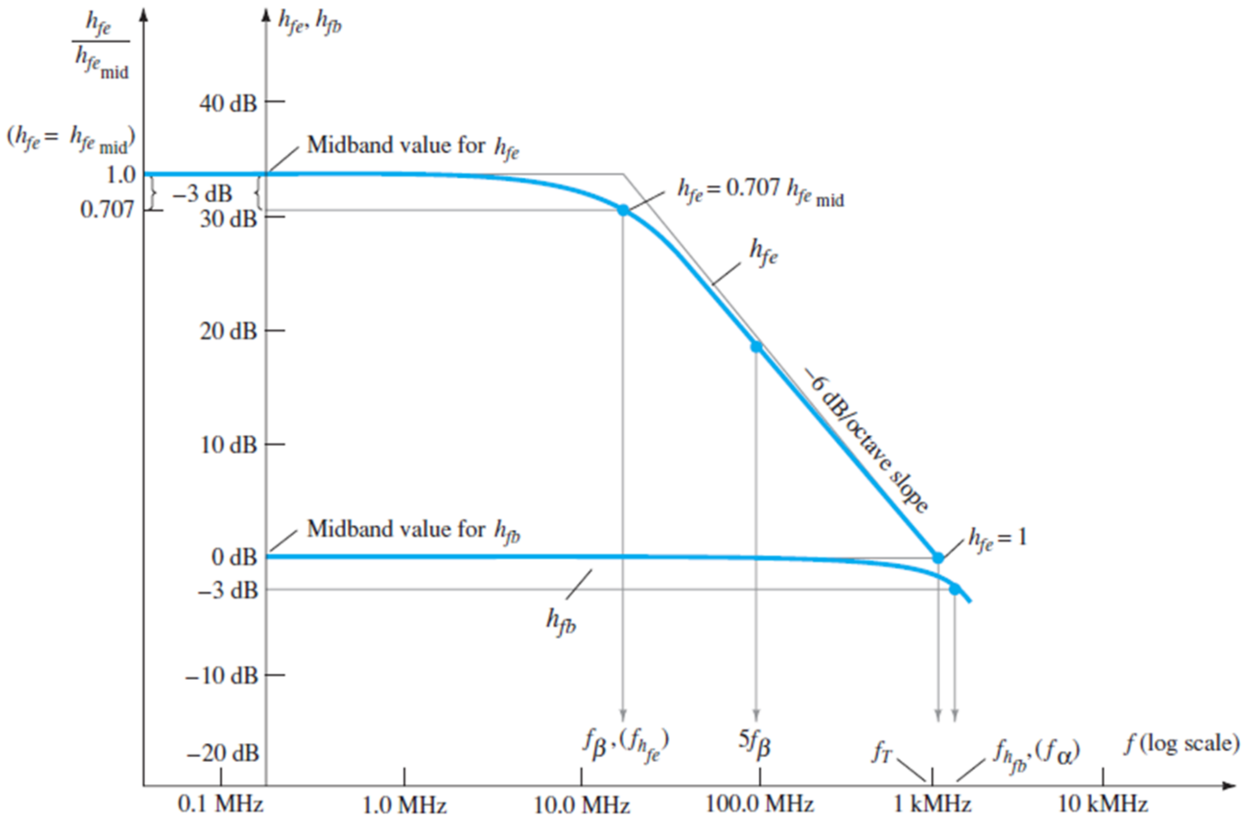
$$f_\beta = f_\alpha(1 - \alpha)$$

**Gain-Bandwidth Product**

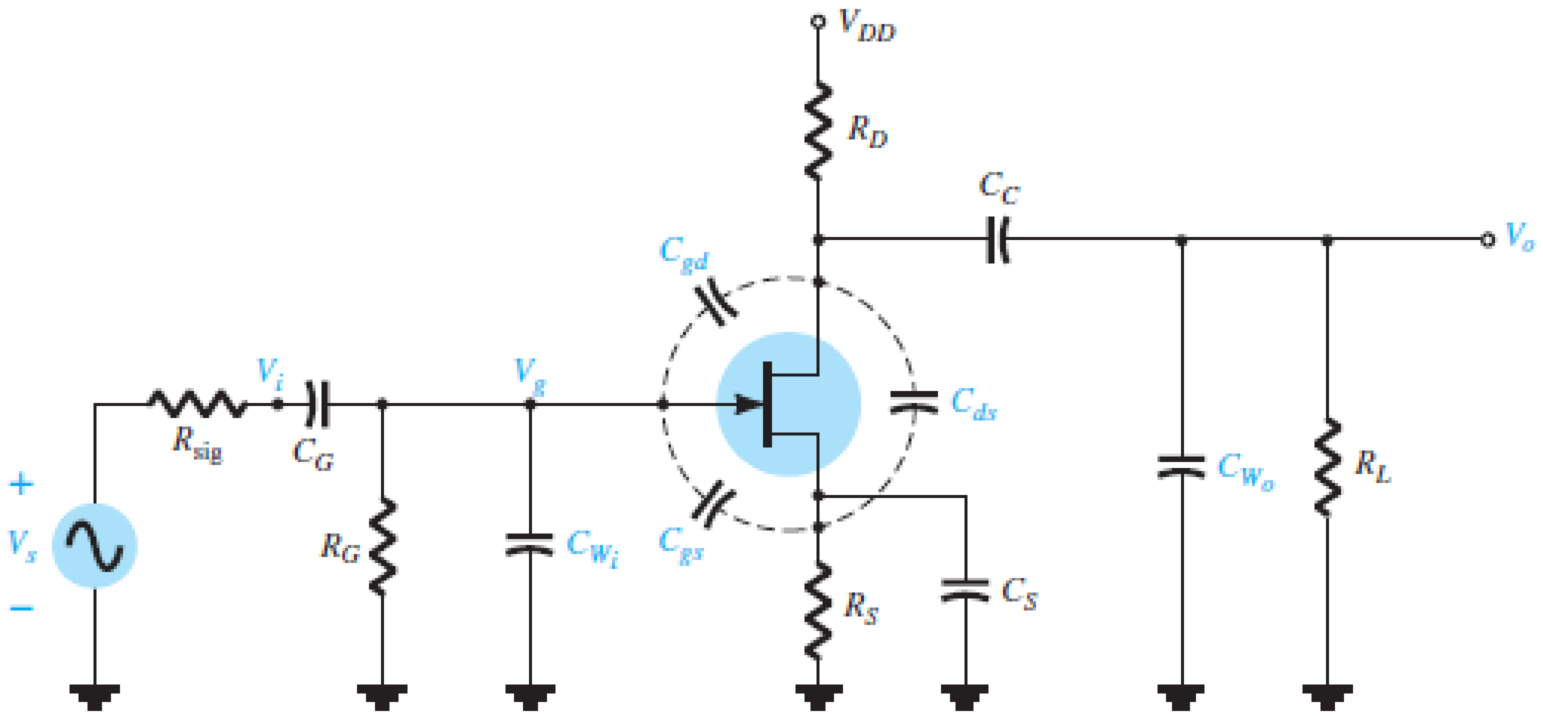
GBP = $A_{v\,mid} * \Delta f$

At $A_v = 1, \Delta f = f_T$

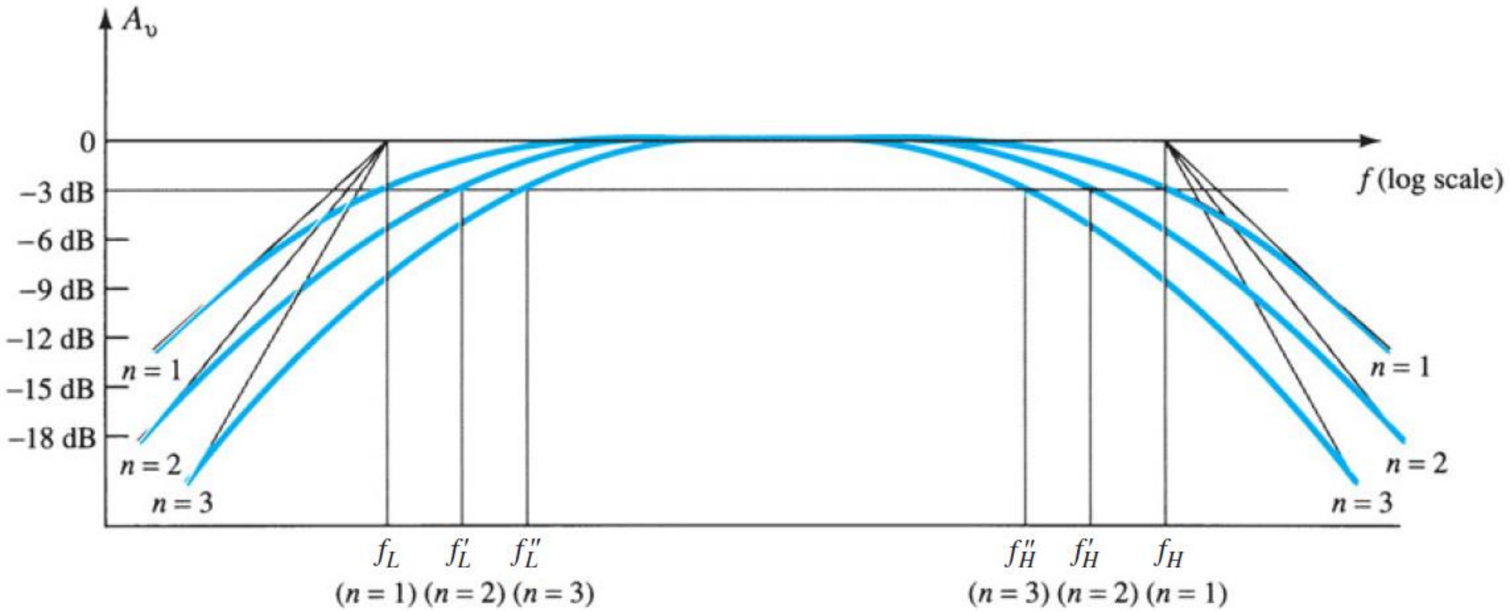
$$f_T = A_{v\,mid} * f_H$$



# Gain-Bandwidth Product



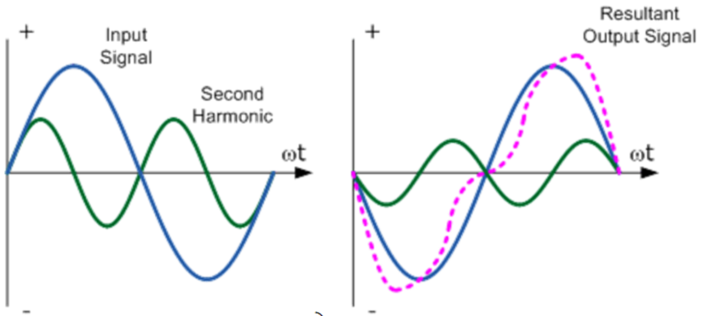
# Multistage frequency effects

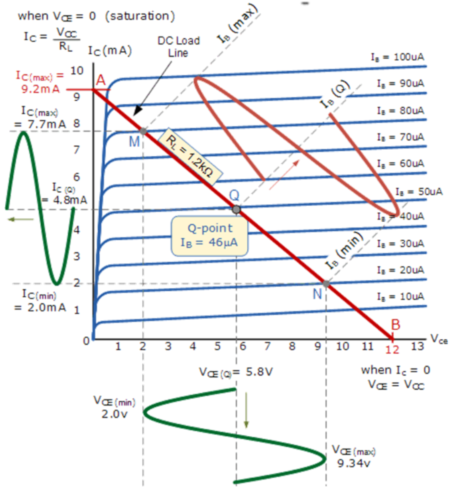



if all the cascades are the same, then

$$f'_L = \frac{f_L}{\sqrt{2^{1/n} - 1}} \qquad f'_H = (\sqrt{2^{1/n} - 1})f_H$$

# Harmonic Distortion




**Harmonic distortion can be defined as**

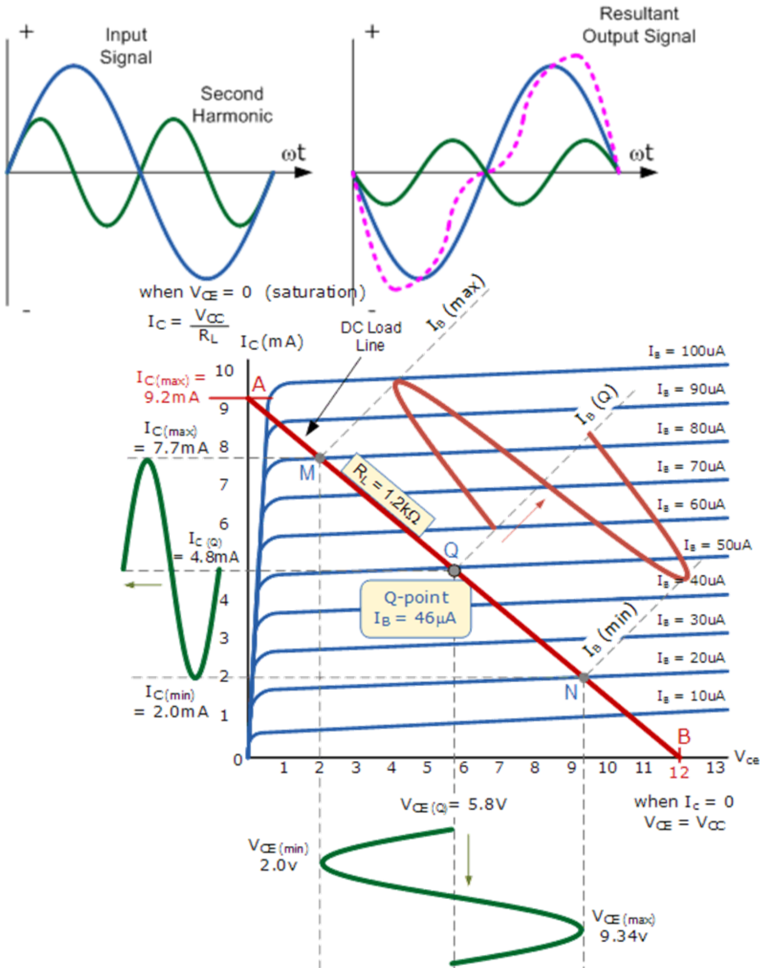
$$\%\ n\text{th harmonic distortion} = \%\ D_n = \frac{|A_n|}{|A_1|} \times 100\%$$

The fundamental component is typically larger than any harmonic component.

**Total Harmonic Distortion**

$$\%\ \text{THD} = \sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots} \times 100\%$$

# Common Source JFET Amplifier




the second harmonic distortion in terms of measured collector current

$$D_2 = \left| \frac{\frac{1}{2}(I_{C_{\max}} + I_{C_{\min}}) - I_{C_Q}}{I_{C_{\max}} - I_{C_{\min}}} \right| \times 100\%$$

the second harmonic distortion in terms of measured collector–emitter voltages

$$D_2 = \left| \frac{\frac{1}{2}(V_{CE_{\max}} + V_{CE_{\min}}) - V_{CE_Q}}{V_{CE_{\max}} - V_{CE_{\min}}} \right| \times 100\%$$

# References

1. Sarma M. S. Introduction to electrical engineering. – New York : Oxford University Press, 2001. – C. 715-716.
2. Boylestad, Robert L. Electronic devices and circuit theory / Robert L. Boylestad, Louis Nashelsky.—11th ed.
3. ISBN 978-0-13-262226-4Scherz P., Monk S. Practical electronics for inventors. – McGraw-Hill Education, 2016.
4. Horowitz, Paul, and Winfield Hill. "The Art of Electronics. 3rd." *New York, NY, USA: University of Cambridge* (2015).
5. All about circuits (https://www.allaboutcircuits.com/)
6. https://www.electronics-tutorials.ws/
7. https://en.wikipedia.org/

# Thank you for your attention!

# Amplifier configurations