MachXO2 and MachXO3 Starter Kit

Evaluation Board User Guide

FPGA-EB-02036-1.3

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DIP	Dual In-line Package
FPGA	Field-Programmable Gate Array
LED	Light Emitting Diode
LUT	Look-Up Table
NVCM	Non Volatile Configuration Memory
PCB	Printed Circuit Board
RoHS	Restriction of Hazardous Substances Directive
USB	Universal Serial Bus
WDT	Watchdog Timer

1. Introduction

This user guide describes how to start using the MachXO2 and MachXO3 Starter Kits, an easy-to-use platform for evaluating and designing with the Mach XO2 and MachXO3 ultra-low density FPGA. Along with the board and accessories, this kit includes a pre-loaded demonstration design. You may also reprogram the on-board MachXO2 and MachXO3 device to review your own custom designs.

The MachXO2 Start Kit currently features the LCMXO2-4000ZE (Flash Based) device in the 256-ball 0.8 mm pitch caBGA package. The MachXO3 Starter Kit currently features the MachXO3L-6900C (NVCM Based) or the MachXO3LF-6900C (Flash Based) device in the 256-ball 0.8 mm pitch caBGA package. The kits also include a Serial Flash Memory for demonstrating external SPI boot-up. The external Flash Memory also supports a dual-boot mode in addition to Golden boot/fail-safe boot options.

See the Ordering Information section for more information.

Note: Static electricity can severely shorten the lifespan of electronic components. See the Storage Handling section of this document for handling and storage tips.

2. Features

The MachXO2 and MachXO3 Starter Kits include:

- Mach XO2/MachXO3L/MachXO3LF Board – The board is a 3” x 3” form factor that features the following on-board components and circuits:
  - One of the following FPGAs
    - LCMXO2-4000ZE-1BG256C (Flash Based)
    - LCMXO3L-6900C-5BG256C (NVCM Based)
    - LCMXO3LF-6900C-5BG256C (Flash Based)
  - USB mini-B connector for power and programming
  - 4-Mb Serial Flash Memory for boot image and dual-boot support.
  - Eight LEDs
  - 4-position DIP switch
  - Momentary push button switch
  - 40-hole prototype area
  - Four 2 x 20 expansion header landings for general I/O, JTAG, and external power
  - 1 x 8 expansion header landing for JTAG
  - 1 x 6 expansion header landing for SPI/I^2C
  - 3.3 V and 1.2 V supply rails

Pre-loaded Demo – The kit includes a pre-loaded counter design that highlights use of the embedded MachXO2 and MachXO3 oscillators and programmable I/O configured for LED drive.

USB Connector Cable – The board is powered from the USB mini-B socket when connected to a host PC. The USB channel also provides a programming interface to the MachXO2 and MachXO3 JTAG ports.

Lattice Development Kits and Boards Web Page – Visit www.latticesemi.com/breakoutboards for the latest documentation (including this guide) and drivers for the kit.

The content of this user guide includes demo operation, programming instructions, top-level functional descriptions of the Starter Kit, descriptions of the on-board connectors, and a complete set of schematics.

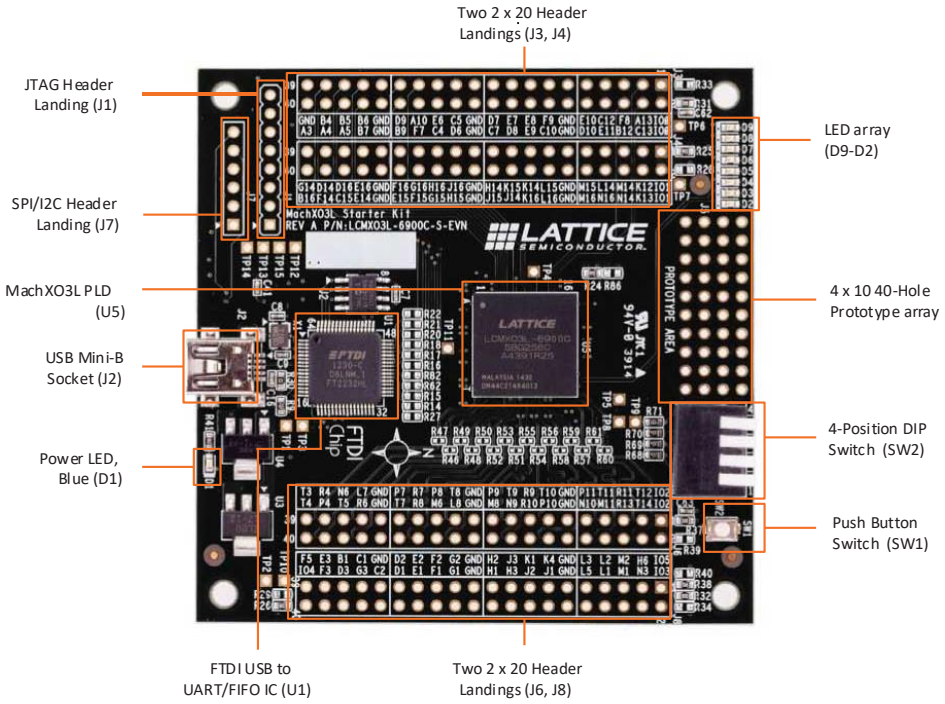


Figure 2.1. MachXO3 Board (MachXO3L Version), Top Side

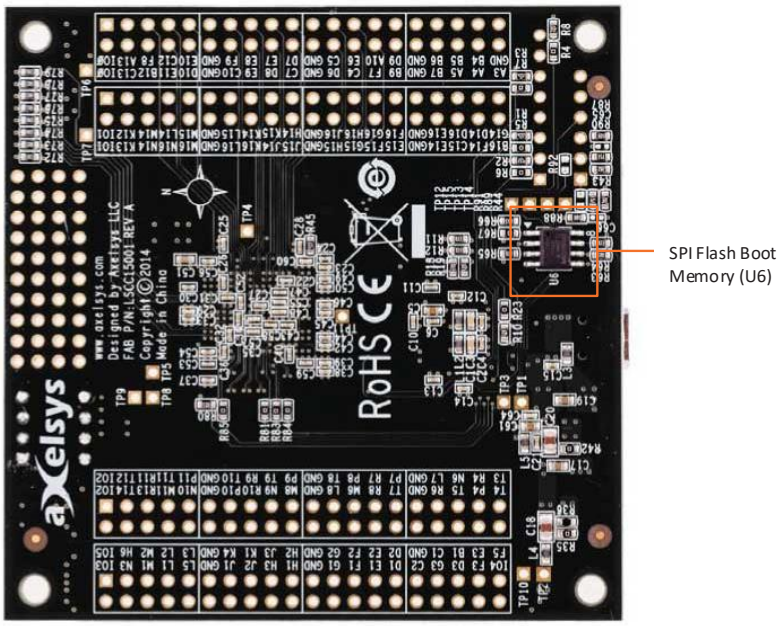


Figure 2.2. MachXO3 Board (MachXO3L Version), Bottom Side

3. Storage Handling

Static electricity can shorten the lifespan of electronic components. Observe these tips to prevent damage that could occur from electro-static discharge:

Use anti-static precautions such as operating on an anti-static mat and wearing an anti-static wrist-band.

Store the evaluation board in the packaging provided.

Touch a metal USB housing to equalize voltage potential between you and the board.

4. Software Requirements

You should install the following software before you begin developing designs for the Starter Kit:

Lattice Diamond® design software

FTDI Chip USB hardware drivers (installed as an option within the Diamond installation program)

5. MachXO2 and MachXO3 Devices

This board currently features the MachXO3L-6900C FPGA which offers embedded Non-Volatile Configuration Memory (NVCM) technology, the MachXO3LF-6900C FPGA which offers embedded Non-Volatile Flash technology for instant-on operation in a single chip, or MachXO2-4000ZE FPGA which also offers embedded Non-Volatile Flash technology for instant-on operation in a single chip. Numerous system functions are included, such as two PLLs and 256 kbits of embedded RAM plus hardened implementations of I^2C and SPI. Flexible, high performance I/O support numerous single-ended and differential standards including LVDS. The 256-ball BGA package provides up to 206 user I/O in a 14 mm x 14 mm form factor. A complete description of these devices can be found in the MachXO2 Family Data Sheet (FPGA-DS-02056) or the MachXO3 Family Data Sheet (FPGA-DS-02032).

6. Demonstration Design

Lattice provides a simple, pre-programmed demo to illustrate basic operation of the MachXO2 and MachXO3 devices. The design integrates an up-counter with the on-chip oscillator. For the XO3L Starter Kit, pre-programmed design resides in the external Serial Flash Memory (SPANSION S25FL204K or S25FL208K, or ON Semiconductor LE25U40CMD). For the XO2 and XO3LF Starter Kits, the pre-programmed design resides in the on-board configuration flash memory.

Note: To restore the factory default demo and program it with other Lattice-supplied examples see the Download Demo Designs section.

6.1. Run the Demonstration Design

Upon power-up, the pre-programmed demonstration design automatically loads and drives the LED array in a 1-hertz pattern. The program shows a clock divider driven either by the MachXO2/MachXO3 internal oscillator or the external FTDI clock chip. The divider modules (*heartbeat.v* and *kitcar.v*) are clocked at the default frequency of 12 MHz which divides the clock to cycle the LED display approximately once per second. The resulting light pattern is determined by the DIP Switch (SW2) setting as shown in Table 6.1.

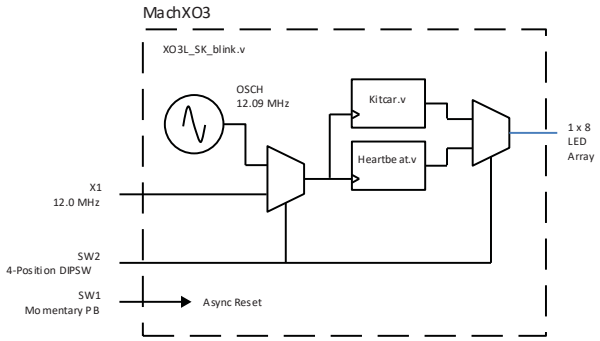


Figure 6.1. Demonstration Design Block Diagram

Table 6.1. DIP Switch and LED Behavior

Switch	Setting	LED Behavior
DIP_SW[1]	0 (Down)	External 12.0 MHz (X1)
	1 (Up)	Internal 12.09 MHz (OSCH)
DIP_SW[2:4]	001	1 Hz Sweep
	011	1 Hz Left-Right
	111	1 Hz Blink
	Others	1 Hz Alternating

WARNING: Do not connect the board to your PC before you follow the driver installation procedure of this section.

Communication between the board and a PC, through the USB connection cable, requires installation of the FTDI chip USB hardware drivers. Loading these drivers enables the computer to recognize and program the board. Drivers can be loaded as part of the installation of Lattice Diamond design software or Diamond Programmer, or as a stand-alone package.

To load the FTDI Chip USB hardware drivers as part of the Lattice Diamond installation:

1. Select **Programmer Drivers** in the Product Options of Lattice Diamond Setup.
2. Select **FTDI Windows USB Driver** or **All Drivers** in the LSC Drivers Install/Uninstall dialog box.
3. Click **Finish** to install the USB driver.
4. After the driver installation is complete, connect the USB cable from a USB port on your PC to the board's USB mini-B socket (J2). After the connection is made, a blue Power LED (D1) lights indicating the board is powered on.
5. The demonstration design automatically loads and drive the LED array in a repeating pattern.

To load the FTDI chip USB hardware drivers via the stand-alone package on a Windows system:

1. Download the FTDI Chip USB Hardware Drivers package from the Lattice website.
2. Extract the FTDI chip USB Hardware driver package to your PC hard drive.
3. Connect the USB cable from a USB port on your PC to the board's USB mini-B socket (J2). After the connection is made, a blue Power LED (D1) lights indicating the board is powered on.
4. If you are prompted, *Windows may connect to Windows Update* select **No, not this time** from available options and click Next to proceed with the installation. Choose the **Install from specific location (Advanced)** option and click **Next**.
5. Search for the best driver in these locations and click the **Browse** button to browse to the Windows driver folder created in the Download Windows USB Hardware Drivers section. Select the **CDM 2.04.06 WHQL Certified** folder and click **OK**.
6. Click **Next**. A screen displays as Windows copies the required driver files. Windows display a message indicating that the installation was successful.
7. Click **Finish** to install the USB driver.
8. The demonstration design automatically loads and drive the LED array in a repeating pattern.

See the Troubleshooting section of this guide if the board does not function as expected.

6.2. Download Demo Designs

The counter demo is preprogrammed into the board, however over time it is likely your board is modified. Lattice distributes source and programming files for demonstration designs compatible with the Starter Kit. The demo design for the board is available on the web.

To download demo designs:

1. In the Lattice website, browse to Development Kits and Boards. Go to the MachXO3L Starter Kit, the MachXO3LF Starter Kit, or the MachXO2ZE Breakout Board web page. In the Documentation section, select the **Design File** tab. Select **MachXO3L Starter Kit Demo Program, the MachXO3LF Starter Kit Demo Program,** or the **MachXO2 Starter Kit Demo Program** and save the file.
2. Extract the contents of *MachXO3L_Starter_Kit.zip*, the *MachXO3LF_Starter_Kit.zip,* or the *MachXO2_Starter_Kit.zip* to an accessible location on your hard drive.
3. Open the Blink.ldf project file in the Lattice Diamond design software.
4. Run the Process Flow and regenerate the Bitstream file.

Continue to Programming a Demo Design with the Lattice Diamond Programmer.

6.3. Programming a Demo Design with the Lattice Diamond Programmer

The demonstration design is pre-programmed into the MachXO2/MachXO3 board by Lattice. If you have changed the design but now want to restore the board to factory settings, use the procedure described below.

To program the MachXO2/MachXO3 device:

1. Install, license and run Lattice Diamond software. See http://www.latticesemi.com/latticediamond for download and licensing information.
2. Connect the USB cable to the host PC and the MachXO3 board.

3. From Diamond, open the *Blink.ldf* project file.
4. Click the **Programmer** icon.
5. Click **Detect Cable**. The Programmer detects the cable (Cable: USB2, Port: FTUSB-0). If the cable is not detected, see the Troubleshooting section.
6. Click **Device Properties**.
7. Change Access Mode to **SPI Flash Programmi**ng.
8. Choose **SPI Flash Background Erase**, **Program**, **Verify** (MachXO3L) or **FLASH Erase, Program, Verify** (MachXO2 and MachXO3LF) operation.
9. Select **Blink_impl1.bit** (MachXO3L) or **Blink_impl1.jed** (MachXO2 and MachXO3LF) programming file.
10. (MachXO3L only) Under SPI Flash Options, change Vendor to **SPANSION** or **ON Semi** (as appropriate), and change Device to **SPI-S25FL204K** or **S25FL208K** or **LE25U40CMDTWG** (as appropriate). Click **OK**.
11. Click the **Program** icon. When complete, **PASS** is displayed in the Status column.
12. Change Access mode to **NVCM Programming Mode** and **NVCM Refresh**, then click **Program** (or power-cycle the Starter Kit board) to initiate a re-boot from the SPI flash.

7. MachXO2 and MachXO3 Starter Kits

This section describes the features of the MachXO2 and MachXO3 Starter Kits in detail.

7.1. Overview

The Starter Kit is a complete development platform for the MachXO2 and MachXO3 FPGAs. The board includes a prototyping area, a USB program/power port, an LED array, switches, and header landings with electrical connections to most of the FPGA's programmable I/O, power, and configuration pins. The board is powered by the PC's USB port or optionally with external power. You may create or modify the program files and reprogram the board using Lattice Diamond software.

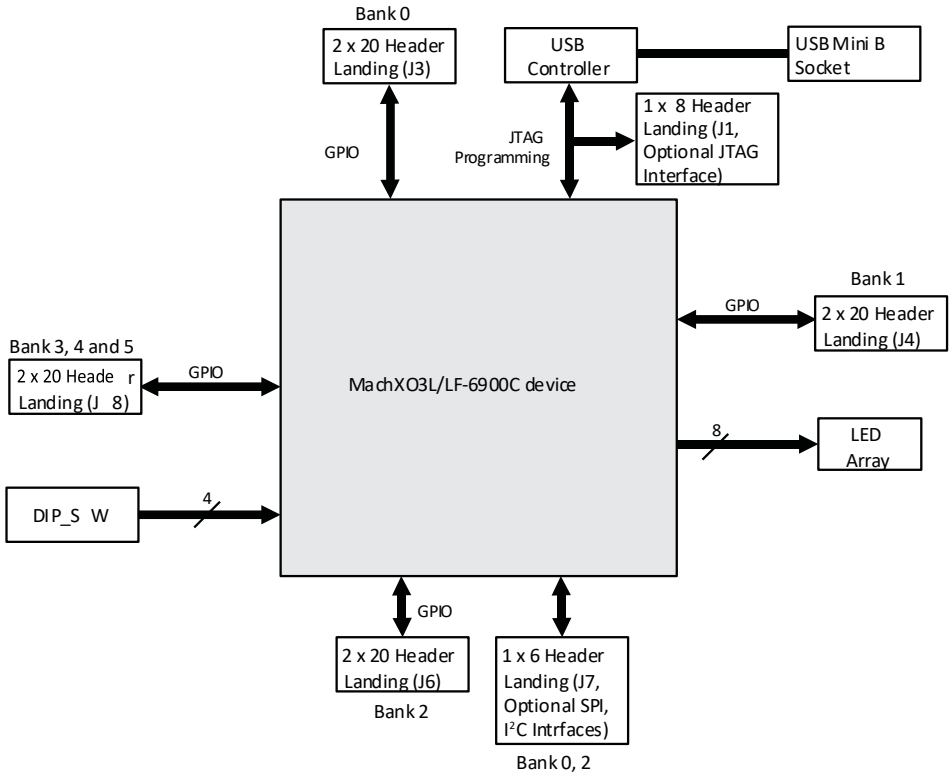


Figure 7.1. MachXO2 and MachXO3L/LF-6900C Block Diagram

Table 7.1 describes the components on the board and the interfaces it supports.

Table 7.1. Starter Kit Components and Interfaces

Component/Interface	Type	Schematic Reference	Description
Circuits			
USB Controller	Circuit	U1: FT2232H	USB-to-JTAG interface and dual USB UART/FIFO IC
USB Mini-B Socket	I/O	J2:USB_MINI_B	Programming and debug interface
Components			
LCMXO2, LCMXO3L, or LCMXO3LF	FPGA	U5: LCMXO2-4000ZE-1BG256C, LCMXO3L-6900C-5BG256C or LCMXO3LF-6900C-5BG256C	4000-LUT and 6900-LUT devices are in a 14 mm x 14 mm, 256-ball caBGA package.
Interfaces			
LED Array	Output	D9-D2	Red LEDs
Push Button Switch	Input	SW1	Momentary User Input
4-position DIP Switch	Input	SW2	User inputs
Four 2 x 20 Header Landings	I/O	J3: header_2x20 J4: header_2x20 J6: header_2x20 J8: header_2x20	User-definable I/O
1 x 8 Header Landing	I/O	J1: header_1x8	Optional JTAG interface
1 x 6 Header Landing	I/O	J7: header_1x6	Optional SPI/I^2C interfaces
4 x 10 40-Hole Prototype Area	—	—	Prototype area 100 mil centered holes.
Test Points	Power	TP1: +3.3 V TP2: +1.2 V TP3: GND	Power and ground reference points

7.2. Subsystems

This section describes the principle subsystems for the Starter Kit in alphabetical order.

7.2.1. Clock Sources

Clock sources for the LED demonstration designs originate from the MachXO2/MachXO3 on-chip oscillator or the 12 MHz crystal X1. You may use an expansion header landing to drive a FPGA input with an external clock source.

7.2.2. Expansion Header Landings

The expansion header landings provide access to user GPIOs, primary inputs, clocks, and VCCO pins of the MachXO2/MachXO3 device. The remaining pins serve as power supplies for external connections. Each landing is configured as one 2 x 20 100 mil.

Table 7.2. Expansion Connector Reference

Item	Description
Reference Designators	J3, J4, J6, J8
Part Number	header_2x20

Table 7.3. Expansion Header Pin Information (J3)

Header Pin Number	-4000 Function	-6900C Function	MachXO3 Ball
1	VCCIO0	VCCIO0	D5,D12,G8,G9
2	VCCIO0	VCCIO0	D5,D12,G8,G9
3	PT28C/INITn	PT36C/INITn	A13
4	PT28D/DONE	PT36D/DONE	C13
5	PT20A	PT22A	F8
6	PT27B	PT35B	B12
7	PT27A	PT35A	C12
8	PT22B	PT26B	E11
9	PT23B	PT27B	E10
10	PT23A	PT27A	D10
11	GND	GND	—
12	GND	GND	—
13	PT22A	PT26A	F9
14	PT23C/JTAGENB	PT27C/JTAGENB	C10
15	PT15B	PT17B	E8
16	PT19B	PT21B	E9
17	PT13B	PT14B	E7
18	PT19A	PT21A	D8
19	PT14D	PT16B	D7
20	PT14B	PT15B	C7
21	GND	GND	—
22	GND	GND	—
23	PT10B	PT10B	C5
24	PT13A	PT14A	D6
25	PT14C	PT16A	E6
26	PT9A	PT9A	C4
27	PT21B	PT25B	A10
28	PT15A	PT17A	F7
29	PT20B	PT22B	D9
30	PT21A	PT25A	B9
31	GND	GND	—
32	GND	GND	—
33	PT11B	PT11B	B6
34	PT14A	PT15A	B7
35	PT9B	PT9B	B5
36	PT11A	PT11A	A5
37	PT12B	PT12B	B4
38	PT10A	PT10A	A4
39	GND	GND	—
40	PT12A	PT12A	A3

Table 7.4. Expansion Header Pin Information (J4)

Header Pin Number	-4000 Function	-6900C Function	MachXO3 Ball
1	VCCIO1	VCCIO1	E13,H10,J10,M13
2	VCCIO1	VCCIO1	E13,H10,J10,M13
3	PR15D	PR19D	K12
4	PR15C	PR19C	K13
5	PR18A	PR23A	M14
6	PR19B	PR24B	N14
7	PR15B	PR18B	L14
8	PR19A	PR24A	N16
9	PR18B	PR23B	M15
10	PR16B	PR21B	M16
11	GND	GND	—
12	GND	GND	—
13	PR16A	PR21A	L15
14	PR15A	PR18A	L16
15	PR14A	PR17A	K14
16	PR13B	PR16B	K16
17	PR14B	PR17B	K15
18	PR10D	PR15B	J14
19	PR10A/PCLKT1_0	PR12A/PCLKT1_0	H14
20	PR13A	PR16A	J15
21	GND	GND	—
22	GND	GND	—
23	PR10C	PR15A	J16
24	PR9B	PR11B	H15
25	PR10B/PCLKC1_0	PR12B/PCLKC1_0	H16
26	PR8A	PR9A	G15
27	PR9A	PR11A	G16
28	PR5B	PR5B	F15
29	PR6B	PR7B	F16
30	PR2B	PR2B/R_GPLLC_FB	E15
31	GND	GND	—
32	GND	GND	—
33	PR5A	PR5A	E16
34	PR3B/R_GPLLC_IN	PR3B/R_GPLLC_IN	E14
35	PR3A/R_GPLLT_IN	PR3A/R_GPLLT_IN	D16
36	PR2C	PR2C	C15
37	PR2A/R_GPLLT_FB	PR2A/R_GPLLT_FB	D14
38	PR6A	PR7A	F14
39	PR8B	PR9B	G14
40	PR2D	PR2D	B16

Table 7.5. Expansion Header Pin Information (J6)

Header Pin Number	-4000 Function	-6900C Function	MachXO3 Ball
1	VCCIO2	VCCIO2	K8,K9,N5,N12
2	VCCIO2	VCCIO2	K8,K9,N5,N12
3	PB27B	PB35B	T12
4	PB26B	PB34B	T14
5	PB27A	PB35A	R11
6	PB26A	PB34A	R13
7	PB24A	PB31A	T11
8	PB23D	PB28B	M11
9	PB24B	PB31B	P11
10	PB23C	PB28A	N10
11	GND	GND	—
12	GND	GND	—
13	PB21B	PB26B	T10
14	PB23A	PB29A	P10
15	PB21A	PB26A	R9
16	PB23B	PB29B	R10
17	PB20A	PB23A/PCLKT2_1	T9
18	PB18B	PB21B	N9
19	PB20B/PCLKC2_1	PB23B/PCLKC2_1	P9
20	PB18A	PB21A	M8
21	GND	GND	—
22	GND	GND	—
23	PB15B	PB18B	T8
24	PB12B	PB15B	L8
25	PB15A	PB18A	P8
26	PB12A	PB15A	M6
27	PB10A	PB13A	R7
28	PB13B/PCLKC2_0	PB16B/PCLKC2_0	R8
29	PB10B	PB13B	P7
30	PB13A/PCLKT2_0	PB16A/PCLKT2_0	T7
31	GND	GND	—
32	GND	GND	—
33	PB9D	PB10B	L7
34	PB7B	PB9B	R6
35	PB9C	PB10A	N6
36	PB7A	PB9A	T5
37	PB6B	PB7B	R4
38	PB3A	PB4A	P4
39	PB6A	PB7A	T3
40	PB3B	PB4B	T4

Table 7.6. Expansion Header Pin Information (J8)

Header Pin Number	-4000 Function	-6900C Function	MachXO3 Ball
1	VCCIO5	VCCIO5	E4
2	VCCIO3	VCCIO3	M4
3	PL8D	PL9D	H6
4	PL20B	PL25B	N3
5	PL20A	PL25A	M2
6	PL17B/PCLKC3_0	PL22B/PCLKC3_0	M1
7	PL17A/PCLKT3_0	PL22A/PCLKT3_0	L2
8	PL16A	PL19A	L1
9	PL16B	PL19B	L3
10	PL16D	PL19D	L5
11	GND	GND	—
12	GND	GND	—
13	PL16C	PL19C	K4
14	PL10C/PCLKT4_0	PL12A/PCLKT4_0	J1
15	PL13B	PL15B	K1
16	PL13A	PL15A	J2
17	PL10D/PCLKC4_0	PL12B/PCLKC4_0	J3
18	PL10A	PL11A	H3
19	PL9B	PL10B	H2
20	PL10B	PL11B	H1
21	GND	GND	—
22	GND	GND	—
23	PL8A	PL9A	G2
24	PL9A	PL10A	G1
25	PL6B/PCLKC5_0	PL6B/PCLKC5_0	F2
26	PL7B	PL8B	F1
27	PL4A/L_GPLLT_IN	PL4A/L_GPLLT_IN	E2
28	PL6A/PCLKT5_0	PL6A/PCLKT5_0	E1
29	PL4D	PL4D	D2
30	PL3B/L_GPLLC_FB	PL3B/L_GPLLC_FB	D1
31	GND	GND	—
32	PL2D	PL2D	C2
33	PL4C	PL4C	C1
34	PL8B	PL9B	G3
35	PL2C	PL2C	B1
36	PL3A/L_GPLLT_FB	PL3A/L_GPLLT_FB	D3
37	PL4B/L_GPLLC_IN	PL4B/L_GPLLC_IN	E3
38	PL7A	PL8A	F3
39	PL8C	PL9C	F5
40	VCCIO4	VCCIO4	H7,J7

J3

1	2
VCCIO0	VCCIO0
A13	C13
F8	B12
C12	E11
E10	D10
GND	GND
F9	C10
E8	E9
E7	D8
D7	C7
GND	GND
C5	D6
E6	C4
A10	F7
D9	B9
GND	GND
B6	B7
B5	A5
B4	A4
GND	A3
39	40

J4

1	2
VCCIO1	VCCIO1
K12	K13
M14	N14
L14	N16
M15	M16
GND	GND
L15	L16
K14	K16
K15	J14
H14	J15
GND	GND
J16	H15
H16	G15
G16	F15
F16	E15
GND	GND
E16	E14
D16	C15
D14	F14
G14	B16
39	40

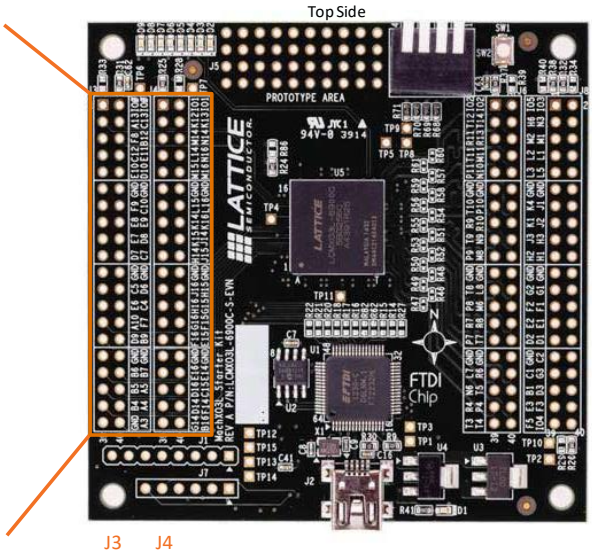
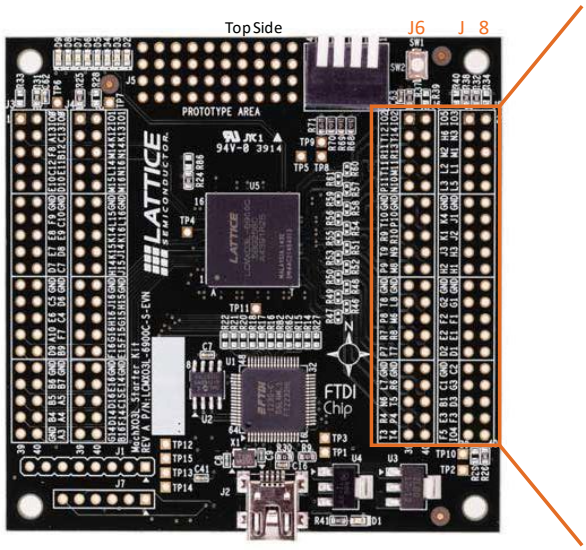


Figure 7.2. J3/J4 Header Landing Callout



J6

1	2
VCCIO2	VCCIO2
T12	T14
R11	R13
T11	M11
P11	N10
GND	GND
T10	P10
R9	R10
T9	N9
P9	M8
GND	GND
T8	L8
P8	M6
R7	R8
P7	T7
GND	GND
L7	R6
N6	T5
R4	P4
T3	T4
39	40

J8

1	2
VCCIO5	VCCIO3
H6	N3
M2	M1
L2	L1
L3	L5
GND	GND
K4	J1
K1	J2
J3	H3
H2	H1
GND	GND
G2	G1
F2	F1
E2	E1
D2	D1
GND	GND
C1	G3
B1	D3
E3	F3
F5	VCCIO4
39	40

Figure 7.3. J6/J8 Header Landing Callout

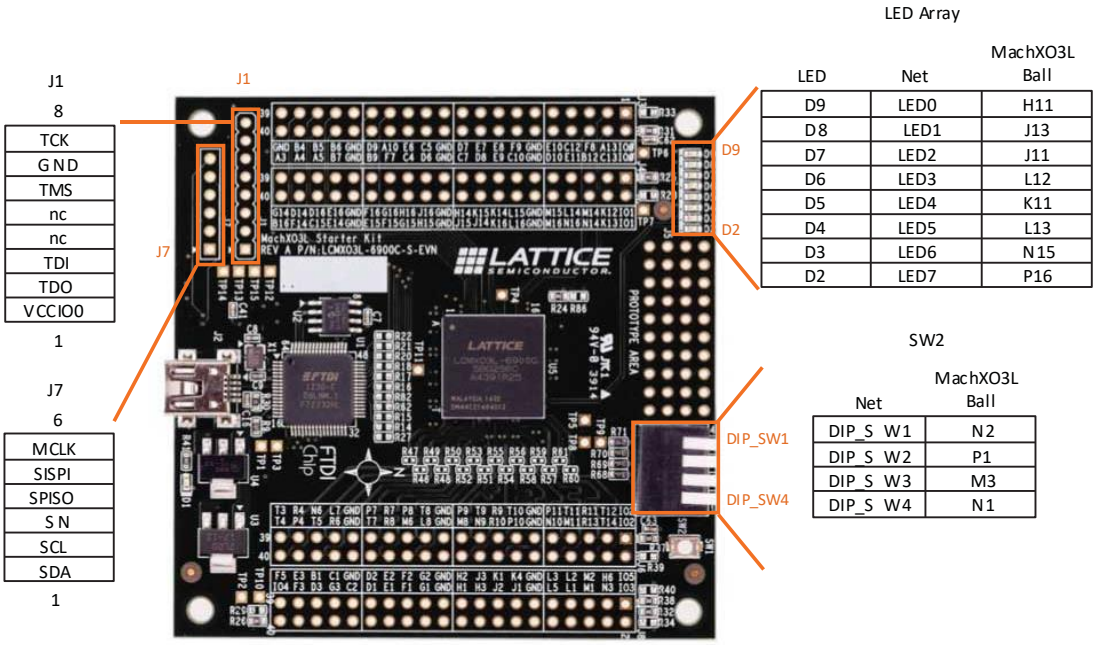


Figure 7.4. J1 Header Landing and LED Array Callout

7.2.3. MachXO2/MachXO3 FPGA

The LCMXO2-4000ZE-1BG256C and LCMXO3L/LF-6900C-5BG256C are 256-ball caBGA package FPGA devices which provide up to 206 usable I/O in a 14 mm x 14 mm package. 150 I/O are accessible from the board headers, switches, and LEDs.

Table 7.7. MachXO2 and MachXO3 FPGA Interface Reference

Item	Description
Reference Designators	U5
Part Number	LCMXO2-4000ZE-1BG256C (Flash), LCMXO3L-6900C-5BG256C (NVCM) or LCMXO3LF-6900C-5BG256C (Flash)
Manufacturer	Lattice Semiconductor
Web Site	www.latticesemi.com

7.2.4. Programming Interface Circuits

For power and programming an FTDI USB UART/FIFO IC converter provides a communication interface between a PC host and the JTAG programming chain of the Starter Kit. The USB 5 V supply is also used as a source for the 3.3 V supply rail. A USB mini-B socket is provided for the USB connector cable.

Table 7.8. USB/JTAG Interface Reference

Item	Description
Reference Designators	U1
Part Number	FT2232HL
Manufacturer	Future Technology Devices International (FTDI)
Web Site	www.ftdichip.com

Table 7.9. JTAG Programming Pin Information

Description	MachXO3 Pin
Test Data Output	C6:TDO
Test Data Input	A6:TDI
Test Mode Select	B8:TMS
Test Clock	A7:TCK

Table 7.10. SPI Programming Pin Information

Description	MachXO3 Pin
Master Clock/Config Clock	P6:MCLK/CCLK
Serial Data Input	P13: SI/SISPI
Serial Data Output	T6: SO/SPISO
SPI Slave Select	R12: SN

Table 7.11. I^2C Programming Pin Information

Description	MachXO3 Pin
Serial Data	C9:SDA
Serial Clock	A9:SCL

7.2.5. LEDs

A blue LED (D1) is used to indicate USB 5V power. Eight red LEDs are driven by I/O pins of the MachXO2/MachXO3 device.

Table 7.12. Power and User LEDs Reference

Item	Description
Reference Designators	Red LEDs (D2, D3, D4, D5, D6, D7, D8, D9) Blue LEDs (D1)
Part Number	LTST-C190KRKT (D2-D9) LTST-C190TBKT (D1)
Manufacturer	Lite-On It Corporation
Web Site	www.liteonit.com

7.2.6. Power Supply

3.3 V and 1.2 V power supply rails are converted from the USB 5 V interface when the board is connected to a host PC.

7.2.7. Test Points

In order to check the various voltage levels used, the following test points are provided:
TP1: +3.3 V
TP2: +1.2 V
TP3: GND

7.2.8. USB Programming and Debug Interface

The USB Mini-B socket of the Starter Kit serves as the programming and debug interface. For JTAG programming, a pre-programmed USB PHY peripheral controller is provided on the Starter Kit to serve as the programming interface to the MachXO2/MachXO3 FPGA. Programming requires the Lattice Diamond or ispVM System software.

Table 7.13. USB Interface Reference

Item	Description
Reference Designators	U1
Part Number	FT2232HL
Manufacturer	Future Technology Devices International (FTDI)
Web Site	www.ftdichip.com

7.3. Board Modifications

This section describes modifications to the board to change or add functionality.

7.3.1. Bypassing the USB Programming Interface

The USB programming interface circuit (USB Programming and Debug Interface section) may be optionally bypassed by removing the 0 Ω resistors: R4, R5, R6, R7 (See Figure A.2). Header landing J1 provides JTAG signal access for jumper wires or a 1 x 8 pin header.

7.3.2. Applying External Power

The Starter Kit is powered by the circuit shown in Figure A.3, based on the 5 V USB power source. You may disconnect this power source by removing the 0 Ω resistors: R35 (VCC_1.2 V) and R42 (VCC_3.3 V). Power connections are available from the test points, TP1 (+3.3 V) and TP2 (+1.2 V). When this power mode is used, the FTDI oscillator will be shut off.

7.3.3. Measuring Bank and Core Power

Test points (TP1, TP2) provide access to power supplies of the MachXO2/MachXO3 FPGA. Inline 1 Ω resistors: R31 (VCCIO0, +3.3 V, Bank 0), R25 (VCCIO1, +3.3 V, Bank 1), R37 (VCCIO2, +3.3 V, Bank 2), R32 (VCCIO3, +3.3 V, Bank 3), R26 (VCCIO4, +3.3 V, Bank 4), R38 (VCCIO5, +3.3 V, Bank 5), R24 (VCC core, +1.2 V) can be used to measure current for the power supplies.

7.4. Mechanical Specifications

Dimensions: 3 in. [L] x 3 in. [W] x 1/2 in. [H]

7.5. Environmental Requirements

The evaluation board must be stored between -40° C and 100° C. The recommended operating temperature is between 0° C and 90° C.

8. Troubleshooting

Use the tips in this section to diagnose problems with the Starter Kit.

8.1. LEDs Do Not Flash

If power is applied but the board does not flash according to the preprogrammed counter demonstration, then it is likely the board has been reprogrammed with a new design. Follow the directions in the Demonstration Design section to restore the factory default.

8.2. USB Cable Not Detected

If Lattice Diamond Programmer or ispVM System does not recognize the USB cable after installing the Lattice USB port drivers and rebooting, the incorrect USB driver may have been installed. This usually occurs if you attach the board to your PC prior to installing the Lattice-supplied USB driver.

8.3. Accessing the Troubleshooting the USB Driver Installation Guide

To access the installation guide for Diamond software and standalone Diamond Programmer:

1. Start Diamond or Diamond Programmer and choose **Help**.
2. Search for **USB driver** or **Troubleshooting**, then select the **Troubleshooting the USB Driver** topic.
3. Follow the directions to install the Lattice USB driver.

To access the installation guide for ispVM:

1. Start ispVM System and choose **Options > Cable and I/O Port Setup**. The Cable and I/O Port Setup Dialog appears.
2. Click the **Troubleshooting the USB Driver Installation Guide** link. The Troubleshooting the USB Driver Installation Guide document appears in your system's PDF file reader.
3. Follow the directions to install the Lattice USB driver.

An alternate failure mode can occur when the user design assigns an output signal to the FPGA package pin C8 which is connected the oscillator (X1) output signal *12 MHz*. This can occur unintentionally when the Placer randomly assigns unconstrained outputs. In this case, the contention squelches the FTDI device (U1) clock input, rendering it unable to communicate. To eliminate the contention, remove the resistor R23. This restores the FTDI device operation and allow the erasure of the offending FPGA image. Resistor R23 should be reinstalled if an external clock source is desired.

8.4. Determine the Source of a Pre-Programmed Device

If the Starter Kit has been reprogrammed, the original demo design can be restored. To restore the board to the factory default, see the Download Demo Designs section for details on downloading and reprogramming the device.

9. Ordering Information

Table 9.1. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
MachXO3L Starter Kit	LCMXO3L-6900C-S-EVN	
MachXO3L Starter Kit	LCMXO3LF-6900C-S-EVN	
MachXO2 Starter Kit	LCMXO2-4000ZE-B-EVN	

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Appendix A. Schematic Diagrams

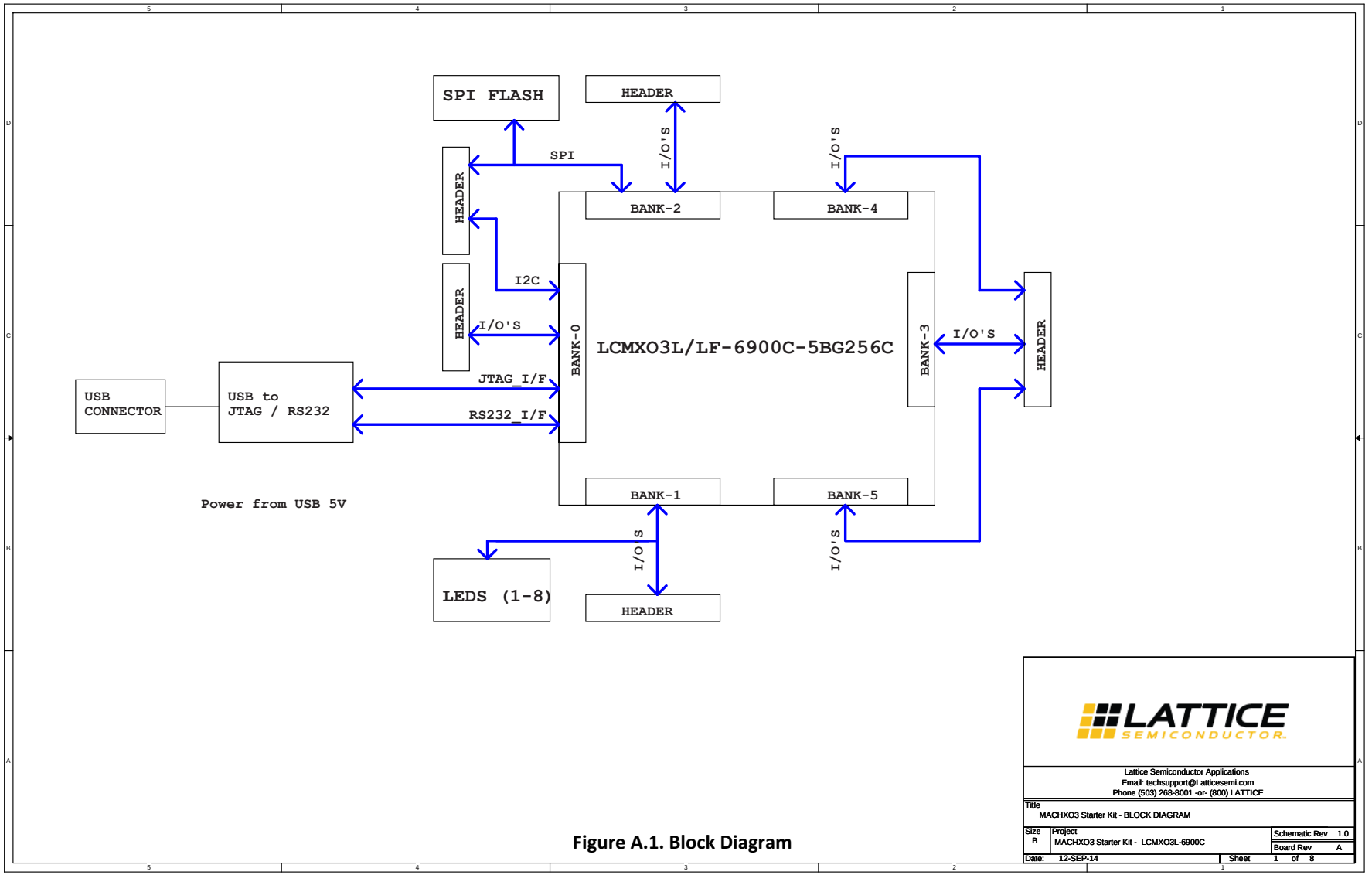


Figure A.1. Block Diagram

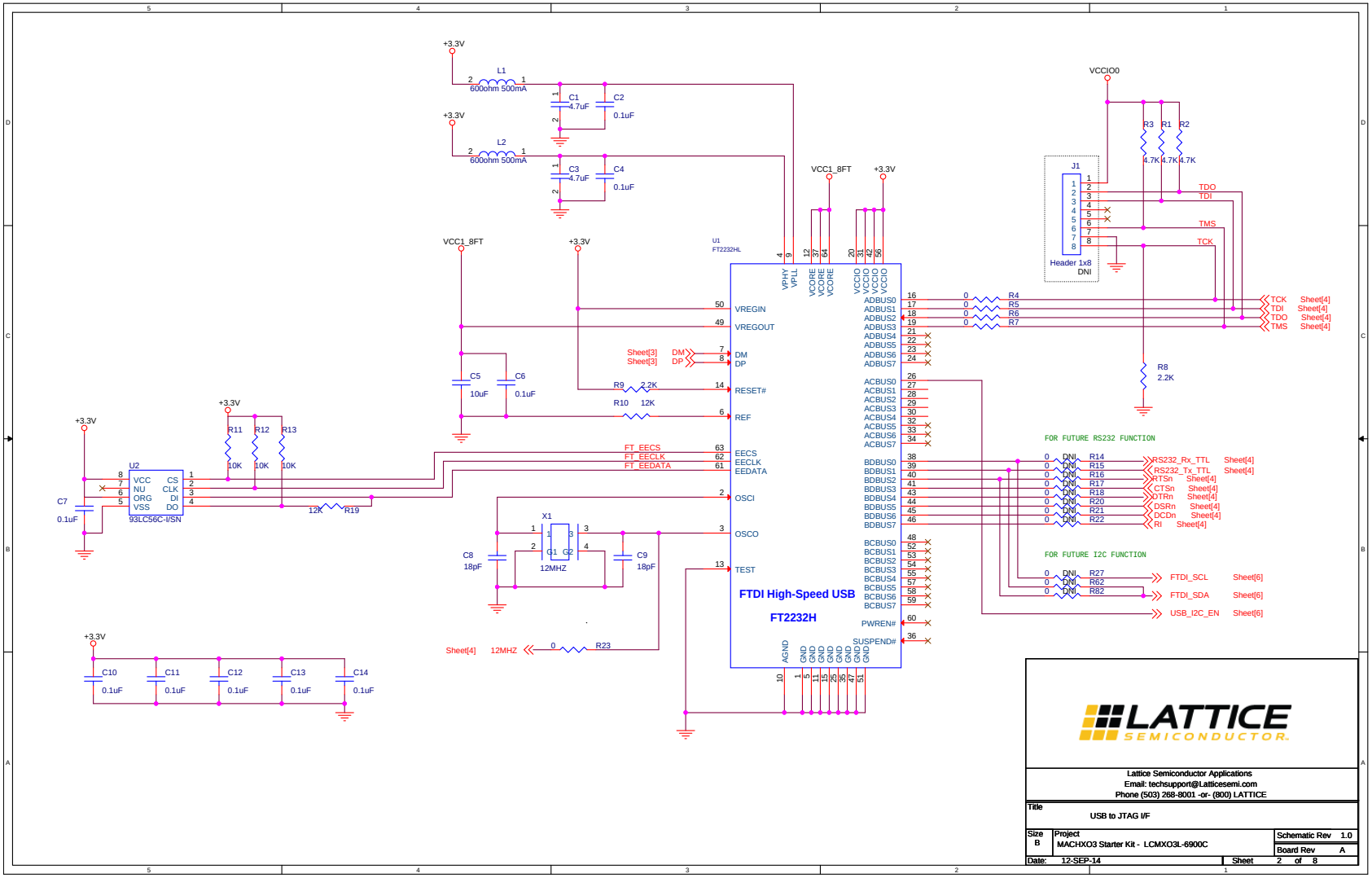


Figure A.2. USB Interface to JTAG

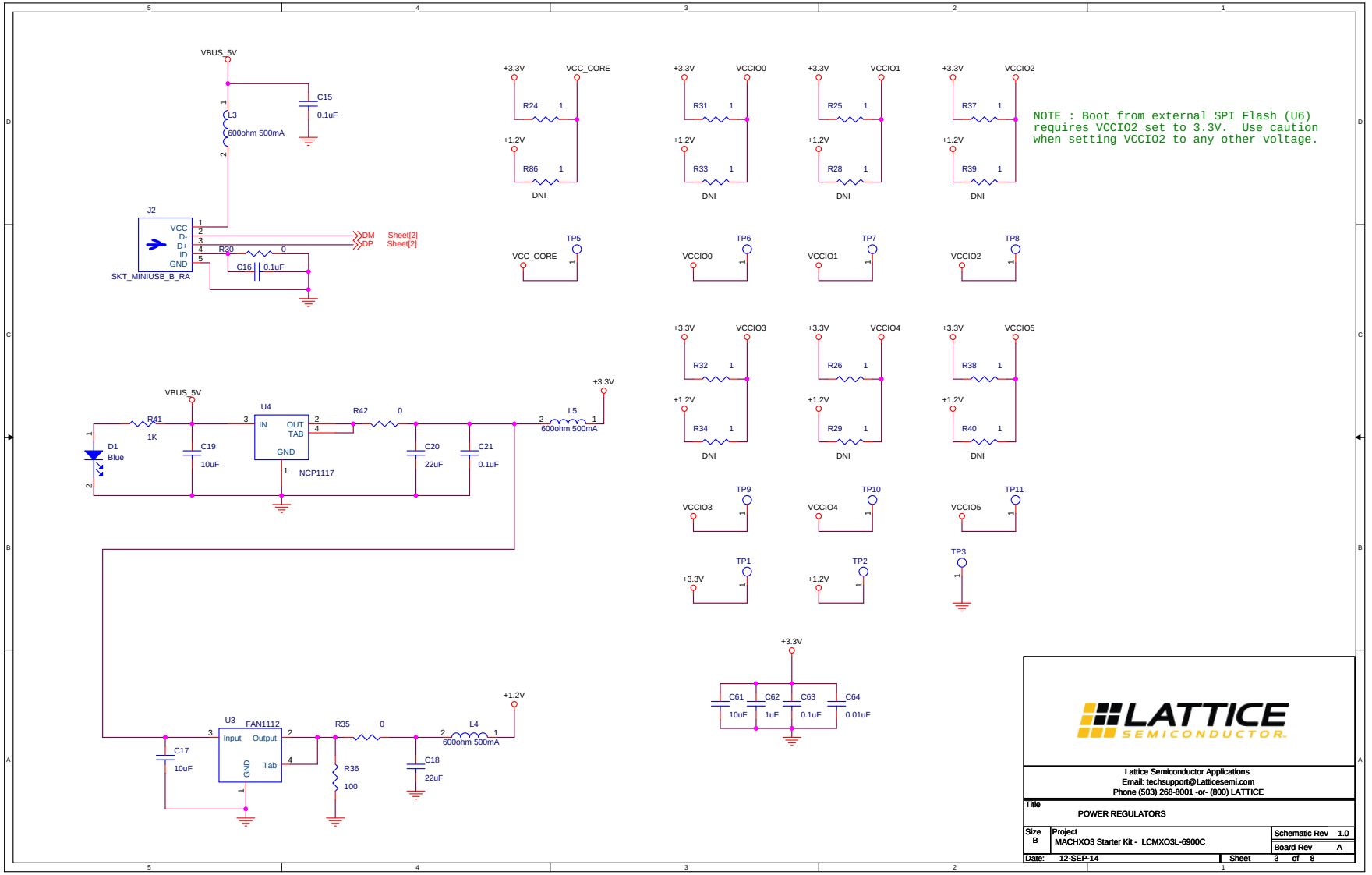


Figure A.3. FPGA

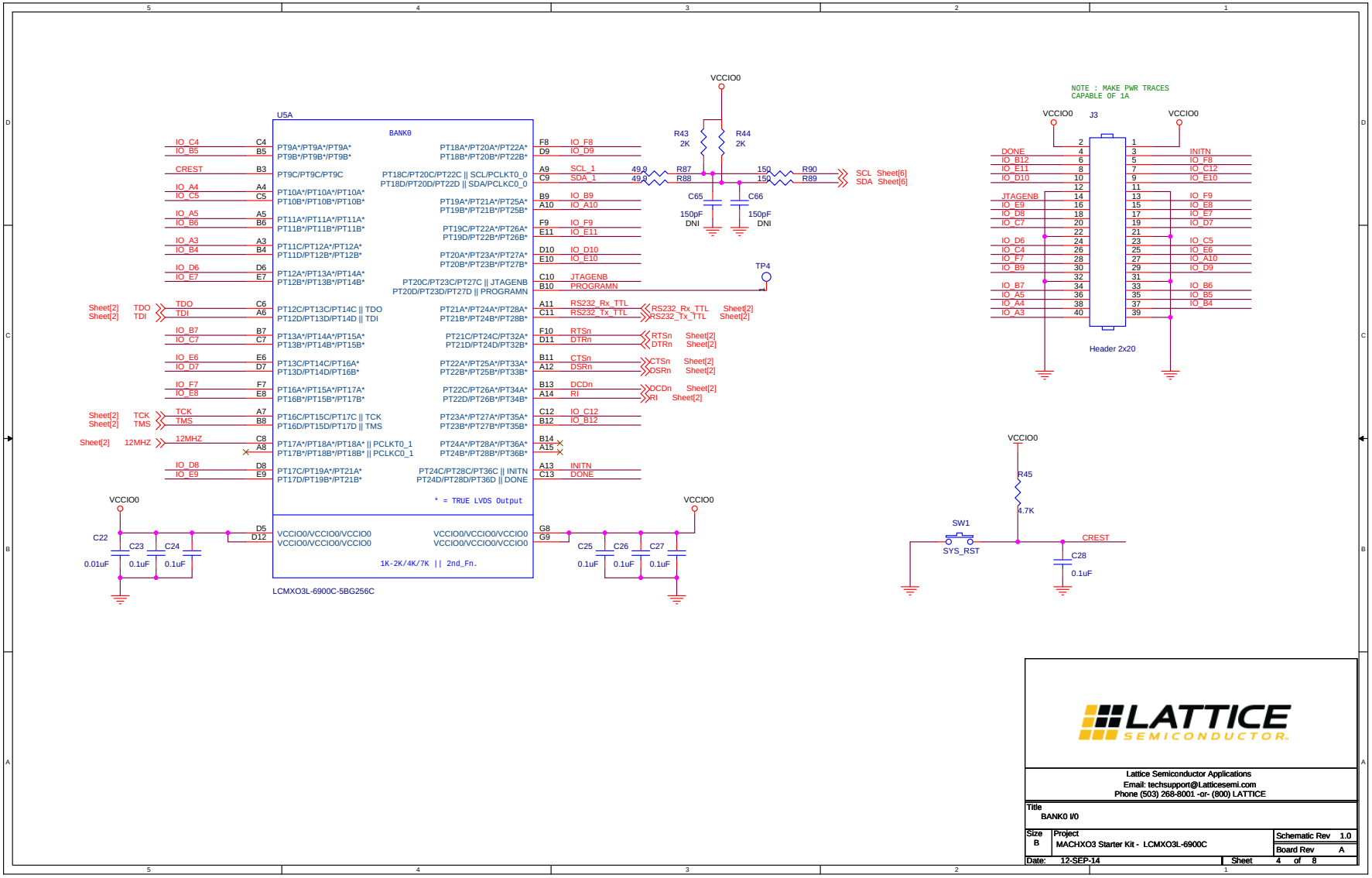


Figure A.4. FPGA

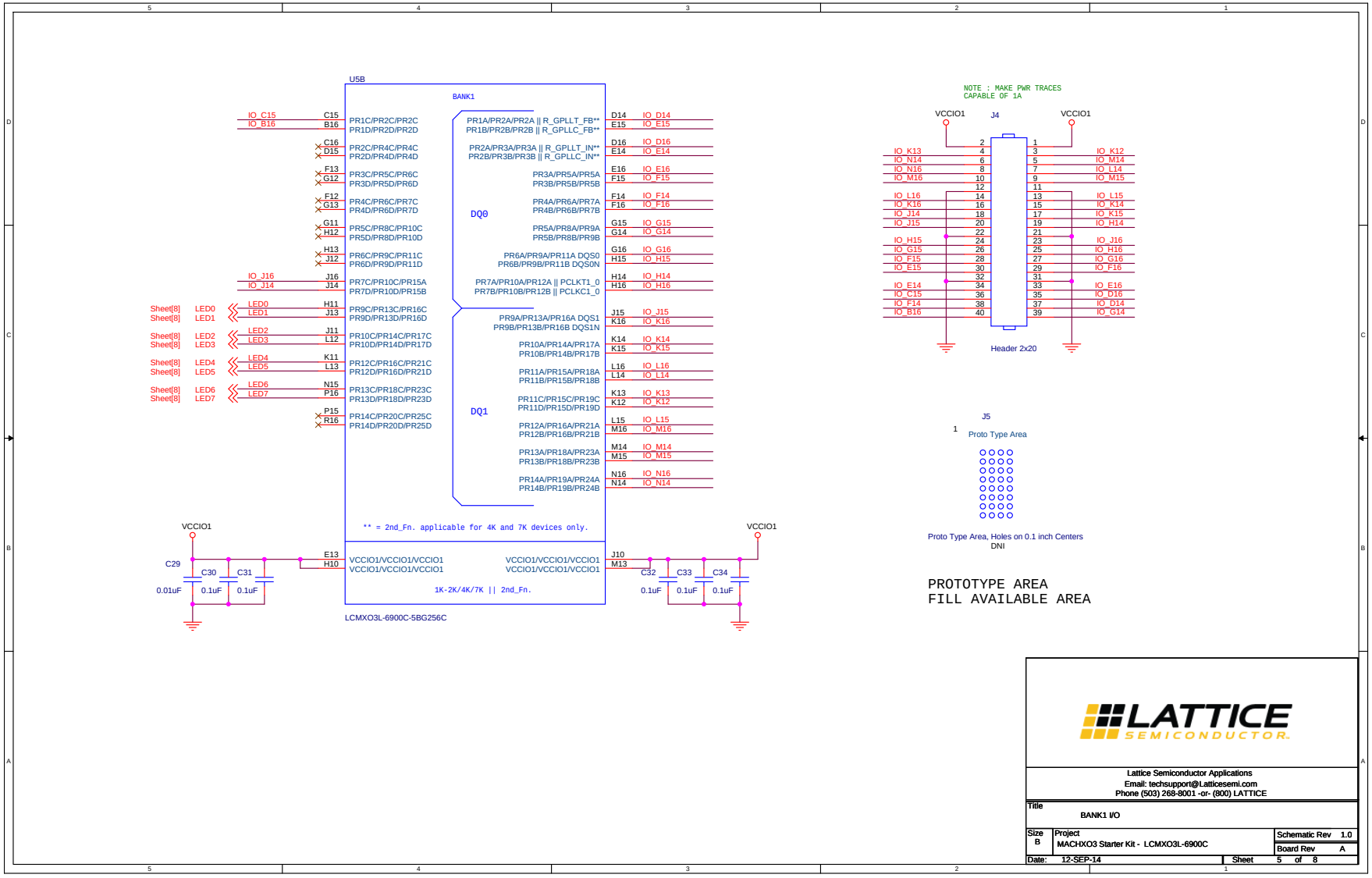


Figure A.5. Power LEDs

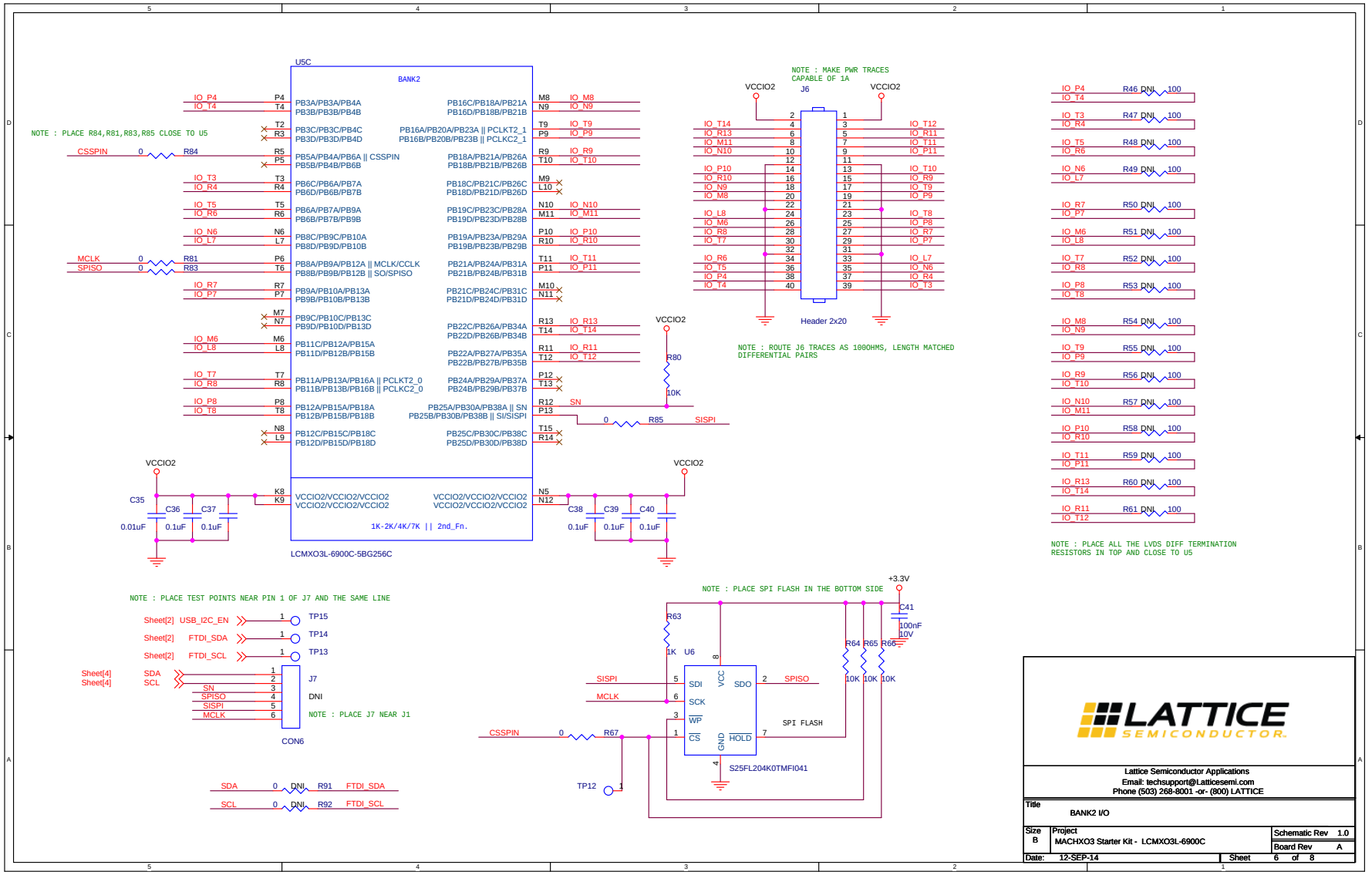


Figure A.6. Bank 2 I/O

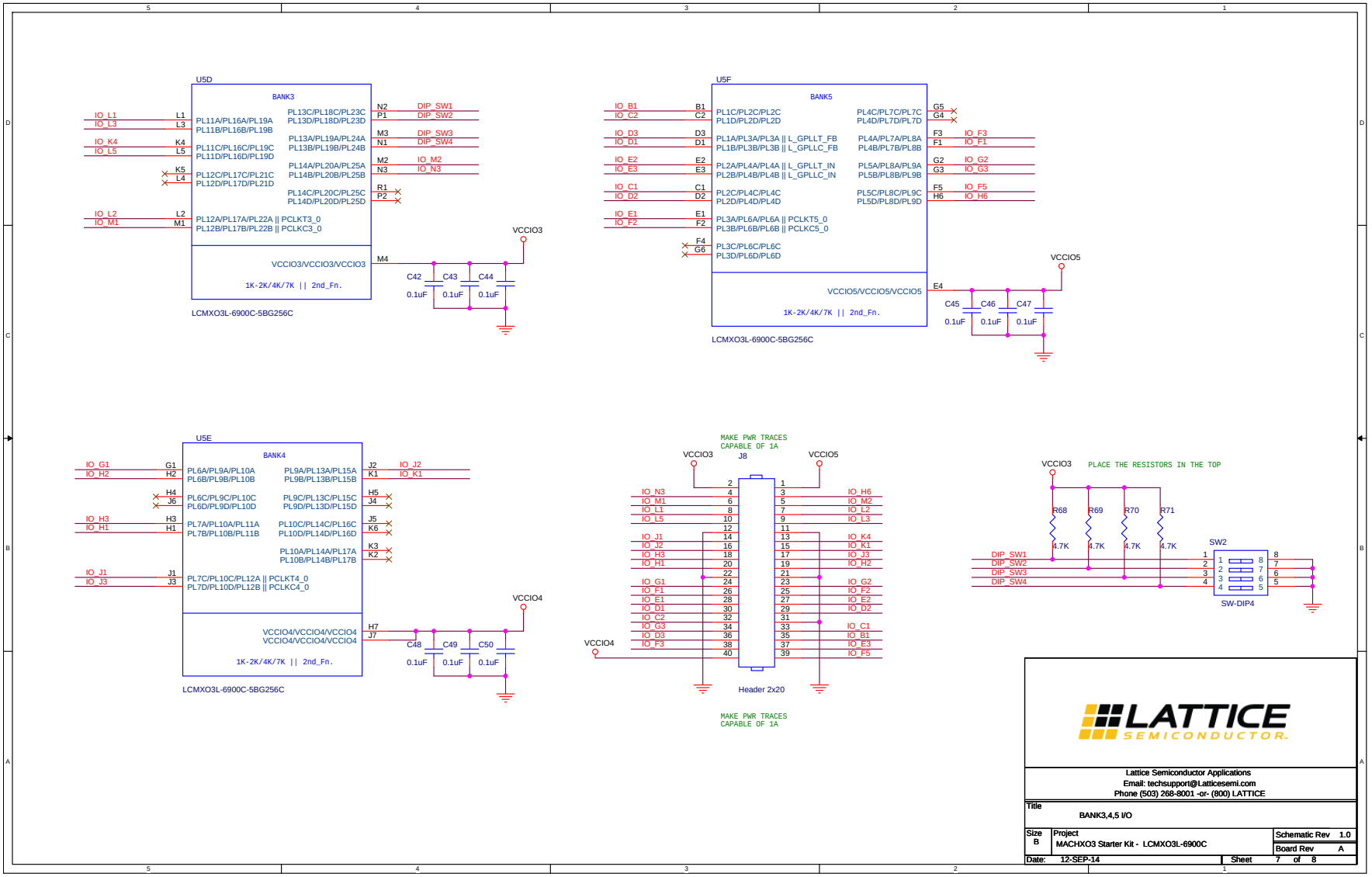


Figure A.7. Bank 3, 4, 5 I/O

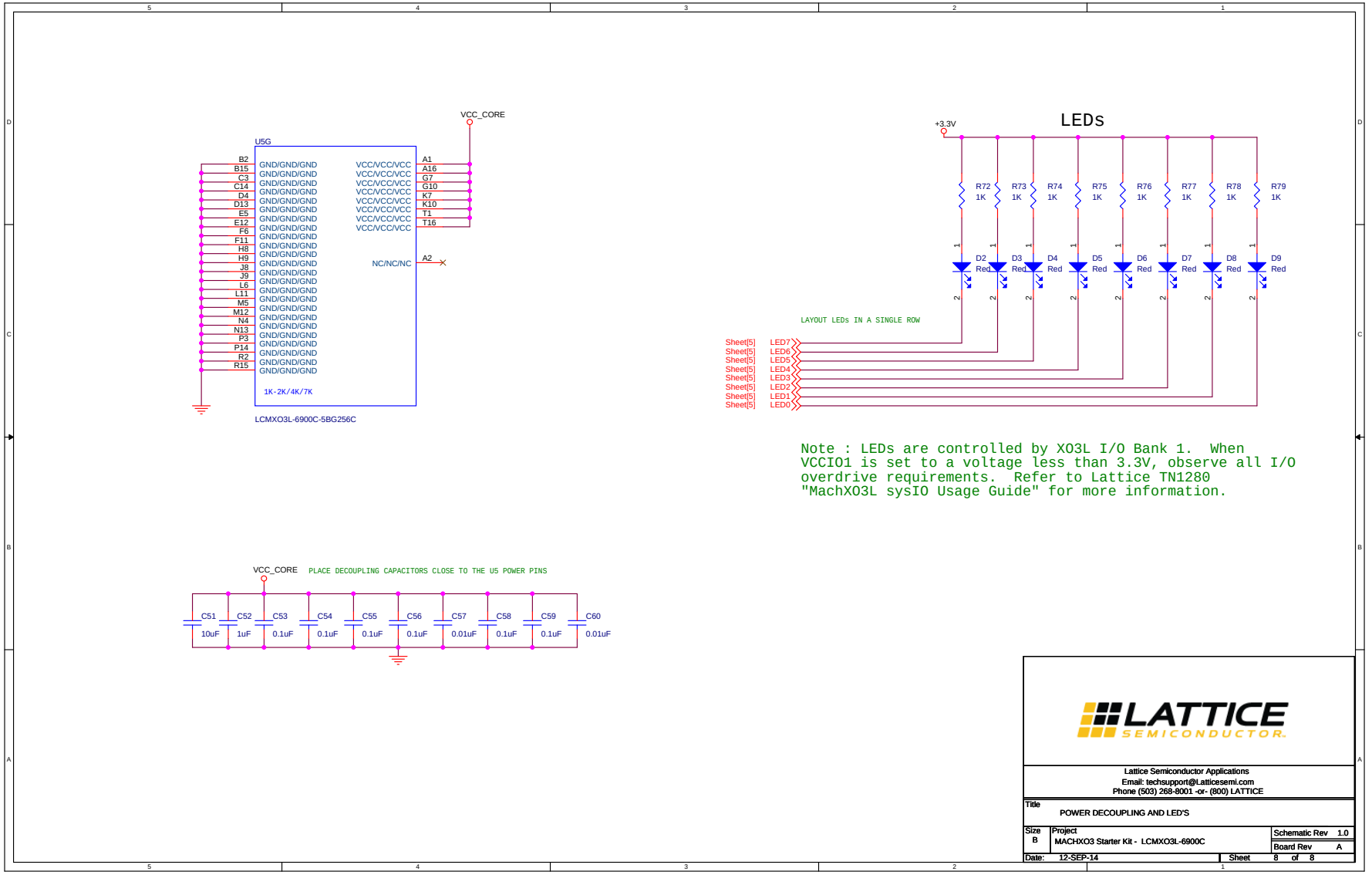


Figure A.8. Power Decoupling and LEDs

Appendix B. Bill of Materials

Item	Quantity	Reference	Value	Manufacturer	MFG Pin
1	2	C1, C3	4.7 uF	Panasonic	ECJ-1VB0J475K
2	44	C2, C4, C6, C7, C10, C11, C12, C13, C14, C15, C16, C21, C23, C24, C25, C26, C27, C28, C30, C31, C32, C33, C34, C36, C37, C38, C39, C40, C42, C43, C44, C45, C46, C47, C48, C49, C50, C53, C54, C55, C56, C58, C59, C63	0.1 uF		C0402C104K4RACTU
3	5	C5, C17, C19, C51, C61	10 uF	Taiyo Yuden	LMK107BJ106MALTD
4	2	C8, C9	18 pF		C0402C180K3GACTU
5	2	C18, C20	22 uF	Taiyo Yuden	LMK212BJ226MG-T
6	6	C22, C29, C35, C57, C60, C64	0.01 uF		C0402C103J4RACTU
7	1	C41	100 nF	Murata	GRM155R61A104KA01D
8	2	C52, C62	1 uF		C0402C105K9PACTU
9	2	C65, C66	150 pF		C0402C104K4RACTU
10	1	D1	Blue	LITE-On INC	LTST-C190TBKT
11	8	D2, D3, D4, D5, D6, D7, D8, D9		LITE-On INC	LTST-C190KRKT
12	1	J1	Header 1 x 8		0022284081
13	1	J2	Mini USB-B	Neltron	5075BMR-05-SM-CR
14	4	J3, J4, J6, J8	Header 2 x 20	Samtec	TSW-120-07-G-D
16	1	J7	Header 1 x 6	Samtec	TSW-106-07-F-S-ND
17	5	L1, L2, L3, L4, L5	600 Ω 500 mA	Murata	BLM18AG601SN1D
18	8	R1, R2, R3, R45, R68, R69, R70, R71	4.7 K	Vishay	CRCW06034K70FKEA
19	13	R4, R5, R6, R7, R23, R30, R35, R42, R67, R81, R83, R84, R85			RC0603JR-070RL
20	2	R8, R9	2.2 K	Vishay	CRCW06032K20FKEA
21	2	R10, R19	12 K		RC0603FR-0712KL
22	7	R11, R12, R13, R64, R65, R66, R80	10 K	Stackpole Electronics Inc	RMCF0603JT10K0
23	13	R14, R15, R16, R17, R18, R20, R21, R22, R27, R62, R82, R91, R92			RC0603JR-070RL
24	7	R24, R25, R26, R31, R32, R37, R38		Vishay	CRCW06031R00JNEAHP
25	7	R28, R29, R33, R34, R39, R40, R86		Vishay	CRCW06031R00JNEAHP
26	1	R36			RC0603FR-07100RL
27	10	R41, R63, R72, R73, R74, R75, R76, R77, R78, R79			RC0603FR-071KL
28	2	R43, R44		Vishay	CRCW06032K00JNEA

Item	Quantity	Reference	Value	Manufacturer	MFG Pin
29	16	R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61			RC0402FR07100RL
30	2	R87, R88	49.9	Vishay	CRCW060349R9FKEA
31	2	R89, R90		Vishay	CRCW0603150RJNEA
32	1	SW1		E-Switch	TL1015AF160QG
33	1	SW2		CTS Electrocomponents	195-4MST
35	1	U1			FT2232HL
36	1	U2		Microchip	93LC56C-I/SN
37	1	U3		Fairchild Semi	FAN1112SX
38	1	U4		On Semi	NCP1117ST33T3G
39	1	U5		Lattice Semiconductor	LCMXO2-4000ZE-1BG256C, LCMXO3L-6900C-5BG256C, or LCMXO3LF-6900C-5BG256C
40	1	U6		Spansion, On Semi	S25FL204K0TMFI041 (early builds) or S25FL208K0RMFI041 (later builds), LE25U40CMDTWG (later builds)
41	1	X1	12 MHz	TXC	7M-12.000MAAJ-T

Revision History

Revision 1.3, September 2021

Section	Change Summary
All	• Changed document number from EB95 to FPGA-EB-02036. • Updated document template. • Added Disclaimers section. • Changed document title from 'MachXO3 Starter Kit'.
Acronyms in This Document	Added this section.
Introduction	Added references to the MachXO2 device and Starter Kit.
Features	Added references to the MachXO2 device and Starter Kit.
MachXO2 and MachXO3 Devices	• Changed section heading from 'MachXO3 Device'. • Added references to the MachXO2 device and Starter Kit. • Added link for the MachXO2 Family Data Sheet to this section.
Demonstration Design	• Updated programming procedure in Programming a Demo Design with the Lattice Diamond Programmer. • Updated the LE25U40CMDTWG MFG Pin in step 10 of Section 6.3 Programming a Demo Design with the Lattice Diamond Programmer. • Added references to the MachXO2 device and Starter Kit. • Added the download procedure the MachXO2 Starter Kit demo design and the link for the MachXO2ZE Breakout Board to Section 6.2. Download Demo Designs.
MachXO2 and MachXO3 Starter Kits	• Changed section heading from 'MachXO3 Starter Kit'. • Added references to the MachXO2 device and Starter Kit. • Changed the figure caption of Figure 7.1. MachXO2 and MachXO3L/LF-6900C Block Diagram from 'MachXO3L/LF-6900C Block Diagram'. • Added information regarding the component LCMXO2, including its schematic reference and its description, to Table 7.1. Starter Kit Components and Interfaces. • Added information regarding the MachXO2 expansion header pin to Table 7.3. Expansion Header Pin Information (J3), Table 7.4. Expansion Header Pin Information (J4), Table 7.5. Expansion Header Pin Information (J6), and Table 7.6. Expansion Header Pin Information (J8). • Changed the heading for Section 7.2.3. MachXO2/MachXO3 FPGA from 'MachXO3 FPGA'. • Changed the table caption for Table 7.7. MachXO2 and MachXO3 FPGA Interface Reference from 'MachXO3 FPGA Interface Reference'. • Added description for the MachXO2 FPGA interface part number to Table 7.7. MachXO2 and MachXO3 FPGA Interface Reference. • Added the sentence ' When this power mode is used, the FTDI oscillator will be shut off.' into Section 7.3.2. Applying External Power.
Ordering Information	Added ordering information for the MachXO2 Starter Kit to Table 9.1. Ordering Information.
Appendix B. Bill of Materials	• Modified item 39 in Appendix B Bill of Materials to add LCMXO2-4000ZE-1BG256C as MFG Pin in the table. • Modified item 40 in Appendix B Bill of Materials to add On Semi and LE25U40CMDTWG (later builds) as manufacturer and MFG Pin, respectively, in the table.

Revision 1.2, March 2016

Section	Change Summary
Demonstration Design	• Indicated external Serial Flash Memory (SPAN-SION S25FL204K or S25FL208K). • Updated Run the Demonstration Design section. Corrected the link to the FTDI Chip USB Hardware Drivers in the procedure for loading the FTDI chip USB hardware drivers via the stand-alone package on a Windows system. • Updated Programming a Demo Design with the Lattice Diamond Programmer section. Modified Device in step 10 of the procedure for programming MachXO3 device. • Updated Download Demo Designs section. Corrected links in the procedure for downloading demo designs.
MackXO3 Starter Kit	Updated Expansion Header Landings section. Revised Figure 7.4. Header Landing and LED Array Callout to correct DIPSW ball callouts.
Appendix B. Bill of Materials	Modified item 40 Spansion MFG Pin in the table.

Revision 1.1, May 2015

Section	Change Summary
All	• Changed document title to MachXO3 Starter Kit User Guide. • Changed instances of MachXO3L to MachXO3. • Indicated MachXO3L and/or MachXO3LF devices and board versions. • Indicated MachXO3 NVCM and/or Flash based devices.
Technical Support Assistance	Updated this section.

Revision 1.0, November 2014

Section	Change Summary
All	Initial release.

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