Memory

- Units of binary data
  - → Smallest unit = 1bit
  - → 1 byte = 8 bits
  - → 1 nibble = 4 bits
  - → 1 byte = 2 nibbles

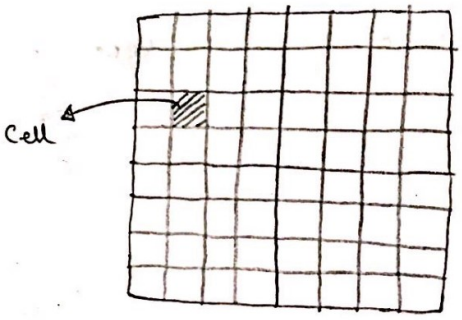


fig: 8×8 bits memory array

or, 1 byte × 1 byte memory array

or, 64 bit memory

or, 8 byte memory

Row × Column ⟶ RC ⇒ 8×8, 16×6, 8×4

- 1 Kb = 2^{10} bits
- 1 KB = $1 \times 2^{10} \times 2^3$ = 2^{13} bits

b → bit
B → byte

- 1 TB = $1 \times 2^{40} \times 2^3$ = 2^{43} bits
- 500 GB = $2^9 \times 2^{30} \times 2^3$ = 2^{42} bits

Dec		Bin.
10^3	K	2^{10}
10^6	M	2^{20}
10^9	G	2^{30}
10^{12}	T	2^{40}

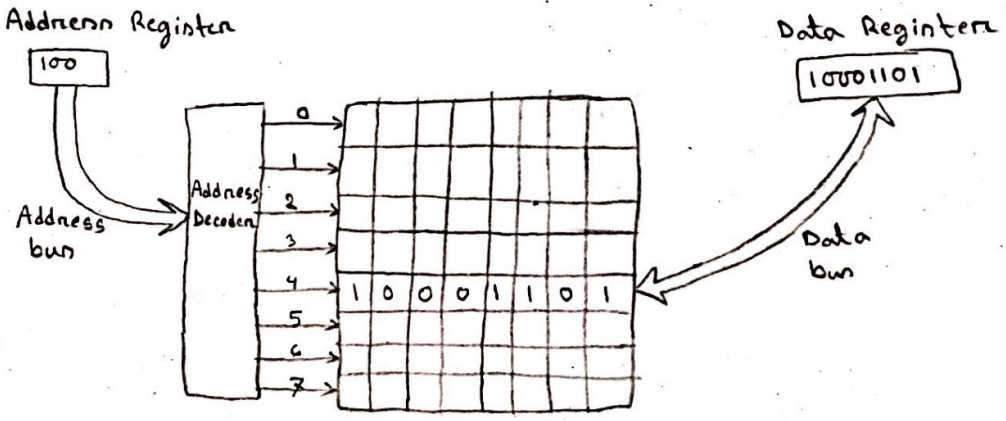
Data bus:

Data goes into memories during a write operation and comes out from memories during a read operation on a set of lines, is known as data bus.

→ Data bus is bidirectional

Address bus:

For a read or write operation an address is selected by placing a binary code representing the desired address on a set of lines is known as address bus.



Write operation:

1) Address code "100" is placed on the address bus & address "4" is selected.

2) Data byte "10001101" is placed on the data bus.

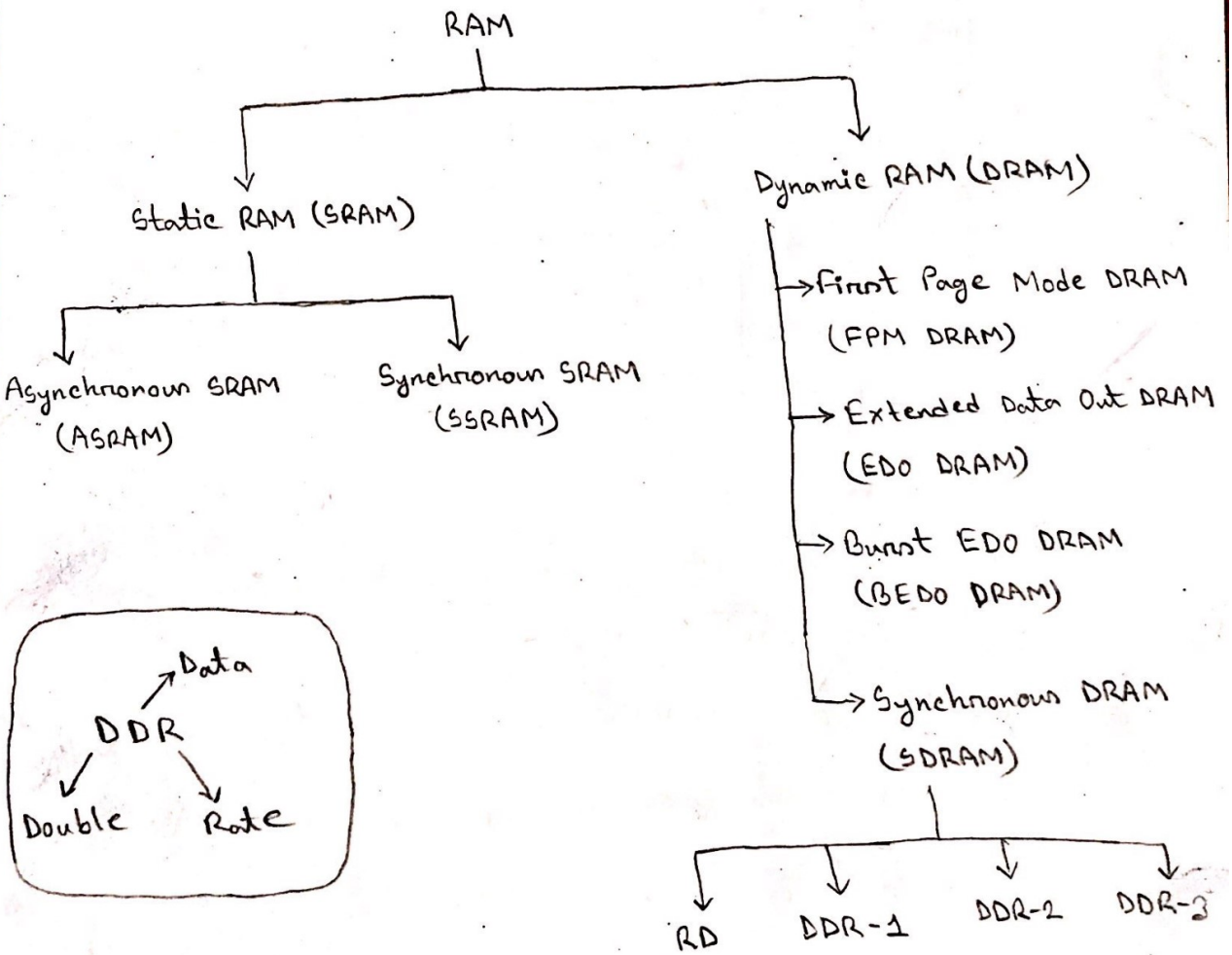
3) Write command causes the data byte to be stored in row "4" (by replacing previous data).

Read operation :

1) Address code "100" is placed on the address bus & address "4" is selected.
2) Read command is applied.
3) The content of address "4" is placed on the data bus and shifted into data register.

RAM (Random Access Memory)

Classification of RAM :



Difference bet^n SRAM & DRAM

adv. for SRAM → SRAM consumes less power than DRAM

→ SRAM uses flip-flops to store data whereas DRAM uses capacitors

adv. for SRAM → Data can be read much faster from SRAM than from DRAM

adv. for DRAM → DRAM can store much more data than SRAM for a given physical size & cost.

RAM Vs ROM

RAM

→ All address are accessible in an equal amount of time and can be selected in any order for a read/write operation

→ All RAMs have both read/write capacity.

→ RAM loses data when power is off → volatile memory

ROM (Read only Memory)

→ Data are stored permanently or semi-permanently (usually during manufacturing)

→ Data can only be read from a ROM

→ ROMs retain stored data even if power is turned off [Non-volatile memory]

Floyd Book
Ch-11 : Data Storage

Cache Memory

- Cache memory is relatively small, high speed memory that stores the most recently used data or instruction from the larger but slower main (primary) memory.

- Cache memory uses SRAM technology
  - L_1 cache memory
  - L_2 cache memory

⊛ **L_1 cache:** The first level cache is usually integrated in the microprocessor chip and has a very limited storage capacity known as primary cache or L_1 cache.

⊛ **L_2 Cache:** The second level cache is a seperate memory chip external to the microprocessor and has larger capacity but slower compared to L_1 cache, known as secondary cache or L_2 cache.

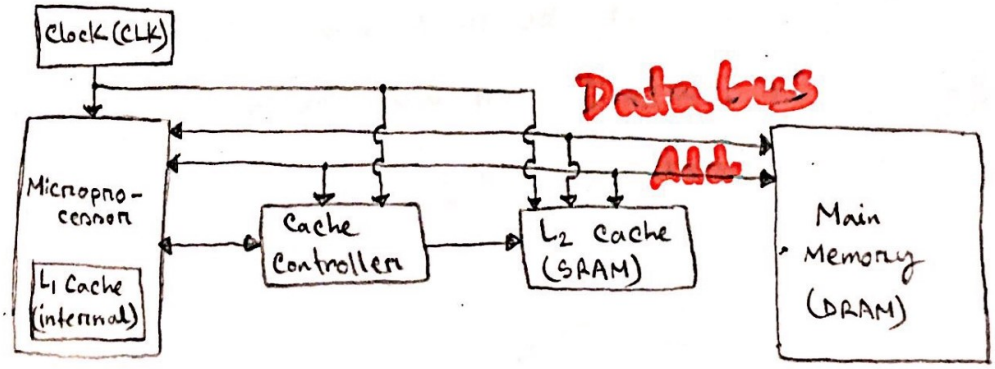


Fig: Block diagram of L_1 & L_2 cache memory in a computer system.

DRAM Cell :

Why refreshing is required in DRAM cell ?

Ans: DRAMs are based on capacitor charge storage for each bit in the memory array. This charge degraded (leaks off) with time and temperature, so each bit must be periodically refreshed (recharged) to maintain the correct bit state. Typically, a DRAM must be refreshed every 8 ms to 16 ms, although for some devices the refresh period can exceed 100 ms.

SRAM 6T operation (Read & Write)

→ From lab manual