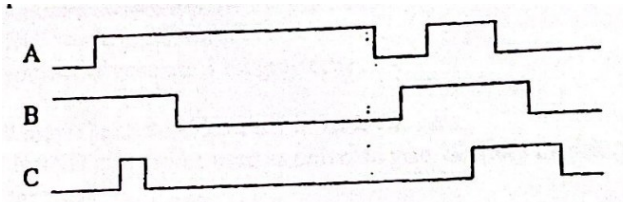
Combination Logic

1. What are the advantages of encoding a decimal number in BCD as compared to straight binary? What is its disadvantage?
2. What range of decimal values can be represented by a four-digit octal number?
3. A typical PC as a 20-bit address code for its memory locations-
   - How many Hex digits are needed to represent a memory address?
   - What is the range of addresses?
   - What is the total number of memory locations?
4. Perform the subtractions $(01001)_2-(11010)_2$ and $(10010)_2-(10011)_2$ using 2's complement.
5. Draw the logic diagram and truth table of OR, NOR and XOR gate using NAND gate only.
6. Simplify the following Boolean expression
   - $X=ABC+A'BC+AC+AC'$
   - $X=A'B(D'+CD)+AB+A'BCD$
7. Which coding technique is good for error detection? Give example.
8. Convert $(10110)_2=(?)_{gray}$ **
9. Minimize the following function: $f(a,b,c,d)=\sum_a(1,3,4,7,11)+\sum_d(5,12,13,14,15)$
10. Define prime implicant with example.
11. Define the following terms:
    - Fan out
    - Noise margin
12. Draw and explain the circuit operation of 2 digit TTL NAND gate.
13. Design a two input CMOS NAND gate with necessary diagram and truth table.
14. Perform subtraction using 2's complement method $85_{10}-47_{10}$
15. Convert $(541.203)_6$ to base 5, base 6, base 8, base 10 and base 16.*
16. Represent the decimal number 28 to excess-3 and BCD code.
17. Given the boolean function $K=AB+A'B'+B'C$ Then-
    - Implement it with AND, OR and NOT gates.
    - Implement it with only OR and NOT gates.
18. Show that the dual of the exclusive-OR is equal to its complement.
19. Simplify the following expression $z=A'BC'+ABC'+BC'D$
20. What are don't care terms? Explain with example.
21. What is parity bit? Design 3-bit odd parity generator and checker.
22. Implement a full adder using two half adder.
23. Design a logic circuit whose output is HIGH only when a majority of inputs A, B and C are LOW.
24. Simplify the following Boolean function using K-map and realize with basic gates:
    $F(A,B,C,D)=\sum_m(1,5,6,12,13,14)+\sum_d(2,4)$
25. Find $(45)_{10}-(83)_{12}$ using two's complement format with 8-bit numbers. Then convert your result back to decimal.
26. Add $(65)_{10}+(72)_{10}$ using 8-bit sign-magnitude format for the numbers. Convert your result to decimal. Is your answer correct? Why or why not?
27. Convert $(1000\,0110)_{BCD}$ to decimal, binary and octal.
28. Simplify $Z=A'C(A'BD)'+A'BC'D'+AB'$ using Boolean algebra.
29. State and prove De Morgan's theorems with the help of truth tables.

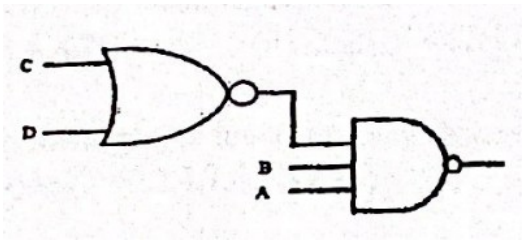
30. Design and explain a full adder in detail with circuit diagram and truth table.
31. Design a combinational logic circuit to compare two 2-bit binary numbers A and B and to generate the outputs A< B, A=B and A>B. Is there a way to derive the third output from the first two outputs?
32. Simplify the following Boolean expression using Quine-McCluskey technique
$f(A,B,C,D)=\Sigma_m(0,1,3,7,8,9,11,15)$
33. List out the advantages and disadvantages of Quine-McCluskey Method.
34. Do the following conversion:

- $(378)_{10}$ to 16 bit binary number.
- $(1010110.1100)_2=(?)_{10}$
- $(10101100)_2=(?)_8$
- $(743)_{16}=(?)_2$

35. Compare between BCD and Binary Code.
36. What is Gray code? Explain with examples, how do you convert binary to Gray and Gray to binary?
37. Subtract $(100111)_2$ from $(001100)_2$ using 2's complement method. Why do you need 2's complement method?
38. Apply the input waveforms of fig-1 to a NOR gate, and draw the output waveform. Then repeat the output waveform with C hold permanently LOW.



39. Determine the truth table for the circuit of fig-2.
x= AB (C+D)



40. Show that a two-input NAND gate can be constructed from two-input NOR gate.
Simplify the following $(A+B)'(A'+B')'$
41. What is DeMorgan's theorem? Explain with truth table.
42. Simplify the expression $x=A'B'C'+A'BC+ABC+AB'C'+AB'C$ using Boolean algebra.
43. Minimize the Boolean function $f(a,b,c,d)=\sum_M(1,4,6,8,10)$
44. Simplify the following expression using K-map
$f(A,B,C,D)=\sum_M(7,9,10,11,12,13,14,15)$
45. Design the circuit corresponding to the truth table shown in Table-1.

A	B	C	X
0	0	0.	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1

1	0	1	0
1	1	0	0
1	1	1	1

46. Do the following conversions:
- $(10101011.1101)_2=(?)_{10}$
- $(3AE8F.2D)_{16}=(?)_8$
- $(80914.25)_{10}=(?)_8$
- $(20345.125)_{10}=(?)_2$
- $(1011001110)_2=(?)_4$

47. Add $(110111)_2$ with $(100111)_2$ Subtract $(100110)_2$ from $(110011)_2$ using 2's complement method.
48. Represent $(-17)_{10}$ in sign magnitude, 1's complement and 2's complement representation.
49. Write the procedure to convert a binary code to gray code with example.
50. With the help of example explain excess-3 code.
51. Write the BCD code for $(9248)_{10}$
52. How can you easily generate 3 bit gray code.
53. Define and draw the truth table of a 3-input X-OR gate.
54. Show that NAND gate can be used as universal gate. Simplify the following using De-Morgan's theorem $(A+B')'(A'+B)'$
55. Simplify the following Boolean expressions to a minimum number of literals:
- $ABC+A'B+ABC'+AC$
- $A'B(D'+CD)+B(A+A'CD)$

56. Simplify the following logic function using Quine-McCluskey technique
$f(A,B,C,D)=\sum_M(0,1,3,7,8,9,11,15)$
57. A combinational circuit produces the binary sum of two 2-bit numbers, $x_¿$ and $y_¿$. The outputs are C, S_1, and S_0 . Provide a truth table of the combinational circuit, deduce the logic function and implement with logic gates. Also, design a circuit for the given problem using two full-adders block.
58. Construct a BCD-to-excess-3-code converter with a 4-bit adder. Remember that the excess-3 code digit is obtained by adding three to the corresponding BCD digit. What must be done to change the circuit to an excess-3-to-BCD-code converter?
59. Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.*
60. Design a code converter that converts a decimal digit from "8 4-2-1" code to BCD ("8 4 2 1") code.
61. Design a combinational circuit with three inputs, x, y, and z, and four outputs, A, B, C and D. When the binary input is 0, 1, 3, or 5, 7 the binary output is double of the input. When the binary input is 2, 4, or 6, the binary output is half of the input.
62. Minimize the function with Quine-McCluskey method:
$F(A,B,C)=\sum_M(0,1,2,5,6,7)$
63. Simplify the following Boolean function using K-map method
$F(A,B,C.D)=\sum_M(0,1,31,8\,14,14)+\sum_D(2,5,9,11)$ .Implement the minimized function
64. Represent $(-469)_{10}$ to sign-magnitude, 1’s complement and 2’s complement form.

65. Convert the following expressions to sum-of-product (SOP) forms:
- $BC(C'D'+CE)$
- $B+C[BD+(C+D')E]$

66. Use a Karnaugh map to reduce each expression to a minimum SOP form:
- $A'B'C'D'+A'B'C'D+ABCD+ABCD'$
- $A'B(C'D'+C'D)+AB(C'D'+C'D)+AB'C'D$

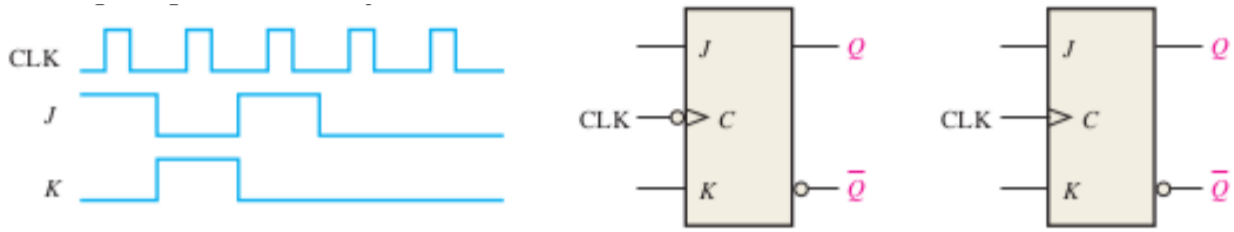
67. Use The Quine-McCluskey Method to reduce each expression to a minimum SOP form:
- $X=ABC+A'B'C+ABC'+AB'C+A'BC$
- $X=A'B'C'D'+A'B'C'D+A'BC'D+ABC'D'+AB'CD'+A'BCD'+AB'C'D$

68. Develop the logic and implement the circuit necessary to meet the following requirements:
A battery-powered lamp in a room is to be operated from two switches, one at the back door and one at the front door. The lamp is to be on if the front switch is on and the back switch is off, or if the front switch is off and the back switch is on. The lamp is to be off if both switches are off or if both switches are on. Let a HIGH output represent the on condition and a LOW output represent the off condition.
69. Design and discuss a 3 bit adder/subtractor circuit.
70. Design a combinational circuit with inputs A, B, C, D and output w, x, y, z. Assume that the inputs A, B, C, D represent a 4-bit signed number. The output is also a signed number, which is the 2's complement of the input.

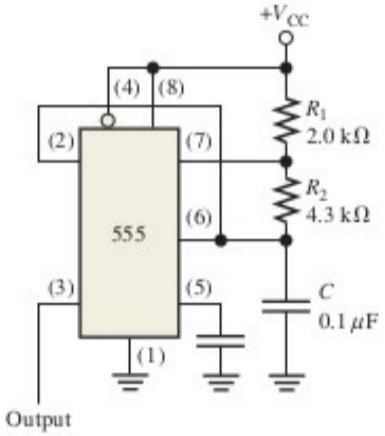
Sequential Circuit

1. Differences between Asynchronous and Synchronous system.
2. Operation of a positive-edge triggered JK flip-flop by timing diagram.**
3. SR-latch to D-latch conversion.
4. Operation of a JK flip-flop by timing diagram.**
5. Limitations of JK flip-flop.
6. Differences of Operation of a D latch and an edge triggered D flip-flop.**
7. Operation of 8-bit DAC using op-amp summing amplifier with binary weighted registers.
8. Design R-2R ladder 4-bit DAC with basic circuit diagram and V_{out} expression.***
9. Advantage of R/2R ladder DAC over weighted registers DAC.**
10. Operation with flow chart, block diagram of a successive approximation ADC.****
11. Block diagram of a 555 timer and explanation of its each pin.**
12. Operation and Design of an Astable multi-vibrator using 555 timer.***
13. Operation and circuit diagram of the edge triggered and clocked SR flip-flop with timing diagram.**
14. Operation and circuit diagrams of D flip-flop by timing diagram.***
15. Operation and Design NAND gate using Basic DTL gates.**
16. Characteristics of TTL gates.
17. Operation of open collector TTL gates.
18. Operation and design of ECL to implement OR and NOR gate.
19. Suitability of ECL.
20. Definition of Transducer, ADC, DAC.
21. If $V_{REF}=5V$ for the 4-bit DAC then find the resolution and full-scale output of the converter.

22. If 8-bit DAC has an output of $3.92\,mA$ for input 01100010. then find the resolution and full-scale output of the converter.**
23. Definition of Timer.
24. Applications of Timer.
25. Operation and Design of an mono-stable multi-vibrator using 555 timer.***
26. Definition of latch and flip-flop.
27. Operation of master-slave SR and JK flip-flop using logic and timing diagram.***
28. Advantages and disadvantages of TTL.
29. Design a NOT gate using MOSFET.
30. Resolution or step size of a DAC.**
31. Logic diagram of a clocked RS flip-flop with four NAND gates.
32. Advantages of a master-slave JK flip-flop?
33. Limitations of SR flip-flop.
34. Definition of setup time, propagation delay and hold time for flip-flop using proper timing diagram.
35. Operation and circuit diagrams of T type flip-flop and by timing diagram.**
36. Operation and circuit design of TTL NAND.
37. Current sourcing and current sinking action?
38. Operation and circuit design of CMOS NOR gate circuit.**
39. A certain binary-weighted-input DAC has a binary input of 1101. If a HIGH = 3V and a LOW = 0V what is Vout?
40. Benefits of clocked flip-flop.
41. Applications of Latch.
42. Operation and internal functional diagram of a 555 timer.
43. Applications of 555 timer.
44. If Resolution or step size is 0.1 V, then what will be the output voltage for a digital input 0001.
45. Advantage of a SAC over digital ramp ADC.**
46. If 8-bit SAC has resolution of 20 mV, then find and illustrate its digital output with diagram for an analog input of 2.17 V.
47. Definition of BCL NOR/OR gate.
48. Definition of Shift register and 3 bit counter.
49. Definition of Digital Ramp ADC.
50. Two edge-triggered J-K flip-flops are shown in Figure. If the inputs are as shown, draw the Q output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET.



51. A 555 timer is configured to run as an astable multivibrator as shown in Figure. Determine its frequency.



52. Determine the values of the external resistors for a 555 timer used as an astable multivibrator with an output frequency of 10 kHz, if the external capacitor C is 0.004 mF and the duty cycle is to be approximately 80%.
53. A certain gate draws a dc supply current from a +5 V source of 2 mA in the LOW state and 3.5 mA in the HIGH state. What is the power dissipation in the LOW state? What is the power dissipation in the HIGH state? Assuming a 50% duty cycle, what is the average power dissipation?
54. Discuss the operation of TTL inverter, NAND and NOR gates with proper diagram.
55. Discuss the operation of CMOS inverter, NAND and NOR gates with proper diagram. What is the resolution in volts of a 10-bit DAC whose F.S. output is 5 V?
56. How many bits are required for a DAC so that its F.S. output is 10 mA and its resolution is less than 40 mA?
57. A micro-controller has an 8-bit output port that is to be used to drive a DAC. The DAC that is available has 10 input bits and has a full scale output of 10 V. The application requires a voltage that ranges between 0 and 10 V in steps of 50 mV or smaller. Which 8-bits of the 10-bit DAC will be connected to the output port?
58. You need a DAC that can span 12 V with a resolution of 20 mV or less. How many bits are needed?
59. A certain 8-bit successive-approximation converter has 2.55 V full scale. The conversion time for VA = 1 V is 80 ms. What will be the conversion time for VA = 1.5 V?
60. An eight-bit digital-ramp ADC with a 40-mV resolution uses a clock frequency of 2.5 MHz and a comparator with VT = 1 mV. Determine the following values.
(a) The digital output for V A = 6.000 V
(b) The digital output for 6.035 V
(c) The maximum and average conversion times for this ADC