

University Of Rajshahi

Lab Report

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Experiment Number: 1

Name of experiment: Design and implement of simple combinational logic circuit.

Objective:

- To learn about the operation of combinational logic circuit.

Tasks:

- To design a circuit to observe the output of a combinational logic circuit.
- To implement the designed circuit on the breadboard.

Theory: The output of a combinational logic circuit can be determined by the logical function of their current input state (0 or 1) at any given instant time. Combinational logic circuit are made of basic logic gates like NAND, NOR, NOT gate and others that are combined and connected together to produce more complicated circuit.

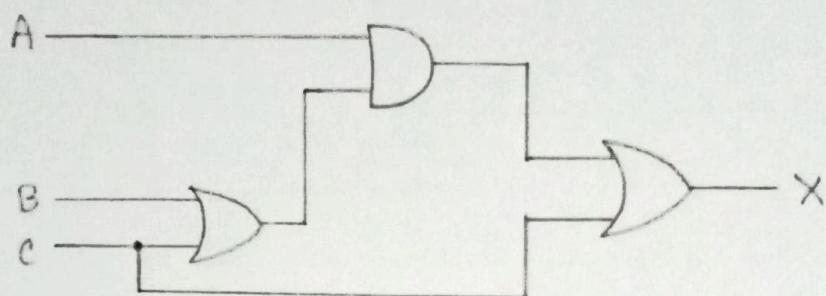
Circuit diagram:

Figure -1

The boolean expression for the circuit:

$$\begin{aligned}
 X &= A(B+C) + C \\
 &= AB + AC + C \\
 &= AB + C(A+1) \\
 &= AB + C \\
 &= Y
 \end{aligned}$$

So the new simplified circuit is:

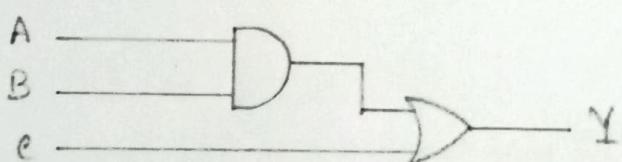


Figure -2

Truth table:

A	B	C	$A(B+C)$	X	Y
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

Requirements: ① Basic gate IC's and wires
 ② Breadboard
 ③ LED

Working Procedure:

- ① At first all the necessary IC's were taken.
- ② Then, Figure-1 and Figure-2 circuit was implemented.
- ③ After that the truth table was verified.

Result and discussion: We have used boolean algebra to simplify the circuit of Figure-1. Because it required more logic gates to implement. After simplification we got a new and simple logic circuit which required less logic gates than before. We implemented both the circuits and verified the circuits according to the inputs from the truth table. The output of the both circuits are same as we said in the truth table.

Precaution:

- ① All the IC's must be checked before the experiment.
- ② Connections should be made properly.
- ③ Supply voltage should be 5v.
- ④ Power supply should be turned off whenever there was a need to make a circuit change.

Experiment Number: 2

Name of experiment: Design and Implement of SR flip-flop.

Objective: To learn about the operation of SR flip-flop

Task:

- To design a circuit to observe the output of a SR flip-flop
- To implement the designed circuit on the breadboard.

Theory:

SR flip-flop is a edge triggered flip flop that means the flip-flop can change its current state only when a signal is applied to its clock input that makes a transmission from 0 to 1 or ~~1 to 0~~ which is also called positive edge triggered SR flip-flop. The set (S) and reset (R) inputs controls the state of the flip flop in the same way of a SR latch.

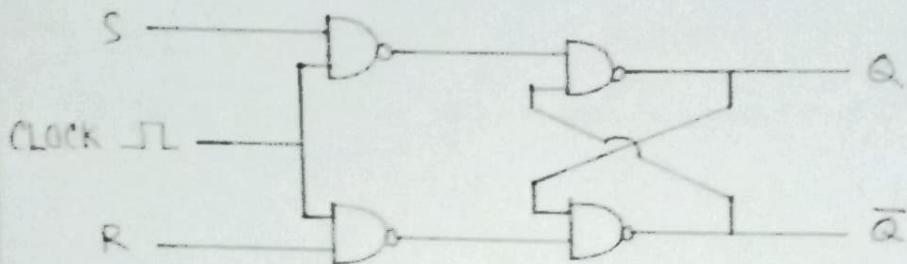
Circuit diagram:

Figure: SR flip flop

Truth table:

S	R	CLOCK	Q	\bar{Q}
X	X	0	Unchanged	
0	0	↑	Unchanged	
1	0	↑	1	0
0	1	↑	0	1
1	1	↑	Invalid	

Equipments: ① Breadboard and wires

② 7400 or 74LS00

③ LED's (2)

④ Resistor

Working procedure:

① First of all, the equipments were collected and then the circuit was implemented according to the diagram.

② SET (S) and RESET (R) inputs were connected to 5V supply voltage.

③ Two LED's were connected to the output of the flip flop to observe the output.

④ After that the truth table was verified.

Result and Discussion: Initially there was no clock pulse and the output remained same. When there was a clock pulse, the output changed their state according to SR control input. But when the S, R both inputs are HIGH (•1) the both outputs were HIGH. As we know that the outputs are complement to each other. So it is an invalid state.

Precaution:

- ① The NAND IC should be placed properly.
- ② Connections should be made properly.
- ③ Supply voltage should be 5V.
- ④ Power supply should be turned off whenever there is a need to make a circuit change.

Experiment Number : 3

Name of experiment: Design and implement of JK flip-flop.

Objective: To learn about the operation of JK flip-flop.

Tasks:

- To design a circuit to observe the output of JK flip-flop.
- To implement the designed circuit on the breadboard.

Theory: JK flip flop is an edge triggered flip flop which is triggered either by the positive going edge or the negative going edge of the clock signal. The J and K inputs control the state of the flip-flop just as SR flip-flop. Except for one major condition which is when $J=K=1$ it doesn't provide an invalid output like SR flip flop. For this condition the JK flip flop will always go to its opposite state upon the ~~a~~ POS of the clock signal. This is called toggle mode of the operation.

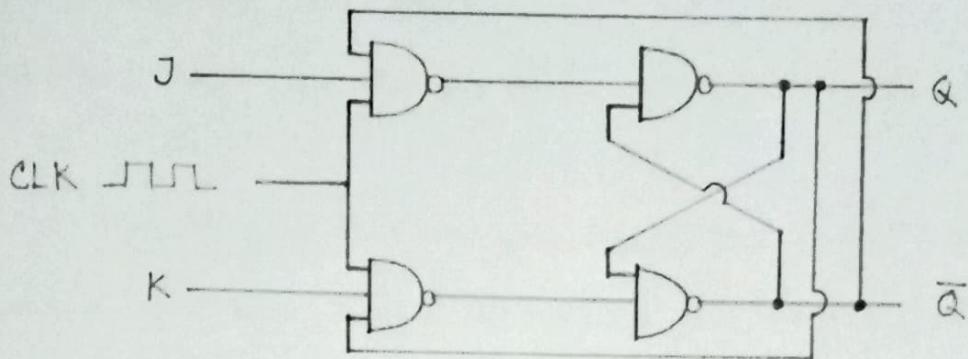
Circuit diagram:

Figure: JK flip flop

Truth table:

J	K	CLK	Q	\bar{Q}
x	x	0	Unchanged	
0	0	\uparrow	Unchanged	
1	0	\uparrow	1	0
0	1	\uparrow	0	1
1	1	\uparrow	Toggle	

Equipments: ① Breadboard and wires

② 7410 or 74LS10 and 7400 or 74LS00

③ LED's

④ Resistor

Working Procedure:

- ① At first all the necessary equipments were taken and then the circuit was implemented according to the diagram.
- ② J and K inputs were connected to 5V supply source.

- ③ The LED's were connected to the output of the flip-flop to observe the output.
- ④ After that the truth table was verified.

Result and Discussion: Initially there was no clock pulse and the output remained the same. When the clock pulse is applied, output was changed according to the input. When the J and K inputs are HIGH (1), the output starts changing its state which means the output starts toggling.

Precaution:

- ① All IC's must be checked before starting the experiment.
- ② Connections should be made properly.
- ③ Supply voltage should be 5V.
- ④ Power supply should be turned off whenever there is a need to make a circuit change.

Experiment Number: 4

Name of experiment: Design and implement of T flip-flop.

Objective: To learn about the operation of T flipflop.

Tasks:

- To design a circuit to observe the output of T flip-flop.
- To implement the designed circuit on the breadboard.

Theory: T flip flop is a single input version of JK flip flop in which the inputs J and K are connected together and is provided as a single input labelled as T. When there is no clock signal the flip-flop is disabled and previous output is maintained at output. When the clock is present and $T=0$, the output doesn't change its state. When $T=1$ and $CLOCK=1$ it causes the condition of $J=K=1$ and therefore the output state starts toggling.

Circuit diagram:

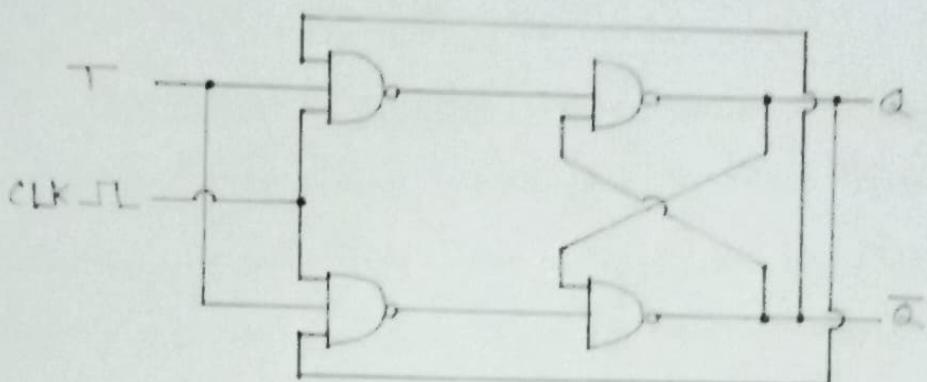


Figure: T flip-flop

Truth table:

T	CLK	Q	\bar{Q}
X	0	Unchanged	
0	↑	Unchanged	
1	↑	Toggle	

- Equipments:
- ① Breadboard and wires
 - ② 7410 or 74LS10 and 7400 or 74LS00
 - ③ LED's
 - ④ Resistor

Working Procedure:

- ① At first all the necessary equipments were taken and then the circuit was implemented according to the diagram.
- ② T input was connected to 5V supply voltage source.
- ③ The LED was connected to the output of the flip-flop to observe the output.

(4) After that the truth table was verified.

Result and Discussion: When there was no clock pulse, the output remained unchanged. & When there was a clock pulse but $T=0$, the output state remained the same. When $T=1$ (i.e. J and K both inputs are HIGH) it started to toggle the output. This toggle continues until the clock pulse stop.

Precaution:

- ① All the IC's must be checked before starting the experiment.
- ② Connections should be made properly.
- ③ Supply voltage should be 5V.
- ④ Power should be turned off whenever there was a need to make a circuit change.

Experiment Number: 5

Name of experiment: Design and implement an astable multivibrator using 555 timers.

Objective:

- To learn to use the oscilloscope for troubleshooting digital circuits.
-

Tasks:

- To design a circuit using 555 timer to study astable multivibrator.
- To implement the designed circuit on the breadboard.
- To observe the output signal.

Theory: Astable multivibrator operates as a free running oscillator. Its output is a repetitive rectangular waveform that switches between two logic levels. The 555 timer is made of two voltage comparators and a SR latch. The voltage comparators are devices that produce a HIGH output when the voltage on the + input is greater than the voltage of the - input. The external capacitor charges up until its voltage exceeds $\frac{2}{3} V_{cc}$ as determined

by the upper voltage comparator. When this comparator output goes HIGH, it resets the output latch, causing the output pin (3) to go LOW. At the same time \bar{Q} goes HIGH closing the discharge switch and causing the capacitor to begin to discharge until the capacitor voltage drops below $\frac{1}{3} V_{CC}$ as determined by the lower voltage comparator. When this comparator output goes high, it sets the SR latch causing the output pin (3) to go to HIGH, opening the discharge switch and allowing the capacitor to start charging again as the cycle repeats.

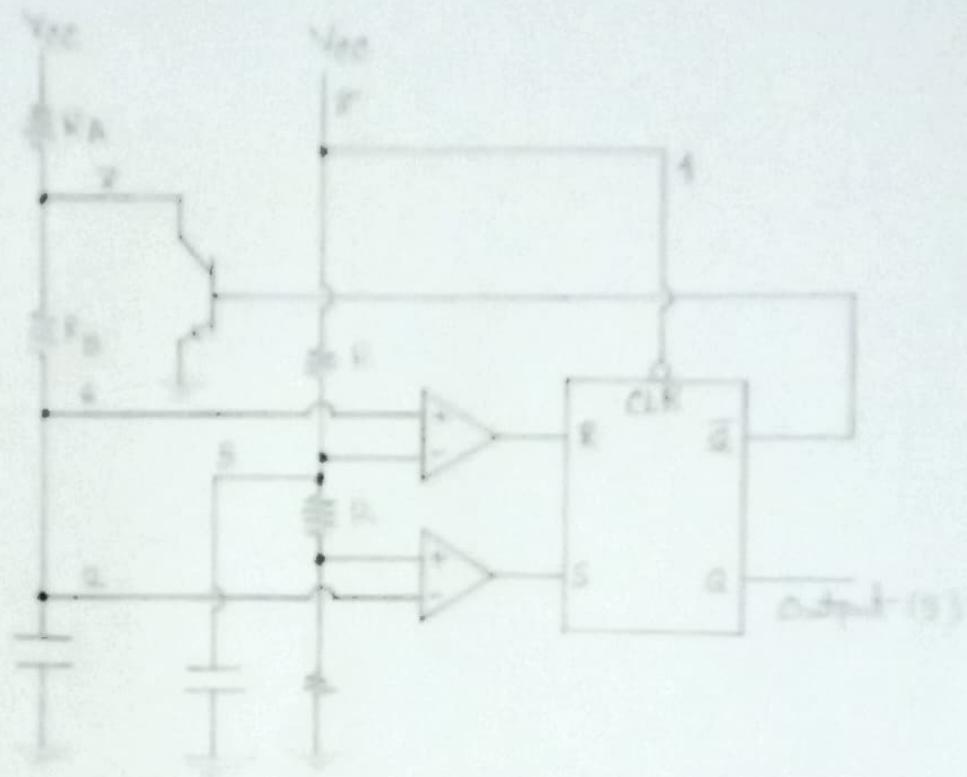
Circuit diagram:

Figure: Variable multivibrator using 555 timer

Equipment:

- ① Oscilloscope
- ② Breadboard and wires
- ③ 555 timer
- ④ Resistors
- ⑤ Capacitors

Working Procedure:

- ① At first all the necessary equipments were taken and then the circuit was implemented according to the diagram.
- ② The output pin was connected to the oscilloscope.

③ After that the output was observed from the oscilloscope.

Observation:

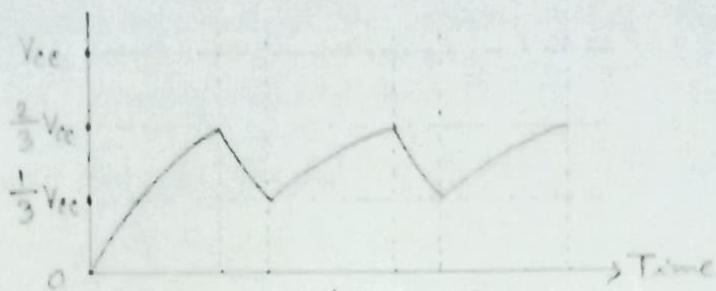


Figure : Analog Output

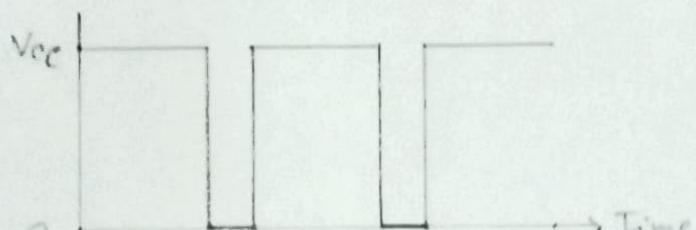


Figure : Digital Output

Result and discussion: When the power supply switch was closed the output was HIGH at the oscilloscope. But after some time the output goes LOW. Again after certain period of time the output goes HIGH. This continued until the power is on.

Hence the both HIGH and LOW states are unstable, it's a astable multivibrator. Here, the HIGH time is greater than the low time. This is due to resistors. If we apply $R_B \gg R_A$ the duty cycle will be closed to 50% (i.e. $t_L \approx t_H$).

Precaution:

- ① 555 timer should be placed properly on the breadboard.
- ② Circuit should be implemented carefully.
- ③ Connections should be made properly.
- ④ Power supply should be 5V.
- ⑤ Power supply should be turned off whenever there was a need to make a circuit change.

Experiment Number: 6

Name of experiment: Design and implement of monostable multivibrator using 555 timer.

Objective:

- To learn to use the oscilloscope for troubleshooting digital circuits.

Tasks:

- To design a circuit using 555 timer to study monostable multivibrator.
- To implement the designed circuit on the breadboard.
- To observe the output signal.

Theory: The monostable multivibrator is also called "one shot" pulse generator. The sequence of events starts when a negative going trigger pulse is applied to the trigger comparator. When this trigger comparator senses the short negative going trigger pulse to be just below the reference voltage ($\frac{1}{3} V_{cc}$) the device triggers and the output goes HIGH. The discharge transistor is turned off and the capacitor ~~the~~ that is externally connected to its collector will start charging to the maximum value through the resistor R.

The HIGH output pulse ends when the charge of the capacitor reaches $\frac{2}{3} V_{cc}$. The internal connection of the monostable multivibrator is given below.

Circuit diagram:

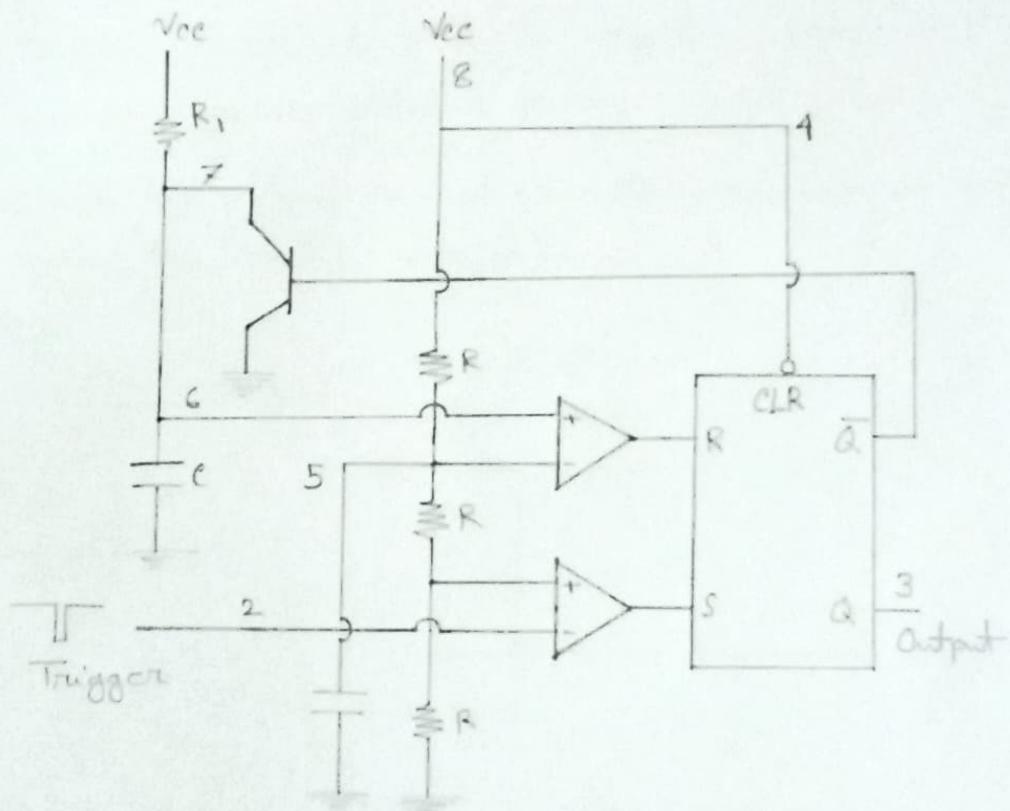


Figure: Monostable multivibrator using 555 timer

Equipments: ① Oscilloscope

② Breadboard and wires

③ 555 timer

④ Resistors

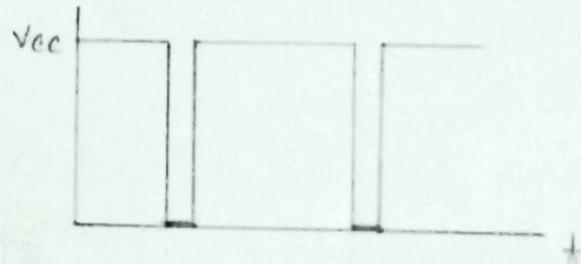
⑤ Capacitors

Working Procedure:

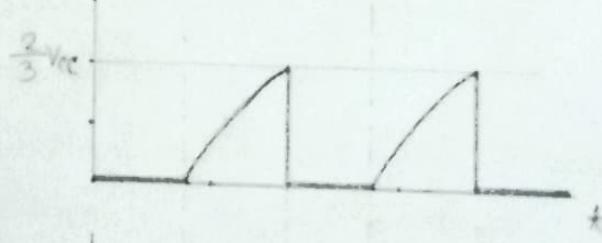
- ① At first all the necessary equipments were taken and the the circuit was implemented according to the diagram.
- ② Trigger pin (2) was connected to a negative pulse trigger switch to provide negative pulse and output pin (3) was connected to the oscilloscope .
- ③ Then the output signal was observed several times when the switch was pressed.

Observation:

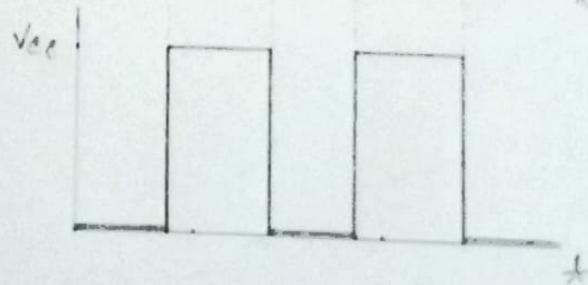
Trigger input :



Analog input :



Digital input :



Result and discussion: Initially the output was LOW (stable state). When the trigger pulse switch was pressed, the output goes HIGH (unstable state). After a certain amount of time the output returned to LOW. This LOW state continued until next trigger pulse occurred. This observation indicates that the circuit has one stable and one unstable state. The unstable state disappears after a certain amount of time. Hence it is a monostable multivibrator.

Precaution:

- ① 555 timer should be placed properly on the breadboard.
- ② Circuit should be implemented properly.
- ③ Connections should be made properly.
- ④ Power supply should be 5V.
- ⑤ Power supply should be turned off whenever there was a need to make a circuit change.