Name of the experiment: To design and implement SR flip-flop.

Objective: To learn about the operation of SR flip-flop.

Task:

(i). To design a circuit to observe the output of a SR flip flop.

(ii) To implement the design circuit on the breadboard.

(iii) To observe the output.

Theory: SR flip-flop is an edge triggered flip-flop. It is triggered by the positive going edge of the clock signal. This means that the FF can change state only when a signal applied to its clock input makes a transition from 0 to 1. The S and R input control the state of the FF in the same manner of a SR Latch. The figure of a SR flip-flop is given at the next page.

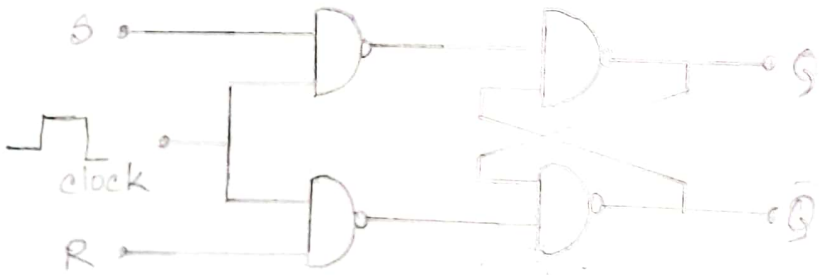

Fig: SR flip-flop

Equipment:

(i) Breadboard

(ii) Wires

(iii) IC 7400 or 741500

Working procedure:

(i) At first all the necessary equipment had been taken and made a circuit according to the circuit diagram.

(ii) Two LED's were connected to the set and reset output to observe the output.

(iii) Set and reset inputs were connected to 5 V voltage supply through switch.

Truth Table:

S	R	clk	Q	$\bar{Q}$
0	0	0	No change	No change
0	0	↑	No change	No change
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	1*	1*

Result and Discussion: Initially there was no clock pulse and the output was remained same. when there was a clock pulse, output change their state according to SR control input. But when set and reset input both are HIGH, the both output were HIGH. As we know, outputs are complement to each other. It's are invalid state.

Precaution:

(i) The NAND IC was placed properly on the bread board.

(ii) Connections were made carefully.

(iii) Supply voltage was 5 V for the safety.

(iv) Power supply was turned off whenever there was a need to make a circuit change.

Name of Experiment: To design and implement JK flip-flop.

Objective: To learn about the operation of JK flip-flop.

Task:

(i) To design a circuit to observe the output of a JK flip-flop.
(ii) To implement the designed circuit on the bread board.
(iii) To observe the output.

Theory: JK flip-flop is triggered by the positive going edge of the clock signal. The J and K input control the state of the flip-flop in the same ways as the S and R inputs for the clocked SR flip-flop except for one major difference the J=K=1 condition does not result in an ambiguous output for this 1, 1 condition the FF will always go to its oposite state upon the POrT of the clock signal. This is called the toggle mode of operation. In this mode, if both J and K are left HIGH the FF will change state (toggle) for each POrT of the clock.

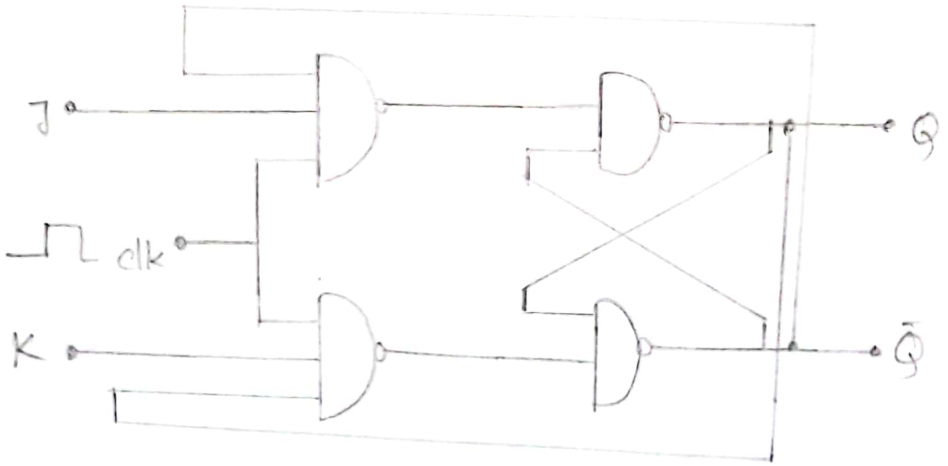

Fig: JK flip-flop

Equipment:

(i) Bread Board.
(ii) wires.
(iii) 7410 or 74LS10 and 7400 or 74LS00 IC.
(iv) LED's
(v) Resistor.

Working procedure:

(i) At first all necessary equipment had been taken and made a circuit according to the circuit drawn above.
(ii) 5 v supply was given to J and K through switch.
(iii) Reset and set output was connected to the LED's to observe the output.
(iv) The set and the reset was given fact to three input NAND gate as one of the input.

Truth table:

J	K	Clk	Q_n	Q_{n+1}
0	0	0	No change	No change
0	0	↑	No change	No change
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	0	1

Result and Discussion: Initially there was no clock pulse and output remained same, when the clock pulse is applied output was changed according to input when J and K are both were HIGH, the output was revesed from the previous state This shows the toggle mode of JK FF.

Precaution:

(i) The 74LS10 IC was placed properly on the bread board.

(ii) Connection were made carefully.

(iii) Power supply was turned off whenever there was a need to make a circuit change.

Name of experiment: To design and implement T flip-flop

Observe: To learn about the operation of T flip-flop.

Task:

(i) To design and a circuit for T flip flop
(ii) To implement the designed circuit on the broad board.
(iii) To observe the output.

Theory: T flip flop is a single input version of JK flip-flop. in which the input J and K are connected together and is provided as a single input as T. when the clock is absent the flip-flop is disabled as usual and previous output is maintained at output when the clock is present and T=0 even through flip-flop is enabled the output does not switch its state when T=1 during clock. it causes J=K=1 and as earlier discussed it will toggle to output state.

Equipments:

(i) Bread boards and wires.
(ii) 7410 or 74LS10 and 7400 or 74LS00 IC
(iii) LED's
(iv) Resistors.

Circuit diagram:

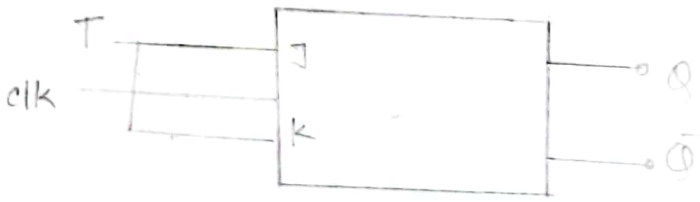

Fig - T flip-flop

Truth Table:

T	clk	Q	$\bar{Q}$
0	x	No change	No change
↑	0	No change	No change
↑	1	Toggle	Toggle.

Working procedure:-

(i) At first all the necessary equipment had been taken and a circuit was made for T flip-flop.

(ii) 5 v supply was connected to the T input through switch.

(iii) The set and reset output was connected to the LEDs and noted down all the results.

Result and Discussion:

When there was no clock pulse, output remined uncharged, when there was a clock but T=0, output still will remain same. When T=1 both J and k is High it drives the output to toggle. This toggle containes untill the clock pulse stop.

Precaution:

(i) The NAND IC was placed properly on the breadboard.

(ii) Connection were given carefully.

(iii) 5 v power supply was turned off whenever there was a need make a circuit change.

Name of the Experiment: To design and Implement D flip flop.

Objectives: To learn about the operation of D flip-flop.

Task:

(i) To design and circuit to observe the output of a D flip flop.
(ii) To implement the designed circuit on the bread board.
(iii) To observe the output.

Theory: The D flip flop is the most important flip flop from other clocked types. It ensures that at the same time both the inputs i.e. S and R are never equal to 1. The Delay flip-flop is designed using a gated SR flip-flop with an inverters connected between the inputs allowing for a single input D. This single data input which is labeled as "D" used in place of the set input and for the complementary Reset input the inverters is used. Thus, the level sensitive D type or D flip flop is constructed from a level sensitive SR flip-flop.

Circuit Diagram:

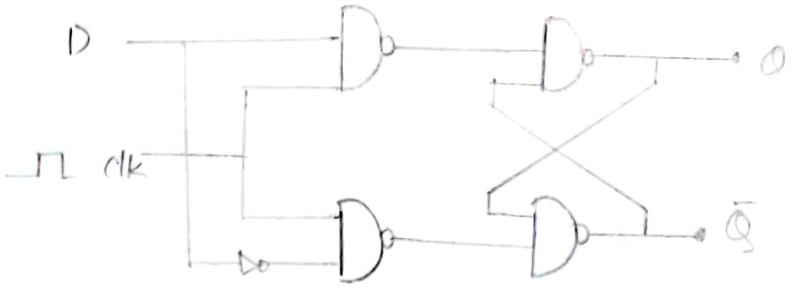

Fig : D-flip-flop

Truth Table:

clk	D	Q	$\bar{Q}$
↓ >> 0	x	NC	NC
↑ >> 1	0	0	1
↑ >> 1	1	1	0

Working procedure:

(i) At first all the necessary equipment had been taken and made a circuit according to the circuit drawn figure.

(ii) Two LED's were connected to the set and Reset output to observe the output.

(iii) Set and Reset inputs were connected to 5 v voltage supply through switch.

Result and Discussion: Initially there was no clock pulse and output was remained same when there was a clock pulse output change theire state according to D control input when D input was ta stayed low the output was remained the set state and when D input stayed high the output remain reset state.

Precaution:

(i). The NOT and NAND IC was placed properly on the broadboard.

(ii) Connection were made carefully.

(iii) Supply voltage 5 v fore safety.