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Lab

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Name of Experiment: DAC USING R-2R LADDER NETWORK.

Objective: To build and study DAC using R-2R ladder network.

Task:

1) To design a circuit to observe the of a DAC circuit.
11) To implement the designed circuit on the breadboard.
111) To observe the output.

Theory:

R-2R Configuration is a simple arrangement that consists of parallel and series resistors connected in the cascaded form to an operational amplifier. An operational amplifier can be used in inverting or non-inverting form depending on the polarity of output voltage that we want to get form DAC. R-2R Ladder resistors act as voltage dividers along with the entire network with the output voltage dependent on the input voltage

Apparatus:

i) Resisters
ii) LEDS
iii) 741 IC
iv) wires

Working procedure:

i) Calculating analog output voltage for various combinations from 0000 to 1111 of 4-bit R-2R ladder network.

ii) Connect the circuit as shown in the diagram

iii) Connect voltages corresponding to logic 1 and logic 0 to the input bit position of R-2R ladder for various combinations from 0000 to 1111.

iv) Read analog output voltage of R-2R ladder network for each combination using multimeter

v) Compare calculated and observed values of analog output voltage corresponding to binary input combination and find the error value.

vi) plot a graph of analog output voltage versus binary number.

Block diagram:

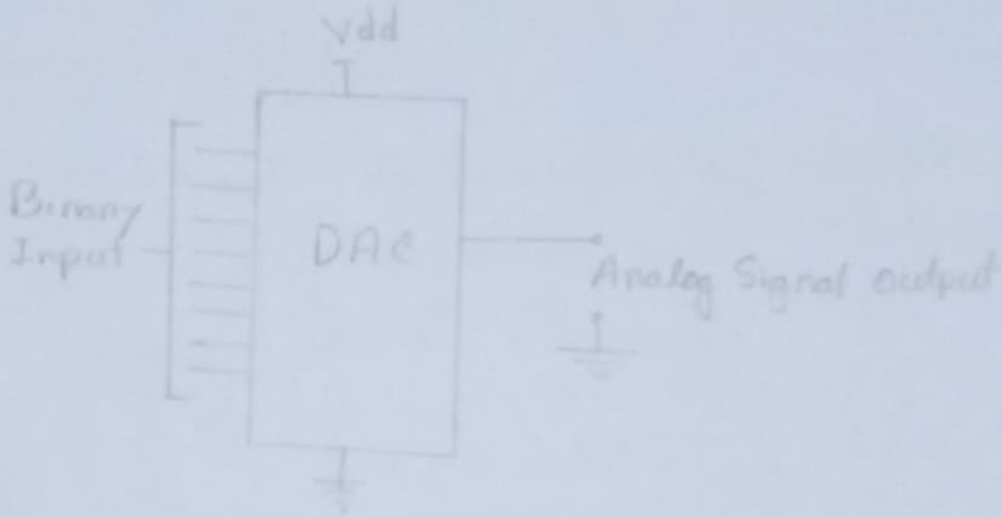

Fig: R-2R DAC

Circuit Diagram:

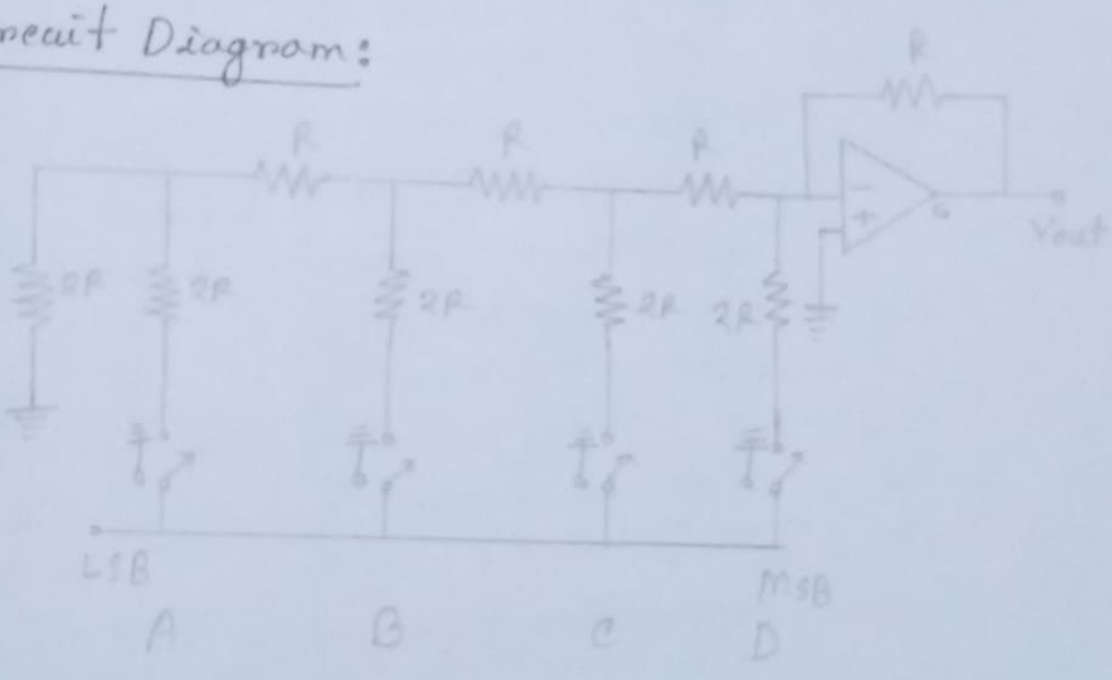

Fig: DAC circuit diagram using R-2R ladder

Note:

1. use $2R = 2\,k\Omega$ or any value and $R = 1\,k\Omega$ can be obtained by connecting two ~~2R~~ 2R resistors in parallel.

2. Connect series combination of 220Ω resistor an LED between input and ground to see input.

Experiment table:

No. of obs	Binary input				Analog output (Vout expression)		
	D	C	B	A	$(8\times V_D+4V_C+2V_B+V_A)/16$	Calculated	Measure
1	0	0	0	0	$(8\times0+0+0+0)/16$	0	0
2	0	0	0	1	$(0+0+0+3.20)/16$	0.2	0.175
3	0	0	1	0	$(0+0+2\times3.25+0)/16$	0.406	0.35
4	0	0	1	1	$(0+0+2\times3.25+3.20)/16$	0.606	0.60
5	0	1	0	0	$(0+4\times3+0+0)/16$	0.75	0.71
6	0	1	0	1	$(0+4\times3+0+3.20)/16$	0.95	0.90
7	0	1	1	0	$(0+4\times3+2\times3.25+0)/16$	1.156	1.10
8	0	1	1	1	$(0+4\times3+2\times3.25+3.20)/16$	1.356	1.30
9	1	0	0	0	$(8\times2.4+0+0+0)/16$	1.20	1.15
10	1	0	0	1	$(8\times2.4+0+0+3.20)/16$	1.40	1.35
11	1	0	1	0	$(8\times2.4+0+2\times3.25+0)/16$	1.606	1.61
12	1	0	1	1	$(8\times2.4+0+2\times3.25+3.20)/16$	1.806	1.78
13	1	1	0	0	$(8\times2.4+4\times3+0+0)/16$	1.95	1.93
14	1	1	0	1	$(8\times2.4+4\times3+0+3.20)/16$	2.25	2.12
15	1	1	1	0	$(8\times2.4+4\times3+2\times3.25+0)/16$	2.356	2.34
	1	1	1	1	$(8\times2.4+4\times3+2\times3.25+3.20)/16$	2.556	2.50

Calculation:

Analog output voltage is given by

$$V_{out} = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + \cdots + V_{n-1} 2^{n-1}}{2^n}$$

$$= \frac{V_A + 2V_B + 4V_C + 8V_D}{16}$$

when n is number of bits $= 4$.

V_A, V_B, V_C, V_D are Digital input voltage levels Corresponding to logic 1 and logic 0.

Result and discussion;

1) Observed analog output voltage matches with calculated analog output voltage.
2) The graph of analog voltage versus binary equivalent shows stepwise increase with step size equal to $\frac{V_R}{2^n}$ v i.e analog output voltage Corresponding to 0001.

Precaution:

i) Always connect ground first and then Connection vcc.
ii) The kit should be ~~be~~ off before changing the Connections
iii) Switch off the kit after the experiment,