

Q) Convert  $(934.685)_{10}$  to base 2, 8 and 16.

$$(934.685)_{10} = (934 + 0.685)_{10} = (?)_2$$

$$\begin{array}{r} 2 | 934 \\ \hline 2 | 467 \rightarrow 0 \\ \hline 2 | 233 \rightarrow 1 \\ \hline 2 | 116 \rightarrow 1 \\ \hline 2 | 58 \rightarrow 0 \\ \hline 2 | 29 \rightarrow 0 \\ \hline 2 | 14 \rightarrow 1 \\ \hline 2 | 7 \rightarrow 0 \\ \hline 2 | 3 \rightarrow 1 \\ \hline 2 | 2 \rightarrow 1 \\ \hline 0 \rightarrow 1 \end{array} \quad (\text{msb})$$

And,

$$\begin{aligned} 0.685 \times 2 &= 1.37 \rightarrow 1 \\ 0.37 \times 2 &= 0.74 \rightarrow 0 \\ 0.74 \times 2 &= 1.48 \rightarrow 1 \\ 0.48 \times 2 &= 0.96 \rightarrow 0 \\ 0.96 \times 2 &= 1.92 \rightarrow 1 \\ 0.92 \times 2 &= 1.84 \rightarrow 1 \\ &\vdots \\ (.685)_{10} &= (101011\dots)_2 \end{aligned}$$

$$\therefore (934)_{10} = (1110100110)_2$$

$$(934.685)_{10} = (1110100110 \cdot 101011\dots)_2$$

$$\textcircled{b} \quad \frac{(1110100110 \cdot 101011\dots)_2}{\begin{array}{r} \downarrow 1 \\ \downarrow 6 \end{array} \quad \begin{array}{r} \downarrow 4 \\ \downarrow 6 \end{array} \quad \begin{array}{r} \downarrow 5 \\ \downarrow 3 \end{array} \quad \dots} = (?)_8$$

$$= (1646.53\dots)_8$$

$$\text{Again, } \frac{(1110100110 \cdot 101011\dots)_2}{\begin{array}{r} \downarrow 3 \\ \downarrow A \end{array} \quad \begin{array}{r} \downarrow 6 \\ \downarrow \end{array} \quad \begin{array}{r} \downarrow A \\ \dots \end{array}} = (?)_{16}$$

$$= (3A6.A\dots)_{16}$$

$$(934.865)_{10} = (1110100110,101011)_2 =$$

$$(1646.53\ldots)_8 = (3A6.A\ldots)_{16}$$

(Ans)

—\*—

3) Represent  $(-469)_{10}$  to Sign-magnitude, 1's Complement and 2's Complement.

9

$$|-469| = 469$$

Here, 469 binary representation -

2	469	(LSB)
2	234 → 1	
2	117 → 0	
2	58 → 1	
2	29 → 0	
2	14 → 1	
3	7 → 0	
2	3 → 1	
2	1 → 1	
	0 → 1	(msb)

$$(469)_{10} = (111010101)_2$$

The base 2 number's actual length is 9  
 A signed binary bit length must be equal  
 to a power of 2, as of

$$2^1=2, 2^2=4, 2^3=8, 2^4=16 \dots$$

First bit (the leftmost) indicates the sign  
 $1 = \text{Negative}$  and  $0 = \text{Positive}$

Positive binary computer representation on  
 16 bits (2 bytes) if needed, add extra 0's  
 in front (to the left) of the base 2  
 number, up to the required length = 16;

$$(469)_{10} = (0000\ 0001\ 1101\ 0101)_2$$

get the negative number representation on  
 16 bits (2 bytes).

Signed binary one's complement,  
 replace all the bits on 0's with 1's and  
 all the bits set on 1's with 0's.  
 (reverse digit, flip the digit)

$$\neg(0000\ 0001\ 1101\ 0101)_2 = (1111\ 1110\ 0010\ 1010)_2$$

Signed binary two's complement add 1 to  
 the number calculated above.

$$\begin{array}{r}
 1111\ 1110\ 0010\ 1010 \\
 + 1 \\
 \hline
 1111\ 1110\ 0010\ 1011
 \end{array} = (-469)_{20}$$

9

Number (-469), a Signed integer, Converted from decimal system (base 10) a signed binary two's complement representation;

$$(-469)_{10} = (1111\ 1110\ 0010\ 1010)_2$$

(Ans)

+ -

3) Convert the following expression to sum-of-products (SOP).

a)  $BCE(C'D' + CE)$

$$= BCEC'D' + BCECE$$

$$= 0 + BCEE$$

$$= BCEE$$

$$\therefore C \cdot C' = 0$$

$$\therefore C \cdot C = C$$

(Ans)

b)  $B + C[B(D + (C + D')E)]$

$$= B + C [BD + CE + D'E]$$

$$= B + BCD + CCE + CD'E$$

$$= B + BCE + CE + CD'E$$

$$= B(1 + CD) + CE(1 + D')$$

$$= B + CE$$

$$\therefore 1 + C = 1$$

$$\therefore 1 + D' = 1$$

(Ans)

4) use a K-map to reduce each expression to a minimum SOP form:

$$\text{a) } A'B'C'D' + A'B'C'D + ABCD + ABCD' \\ = \Sigma(0, 1, 15, 14)$$

K-map for 4 bit

AB	CD			
	00	01	11	10
00	(1 1)			
01				
11		(1 1)		
10				

$$= \bar{A}\bar{B}\bar{C} + ABC$$

(Ans)

$$\text{b) } A'B(C'D' + C'D) + AB(C'D' + C'D) + ABC'D \\ = A'BC'D' + A'BC'D + ABC'D' + ABC'D \\ = \Sigma(4, 5, 12, 13, 9)$$

K-map

AB	CD			
	00	01	11	10
00				
01	(1 1)			
11	(1 1)			
10		(1)		

$$= BC' + AC'D$$

(Ans)

5) Use the Quine-McCluskey method to reduce each expression to a minimum SOP form:

$$\text{a) } x = ABC + A'B'C + ABC' + AB'C + A'B'C \\ = \sum(1, 3, 5, 6, 7)$$

minterms

No of 1's	Binary no	Check PI	Stage-I	Check PI	Stage-II
1 → 1	001	✓	1, 3 → 0-1	✓	1, 3, 5, 7 → --1
2 → 3	011	✓	1, 5 → -01	✓	1, 5, 3, 7 → --1
5	101	✓	6, 7 → 11-	⑥	
6	110	✓	5, 7 → 1-1	✓	
3 → 7	111	✓	3, 7 → -11	✓	

	1	3	5	6	7
$a(1, 3, 5, 7) \rightarrow --1$	✓	✓	✓		✓
$b(6, 7) \rightarrow \overline{11}$	✓			✓	✓
	✓	✓	✓		✓

$$= a + b$$

$$= C + AB$$

(Ans)

$$\begin{aligned}
 b) x &= A'B'C'D' + A'B'C'D + A'B'C'D + AB'C'D' + A'BC'D \\
 &\quad + A'BCD' + AB'CD \\
 &= \{0, 1, 5, 6, 9, 10, 12\}
 \end{aligned}$$

No of 1  $\rightarrow$  Minterms      Cheekeen PI      Stage-I

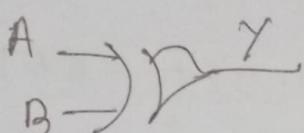
$0 \rightarrow 0 = 0000$	✓	$(0, 2) = 000-$ @
$1 \rightarrow 1 = 0001$	✓	$(1, 5) = 0-01$ @
$2 \rightarrow 5 = 0101$	✓	$(1, 9) = -001$ @
$6 = 0110$	④	
$9 = 1001$	✓	
$10 = 1010$	⑤	
$12 = 1100$	⑥	

	0	1	5	6	9	10	12
a $0, 1 = 000-$	✓	✓					
b $6, 5 = 0-01$		✓	✓				
c $1, 9 = -001$	✓				✓		
d $6 = 0110$				✓			
e $10 = 1010$						✓	
f $12 = 1100$	✓		✓	✓	✓	✓	✓

$$\begin{aligned}
 &= a + b + c + d + e + f \\
 &= A'B'C' + A'C'D + B'C'D + A'BCD' + AB'C'D + ABC'D' \\
 &\quad \text{(Ans)}
 \end{aligned}$$

6). It's a X-OR gate the output is high when only one of the inputs is high, when both the inputs are higher low the output remains low.

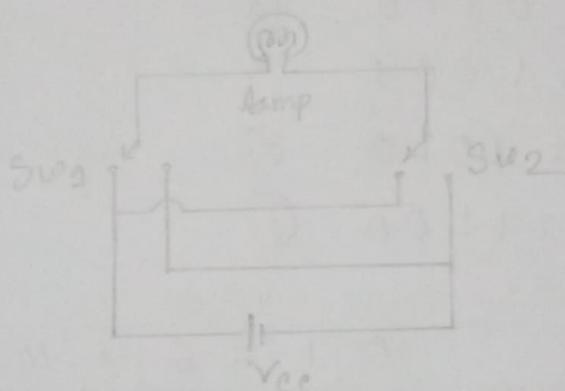
$$\begin{aligned} Y &= \bar{A}B + A\bar{B} \\ &\equiv A \oplus B \end{aligned}$$



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

High = 1

Low = 0



X-OR gate

-① -

7) Design 3 bit Adder circuit and discuss.

Full Adder: Full Adder is a combinational logic circuit. It is used for the purpose of adding two single bit numbers with a carry.

- i) The least significant bits are 0 and 1, giving a sum of 1 with no carry,
- ii) There is no carry in front a previous stage.
- iii) The next bits are 1 and 1 with no carry in, giving a sum of 0 and a carry of 1.
- iv) The most significant bits are both 1 with a carry in of 1.
- v) This gives a sum of 1 and a carry of 1.
- vi) This results of adding 110 to 111 is 1101.

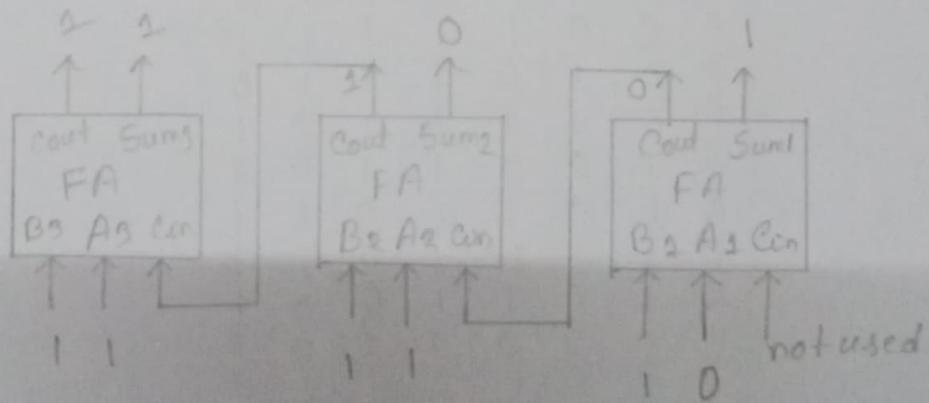


Fig.1: Block diagram of 3 bit Adder.

### 3 bit Subtractor:

A Full Subtractor is a combinational logic circuit which performs a subtraction between the two 1-bit binary numbers and it also considers the borrow of the previous minuend bit.

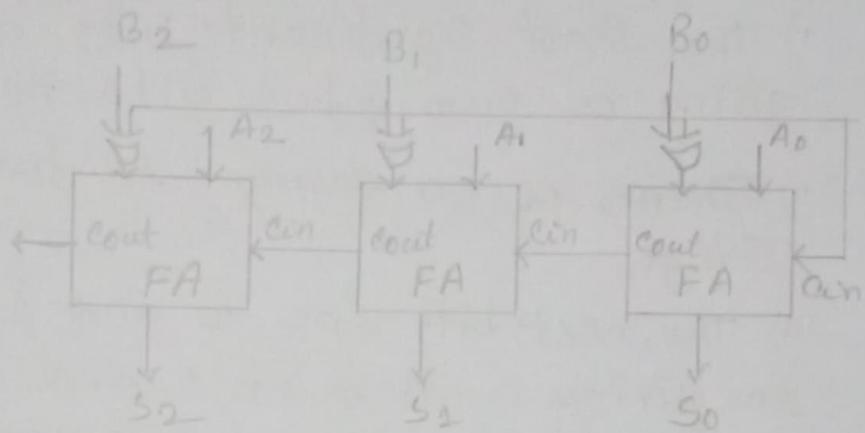


Fig: 3bit Adder subtractor

- 8) 2's complement input and output

Input				Output			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

Now, Simplified expression for w.

		CD	AB	00	01	11	10
		00		1	1	1	
		01		1	1	1	1
		11					
		10		1			

$$w = \bar{A}B + \bar{A}C + \bar{A}D + A\bar{B}\bar{C}\bar{D}$$

Simplified expression for x.

		CD	AB	00	01	11	10
		00		1	1	1	1
		01		1			
		11		1			
		10		1	1	1	

$$x = B\bar{C}\bar{D} + \bar{B}D + \bar{B}C$$

Simplified expression for y.

		CD	AB	00	01	11	10
		00		1		1	
		01		1		1	
		11		1		1	
		10		1		1	

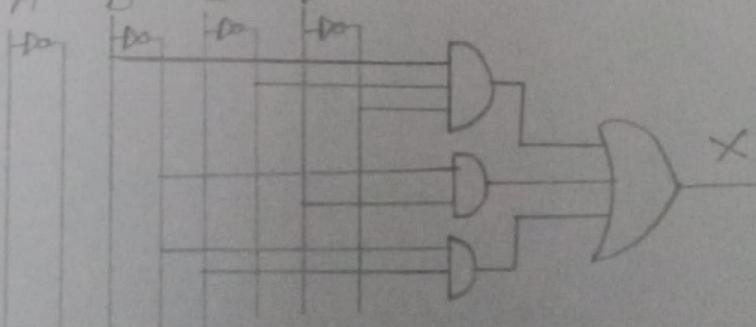
$$y = \bar{C}D + C\bar{D} \\ = C \oplus D$$

Simplified expression for z.

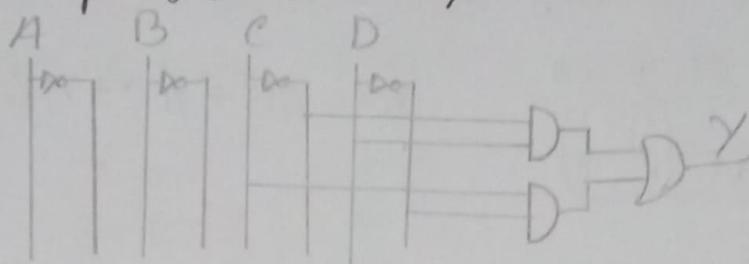
		CD	AB	00	01	11	10
		00		1	1		
		01		1	1		
		11		1	1		
		10		1	1		

$$z = D$$

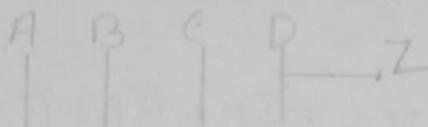
Logic circuit for x = B\bar{C}\bar{D} + \bar{B}D + \bar{B}C



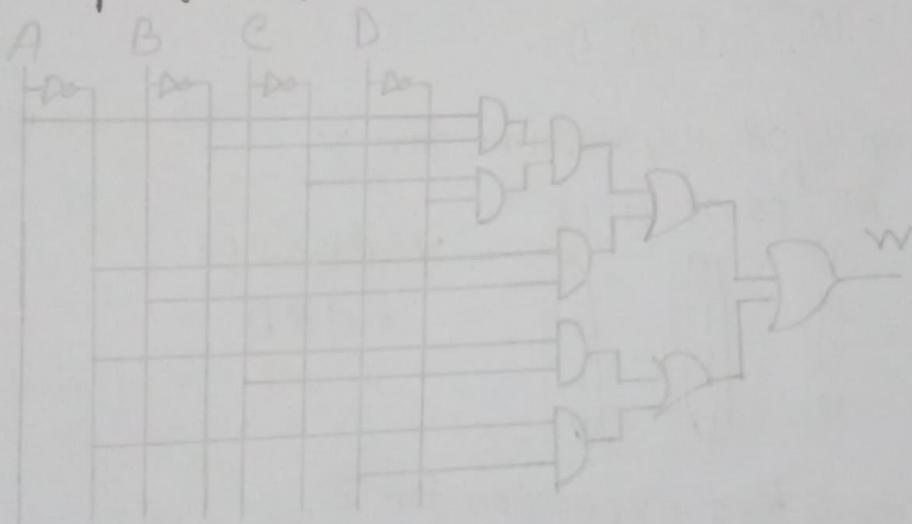
Simplified from  $y = \bar{C}D + C\bar{D}$



Simplified from  $z = D$



Simplified from  $w = A\bar{B}\bar{C}\bar{D} + \bar{A}B + \bar{A}C + \bar{A}D$



→ M →

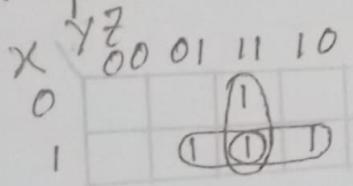
9) Truth table that defines the required relationship between inputs and outputs.

Inputs			Outputs		
X	Y	Z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

Input 0,1,2,3 } Output

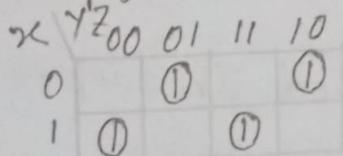
Input 4,5,6,7 } Output

K-map for A:



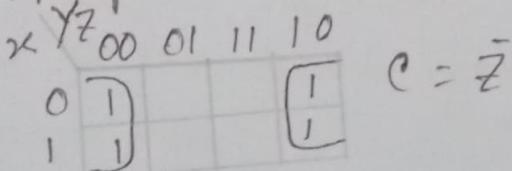
$$A = YZ + XZ + XY$$

K-map for B:



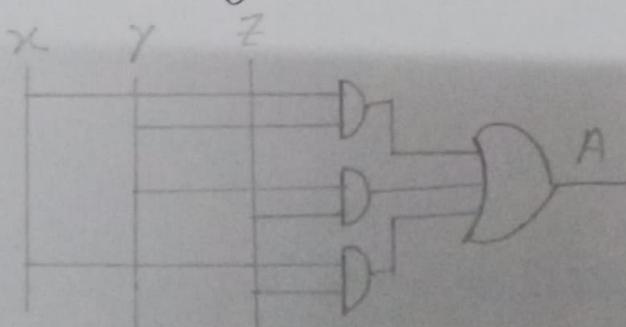
$$B = \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y}Z + XY\bar{Z} + \bar{X}YZ$$

K-map for C:

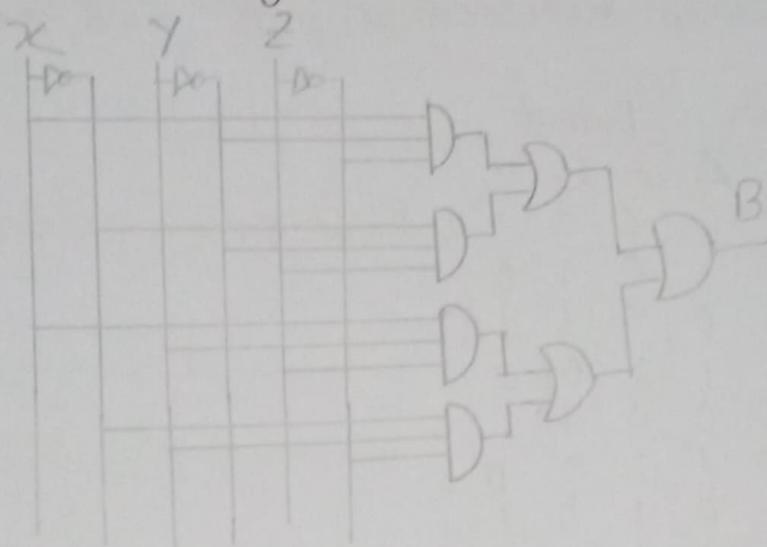


$$C = \bar{Z}$$

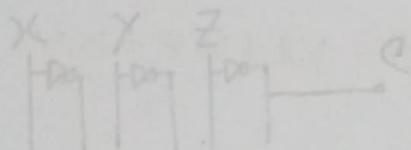
Circuit diagram for  $A = XY + YZ + XZ$



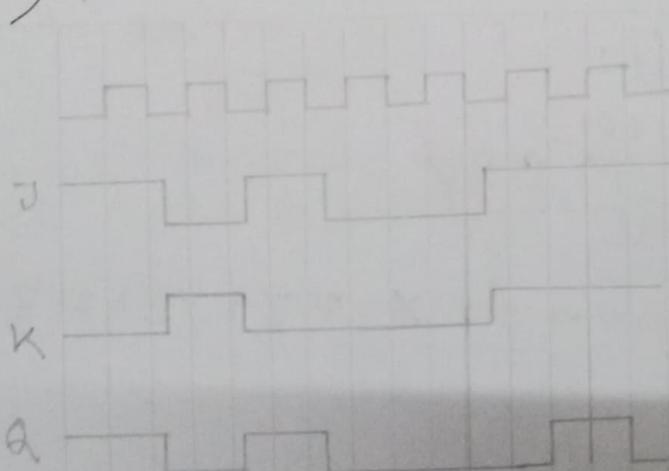
Circuit diagram for B:  $x\bar{y}\bar{z} + \bar{x}\bar{y}z + xy\bar{z} + \bar{x}yz$



Circuit diagram for C:



10) Positive edge triggered JK flip-flop:



J	K	Q	$\bar{Q}$	
0	0	memory		
0	1	0	1	reset
1	0	1	0	set
1	1			Toggle

Fig: positive edge triggered diagram

Negative edge triggered JK flip-flop

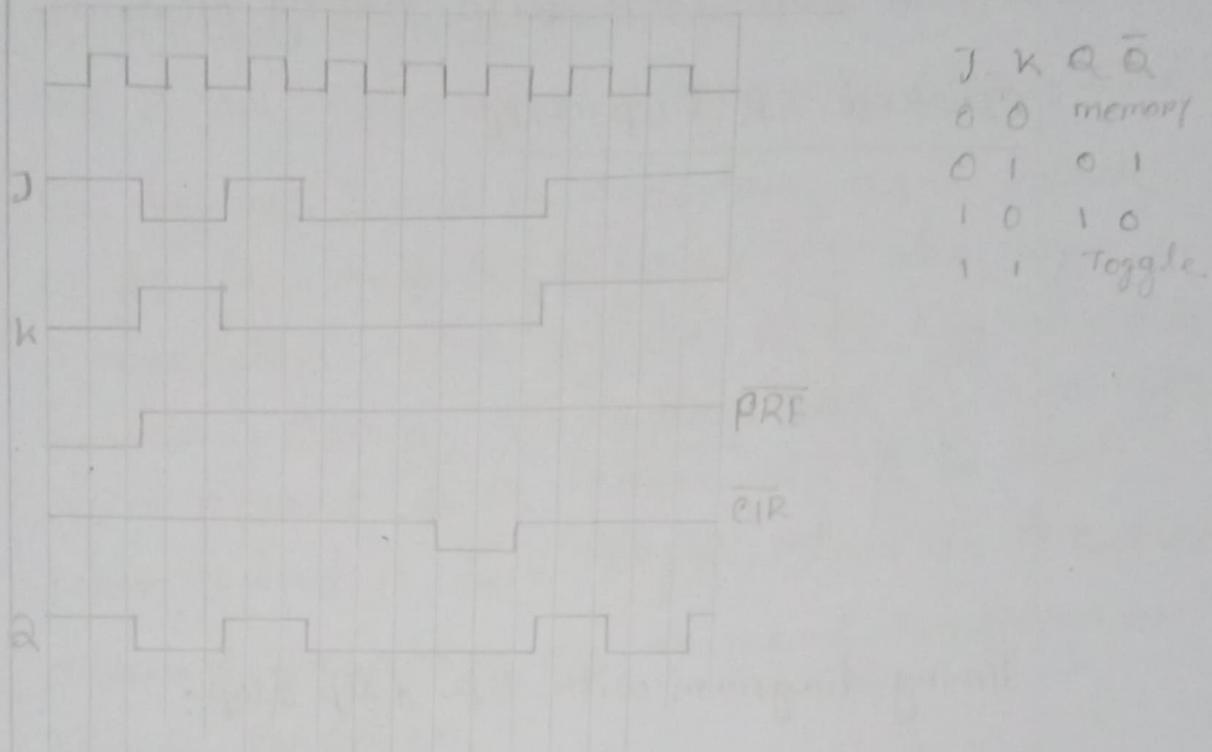


Fig. Negative edge triggered diagram

Difference between positive and negative edge triggered JK flip-flop:

Positive edge triggered

- i) A Positive edge triggered is the low-to-high transition.

Negative edge triggered

- i) A Negative edge triggered is the high-to-low transition.

ii) Draw and explain SR and JK master-slave flip-flop with timing diagram:

Clocked SR flip-flop:

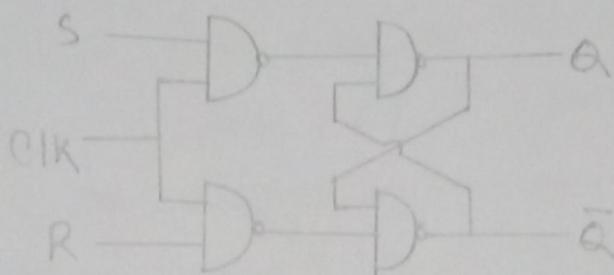


Fig: SR flip-flop

Timing diagram with SR flip flop:

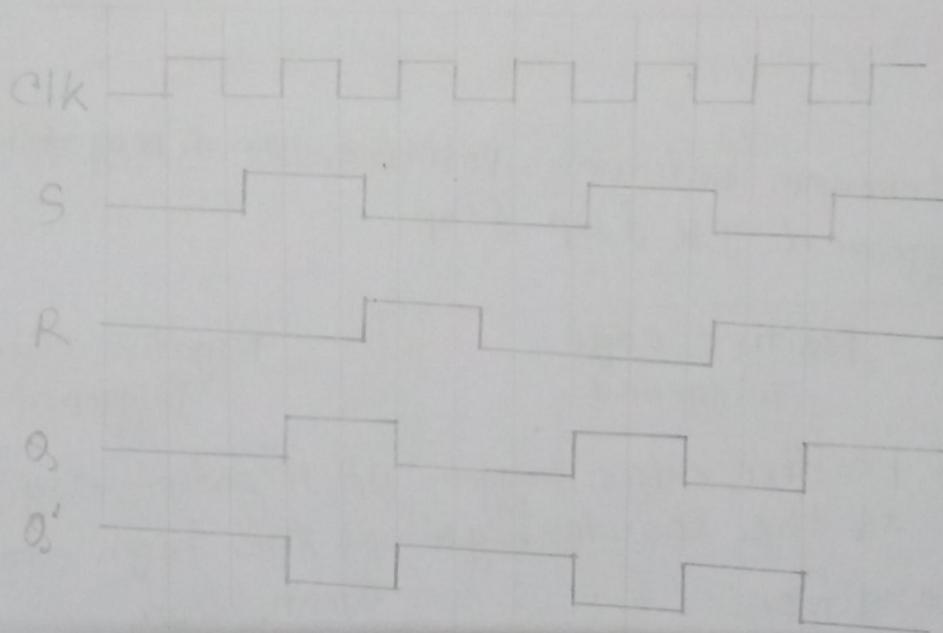


Fig: Timing diagram with SR flip-flop

In our description of SR flip-flop operation, that two signals are applied to the ~~S~~ S and R or type of R-S type flip-flop is used.

The figure S and R are low, as a result Q is low and  $\bar{Q}$  is high. S are high and R are low, as a result Q is high and  $\bar{Q}$  is low. Again, S are low and R are high, as a result Q is low and  $\bar{Q}$  is high. When S and R are high, this is the Race around Condition or Jamped Condition or Toggle condition.

### Master Slave JK flip-flop:

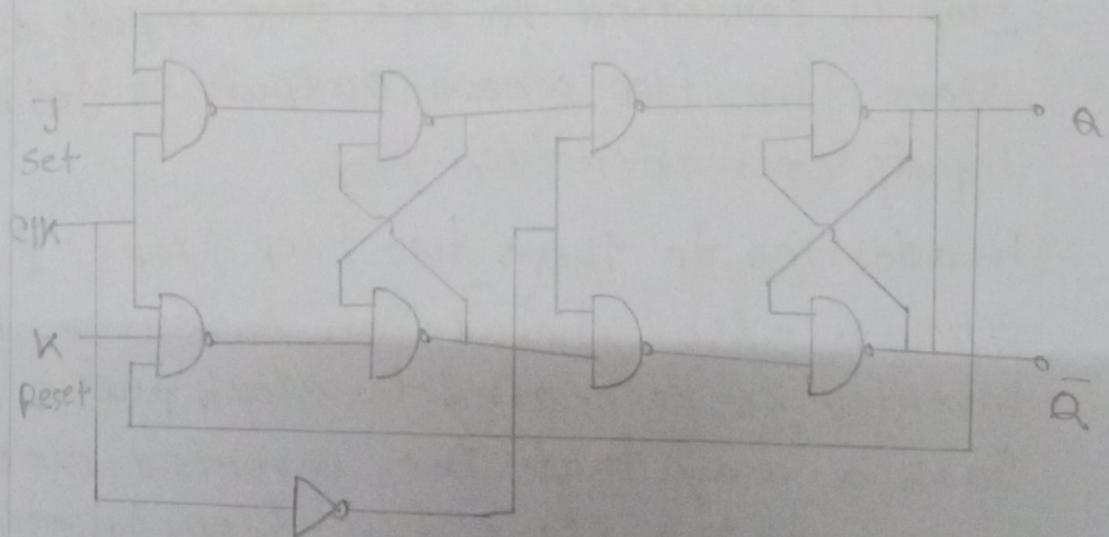


Fig: master slave JK flip-flop

Timing diagram of master slave JK flip-flop;

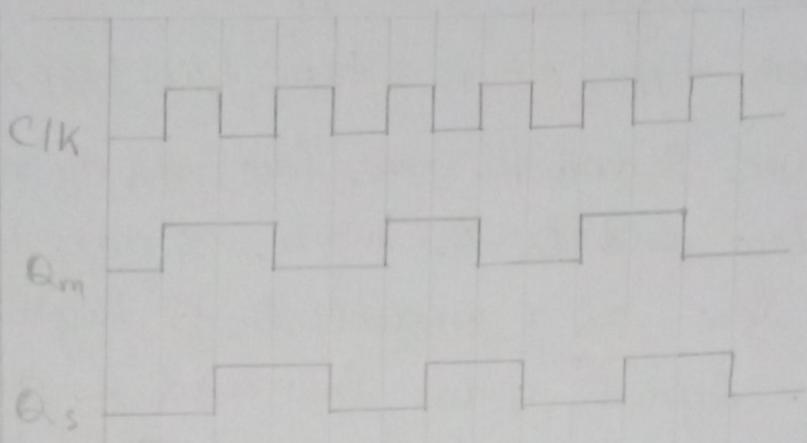


Fig: master slave timing diagram

The master slave flip-flop is basically a combination of JK-flip-flops connected together in a series configuration. Out of these, one acts as the "master" and the other as a "Slave". The output from the master flip-flop is connected to the two inputs of the Slave flip-flop whose output is fed back to inputs of master flip-flop.

In addition to these two flip flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if  $CP=0$  for master flip-flop, then  $CP=1$  for a slave flip-flop. and if  $CP=1$  for master flip flop then it becomes 0 for slave flip-flop.

12) Given A Astable Multivibrator:

$$R_1 = 2.0 \text{ k}\Omega = 2 \times 10^3 \Omega$$

$$R_2 = 4.3 \text{ k}\Omega = 4.3 \times 10^3 \Omega$$

$$C = 0.1 \mu\text{F} = 0.1 \times 10^{-6} \text{ F}$$

$$= 1 \times 10^{-7} \text{ F}$$

We know,

$$T = 0.693 (R_1 + 2R_2) \cdot C$$

And,

$$f = \frac{1}{T} = \frac{1}{0.693(R_1 + 2R_2)C}$$

$$= \frac{1.44}{(R_1 + 2R_2)C}$$

$$= \frac{1.44}{[2 \times 10^3 + 2(4.3 \times 10^3)]} \times (1 \times 10^{-7})$$

$$= 1358.49 \text{ Hz.}$$

$$= 1.35 \times 10^3 \text{ kHz}$$

(Ans)

$$13) \text{ Given, Duty cycle } = \frac{R_1 + R_2}{(R_1 + 2R_2)} = 80\% = 0.8$$

$$\text{frequency, } f = \frac{1}{T} = 10 \text{ kHz} = 10 \times 10^3 \text{ Hz}$$

$$\text{Capacitor, } C = 0.004 \mu\text{F}$$

$$= 0.004 \times 10^{-6} \text{ F}$$

We know,

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)C} = 10 \text{ kHz} = 10 \times 10^3$$

$$\Rightarrow R_1 + 2R_2 = \frac{1.44}{(10 \times 10^3) \times (0.004 \times 10^{-3})}$$

$$R_1 + 2R_2 = 36 \quad \text{--- (1)}$$

Again, eq @ from,

$$\frac{R_1 + R_2}{(R_1 + 2R_2)} = 0.8$$

$$\Rightarrow \frac{R_1 + R_2}{36} = 0.8$$

$$\Rightarrow R_1 + R_2 = 0.8 \times 36 \times (0.004 \times 10^{-3})$$

$$= 28.8 \Omega \quad \text{--- (2)}$$

$$\therefore R_1 + 2R_2 = 36$$

$$R_1 + R_2 = 28.8$$

$$\underline{\underline{R_2 = 7.2 \Omega}} \Rightarrow 72 \times 10^{-4} \text{ k}\Omega$$

Given eq (1),

$$R_1 = 28.8 - R_2$$

$$= 28.8 - 7.2$$

$$= 21.6 \Omega = 216 \times 10^{-4} \text{ k}\Omega.$$

$$\therefore R_1 = 216 \times 10^{-4} \text{ k}\Omega$$

$$R_2 = 72 \times 10^{-4} \text{ k}\Omega$$

(Ans)

14) Given,

$$V_{CC} = 5V$$

$$I_{CCL} = 2mA = 2 \times 10^{-3}A$$

$$I_{CCH} = 3.5mA = 3.5 \times 10^{-3}A$$

$\therefore$  Compute the power dissipation in low-state,

$$\begin{aligned} PD_L &= V_{CC} \times I_{CCL} \\ &= 5 \times 2 \times 10^{-3} \\ &= 10 \times 10^{-3} \end{aligned}$$

Again,

Compute the power dissipation in high-state,

$$\begin{aligned} PD_H &= V_{CC} \times I_{CCH} \\ &= 5 \times 3.5 \times 10^{-3} \\ &= 17.5 \times 10^{-3} \end{aligned}$$

Compute the average dissipation is -

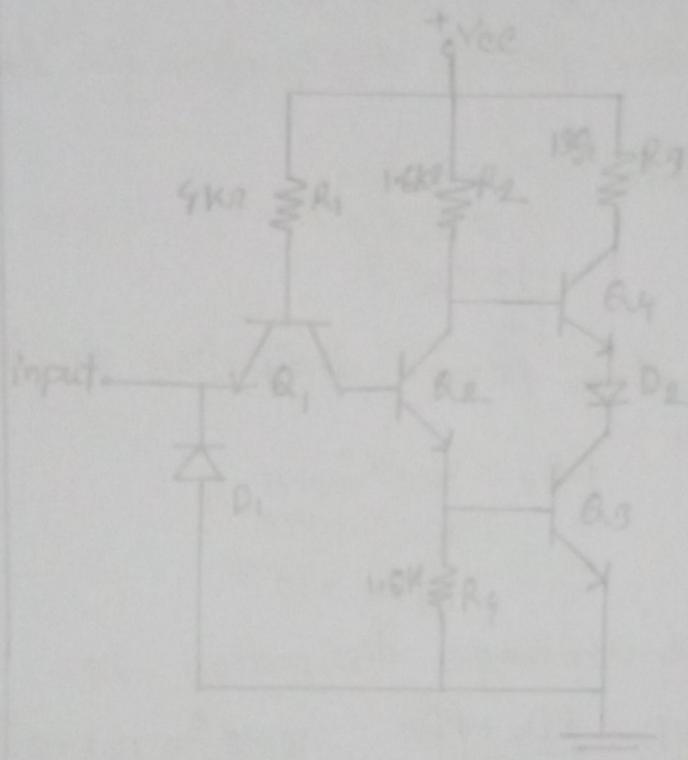
$$\begin{aligned} PD &= \frac{PD_L + PD_H}{2} = \frac{10 \times 10^{-3} + 17.5 \times 10^{-3}}{2} \\ &= 0.01375 \\ &= 13.75 \times 10^{-3} \end{aligned}$$

(Ans)

→ \*

15) proper diagram of TTL Inverter, NAND, NOR gates.

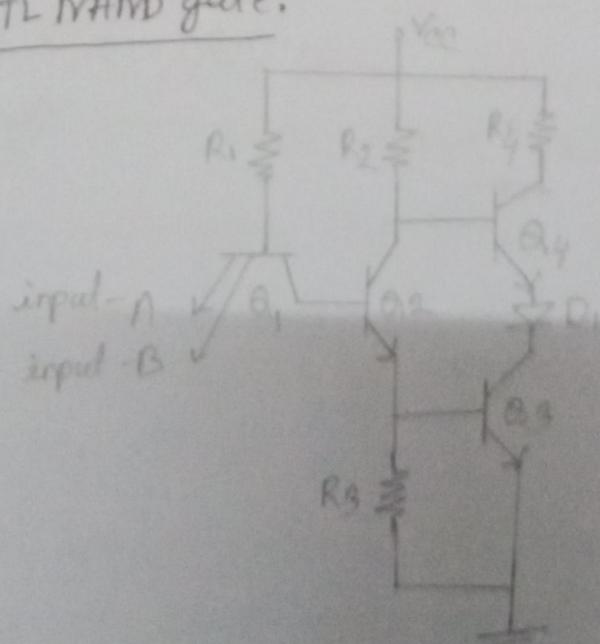
### TTL Inverter:



input	output
0	1
1	0

Fig: TTL Inverter

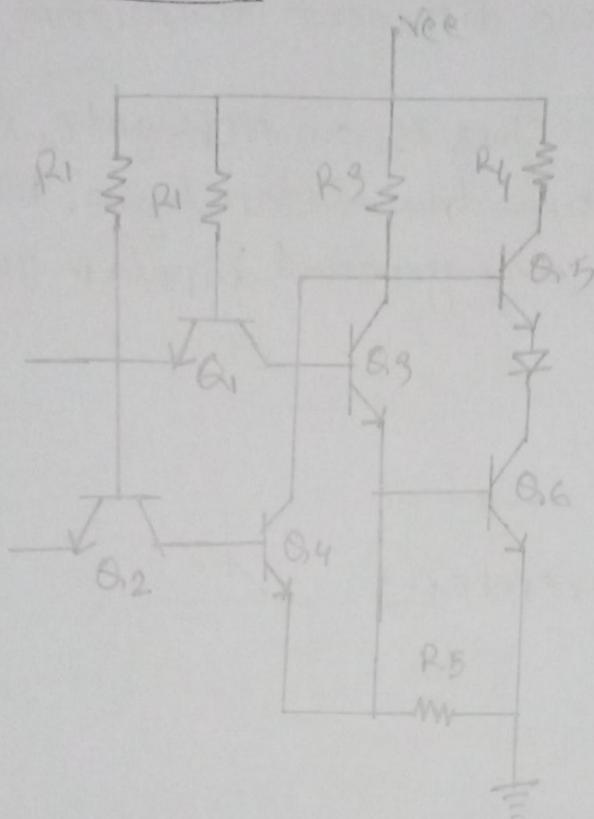
### TTL NAND gate:



input	output	
A	B	Y
0	0	1
0	1	1
1	1	1
1	0	0

Fig: NAND gate

### TTL NOR gate



input		output
A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

Fig: TTL NOR

TTL: TTL is an acronym for Transistor-Transistor Logic. It relies on circuits built from bipolar transistors to achieve switching and maintain logic states.

TTL Inverter: The basic TTL inverter consists of three stages: a current steering input, a phase splitting stage, and an output driver stage.

TTL NAND gate: A TTL NAND gate logic circuit has at least four bipolar junction transistors in which the input has two emitters. The

Output is taken between the emitter and collector of two different transistors.

TTL NOR gate: This is an NOR gate implemented using transistor-transistor logic. NOR gate circuit using any general bipolar junction transistors.

—\*—

16) CMOS inverter:

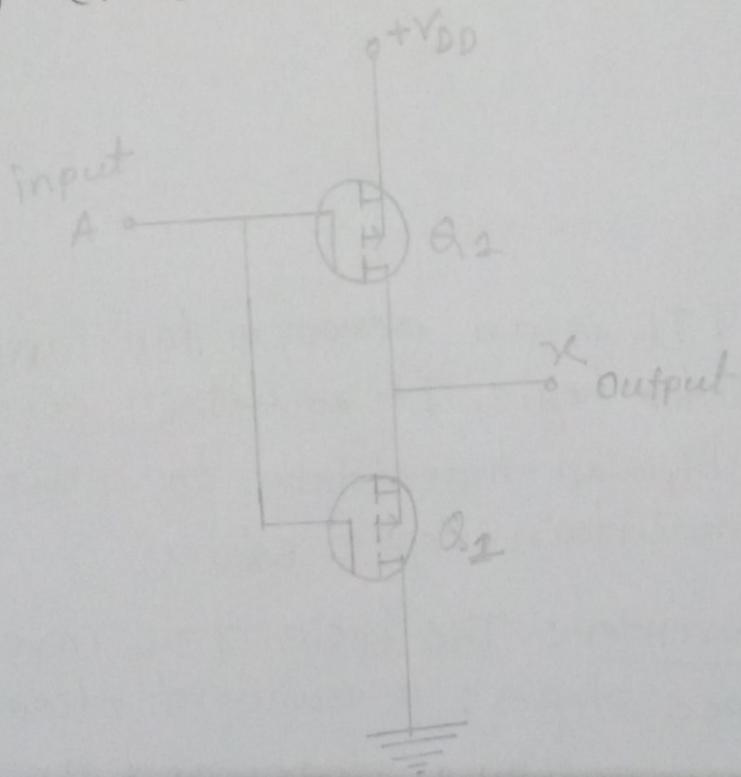
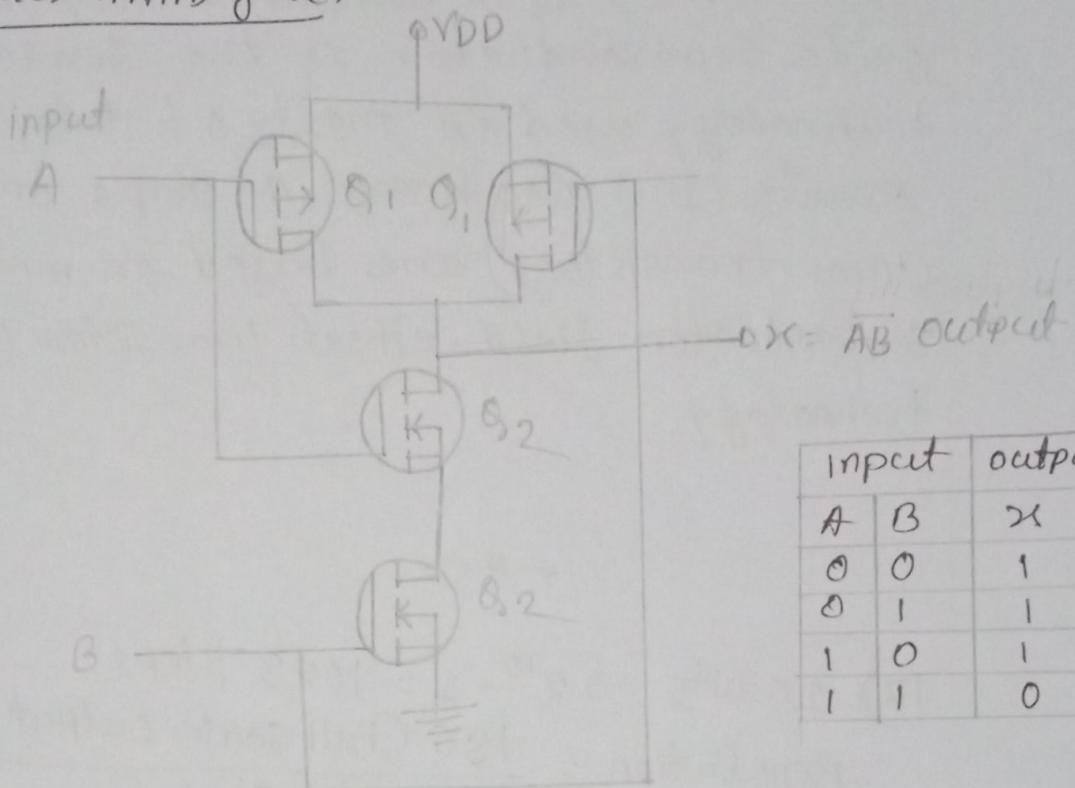


Fig: CMOS - inverter

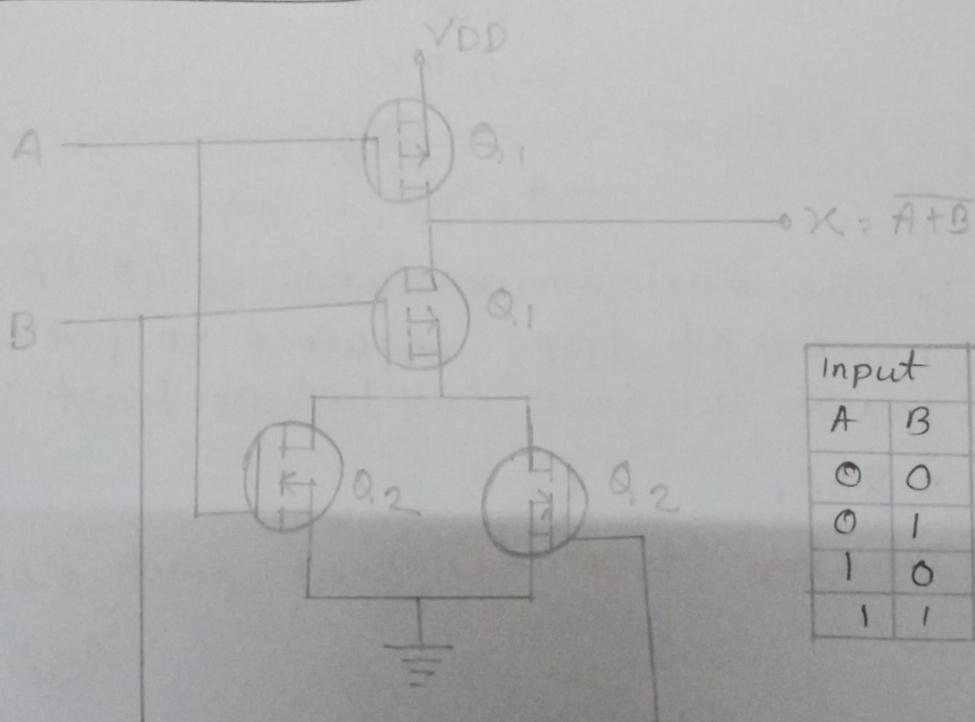
### cmos NAND gate



input	output	
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

Fig: cmos NAND gate

### cmos NOR gate:



input	output	
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

Fig: cmos-NOR gate.

CMOS: CMOS is a complementary metal-oxide semiconductor is the semiconductor technology used in most of today's integrated circuits (ICs) also known as chips or microchips. CMOS transistors are based on metal-oxide semiconductor field-effect transistor (MOSFET) technology.

- \* -

17) 10 bits  $\rightarrow 2^{10} - 1 = 1023$  steps

$$\text{Resolution} = \frac{\text{FSO (Full Scale Output voltage)}}{\text{steps size}}$$

$$= \frac{5}{1023}$$

$$= 4.88 \text{ mV}$$

$$\approx 5 \text{ mV}$$

(Ans)

- \* -

18) The maximum resolution is 40 mA. The number of steps required to produce 10 mA full scale will be at least  $10 \text{ mA} / 40 \text{ mA} = 250$ .

Therefore, it requires at least 8 bits,

(Ans)

19

20) Given, resolution  $\leq 20 \text{ mV}$  on  $20 \times 10^3 \text{ V}$

$$\text{F.S.O}/A_{fs} = 12 \text{ V}$$

we know,

$$\text{resolution} \cdot K = \frac{A_{fs}/\text{F.S.O}}{2^n}$$

$$\text{or}, \frac{12}{2^n} \leq 20 \times 10^{-3}$$

$$\text{or}, 12 \leq 20 \times 10^3 \times 2^n$$

$$\text{or}, \frac{12}{20} \times 10^3 > 2^n$$

$$2^n \leq 600$$

$$\log_2 2^n \leq \log_2 600$$

$$\log_2 2^n \leq \log_2 2^9$$

$$\therefore n \leq 9 \quad (\text{Ans})$$

21) Conversion time of successive approximation ADC depends upon the number of bits only, and not on the value of the voltage.  
Hence, Conversion time,  $80 \text{ ms} = 80 \times 10^{-3} \text{ s}$ .

(Ans)

- 4 -

22) A monostable multivibrator:

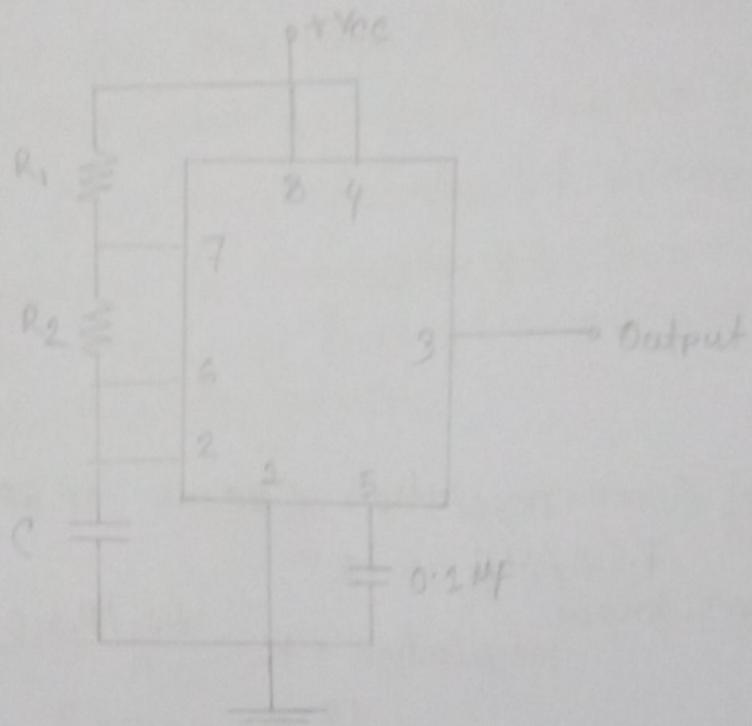


Fig: monostable multivibrator using 555 timer

Hence pin configuration:

1 → Ground ; 2 → Trigger ; 3 → Output ;  
4 → Reset ; 5 → Control voltage ; 6 → Threshold ;  
7 → Discharge ; 8 → +vee (input)

operation of monostable multivibrator: Firstly, when the circuit is switched ON, transistor  $Q_1$  will be in OFF state and  $Q_2$  will be in ON state. This is the stable state. As  $Q_1$  is OFF, the collector voltage will be  $V_{cc}$  at point A and hence  $C_1$  gets charged. A positive triggered pulse applied at the base of the transistor  $Q_2$  turns the transistor ON. This decreases the collector voltage, which turns OFF the transistor  $Q_2$ . The capacitor  $C_1$  starts discharging at this point of time. As the positive voltage from the collector of transistor  $Q_2$  gets applied to transistor  $Q_1$ , it remains in ON state. This is the quasi-stable state or meta-stable state.

— \* —

23  
30)

24) Output voltage =  $k \times$  input voltage

$$k = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{2.0}{100}$$

$$= 0.02$$

$$(01100100)_2 = (?)_{10}$$

$$\begin{array}{r} 128 \ 64 \ 32 \ 16 \ 8 \ 4 \ 2 \ 1 \\ 0 \ 1 \ \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \end{array}$$

$$= (100)_{10}$$

Again,

$$\text{input voltage. } = (179)_{10}$$

$$\text{output voltage} = k \times \text{input voltage}$$

$$= 0.02 \times 179$$

$$= 3.58 \text{ V}$$

(Ans)

$$(10110011)_2 = 179_{10}$$

$$k = 0.2$$

— \* —

"Starting"