

## Section B.

2020. 6(b)

what is 555 timer? 8 Pin

⇒ The 555 timer IC is an integrated circuit (IC) used in a variable variety of timer, delay, pulse

1. what is timer (555)?

⇒ The 555 timer is an 8 pin Integrated Circuit (IC) used in a variety of timer, delay, pulse generation and oscillator applications.

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The 555 timer is an 8 pin IC that is capable of producing accurate time delays and/or oscillator.

2020. 6(b) Draw the pin Configuration of a 555 timer IC and explain the function of each pin.

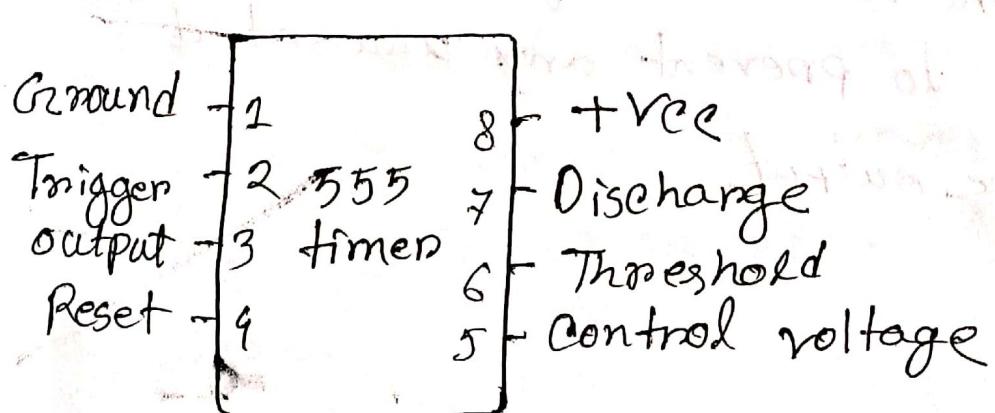


Fig: Pin Configuration of 555 timer

Explain no of pin:

Pin-1: Ground Terminal: All the voltages are measured with respect to this terminal. Ground reference voltage, low(0).

Pin-2: Trigger: The negative input to comparator No 1. A Negative pulse on this pin "sets" the internal flip-flop when the voltage drops below  $\frac{2}{3} V_{cc}$  causing the output to switch from a "Low" to a "High" state.

Pin-3: Output: It is the output pin of the IC, connected to the  $Q'(Q \bar{ })$  of the F/F with an inverter or between as shown in the figure.

Pin-4: Reset: This pin is used to "reset" the internal flip flop controlling the state of the output, pin-3. This is an active-low input and is generally connected to a logic "1" level when not used to prevent any unwanted resetting of the output.

Pin-5: Control voltage: This pin controls the timing of the 555 by overriding the 2/3 reference level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a  $10\text{ nF}$  capacitor to eliminate any noise.

Pin-6: Threshold: The positive input to comparator No 2. This pin used to reset the flip-flop when the voltage applied to it exceeds 2/3 V<sub>cc</sub> causing the output to switch from "HIGH" to "Low" state. This pin connects directly to the RC timing circuit.

Pin-7: Discharge: The discharge pin is connected directly to the collector of an internal NPN transistor which is used to "discharge" the timing capacitor to ground when the output at pin 3 switches "Low".

Pin-8: ~~+vec~~; This is the power supply pin and for general purpose TTL 555 timers is between 4.5 V and 15 V.

2020 6(a): Draw the internal functional diagram of a 555 timer and explain its basic operation. What are the applications of 555 timer?

### Application of 555 timer:

- i) The 555 IC is used for tone generation.
- ii) It is used to make an alarm circuit.
- iii) They also used for frequency division applications.
- iv) The IC 555 is used as a relaxation oscillator.
- v) They are also used in digital counter circuits.
- vi) IC 555 is widely used for electronics projects.
- vii) IC 555 is used as a pulse generation.

### Internal functional diagram of 555 timer:

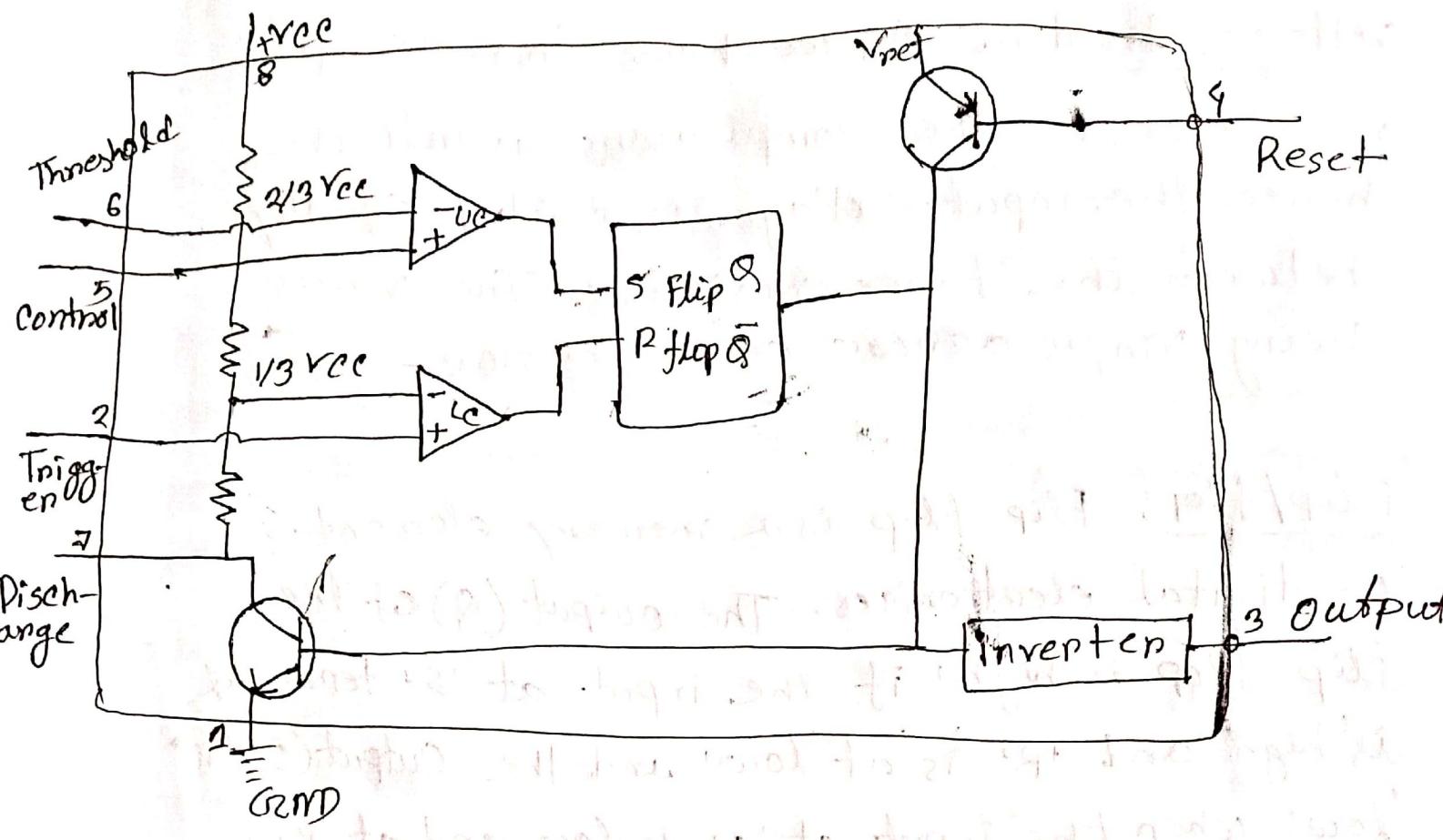


fig: Internal functional diagram of 555 timer

### Basic operations:

Comparators: The comparators are the basic electronic component which compares the two input voltages i.e. between the inverting (-) and the non inverting (+) input then the output is more than the inverting input then the output of the comparator is high. Also the input resistance of an ideal comparator is infinite.

Voltage dividers: As we know that the input resistance of the comparators is infinite hence the input voltage is divided equally between the three resistors. The value being  $V_{in}/3$  across each resistor.

Flip/flop: Flip-flop is a memory element of digital electronics. The output ( $Q$ ) of the flip-flop is 'high' if the input at 'S' terminal is 'high' and 'R' is at 'low' and the Output ( $Q$ ) is 'low' when the input at 'S' is low and at 'R' is high.

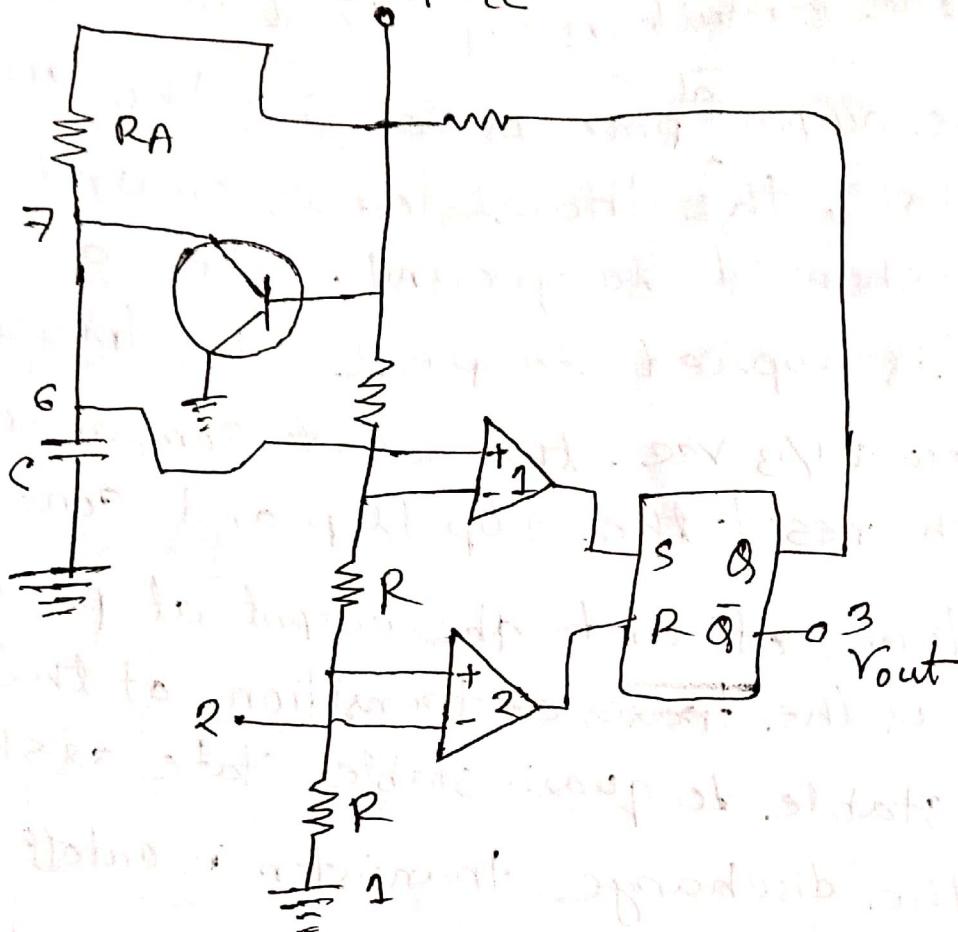
2015. 8(b),

2019. 8(a): Discuss the operation of a 555 timer IC based monostable multivibrator.

⇒ A Monostable multivibrator (MMV) often called one-shot multivibrator is a pulse generator circuit in which the duration of the pulse is determined by the R-C network, connected externally to the 555 timer. In such a vibrator, one state of output is stable while the other is quasi-stable (usable).

The operation of the circuit is explained below:

Initially, when the output at pin 3 is low i.e. the circuit is in a stable state, the transistor is on and capacitor - C is shorted to ground. When a negative pulse is applied to pin 2, the trigger input falls below  $+1/3 V_{cc}$ , the output Comparator goes high which reset the flip flop and consequently the transistor turns off and the output at pin 3 goes high. This is the transition of the output from stable to quasi-stable state as shown in figure. As the discharge transistor is cutoff, the capacitor C begins charging toward  $+V_{cc}$  through resistance  $R_A$  with a time constant equal to  $R_A C$ . When the increasing capacitor voltage becomes slightly greater than  $+2/3 V_{cc}$ , the output of Comparator 1 goes high, which sets the flip flop. The transistor goes to saturation, thereby discharging the capacitor C and the output of the timer goes low, as illustrated in figure.



2015. 8(a) What are the different applications of timer?

- ⇒ i) LED Flasher
- ii) Frequency generator
- iii) As a memory unit
- iv) Turn on device for certain time.

2014.8(b) Design an astable multivibrator using 555 timer and explain its operation. 555

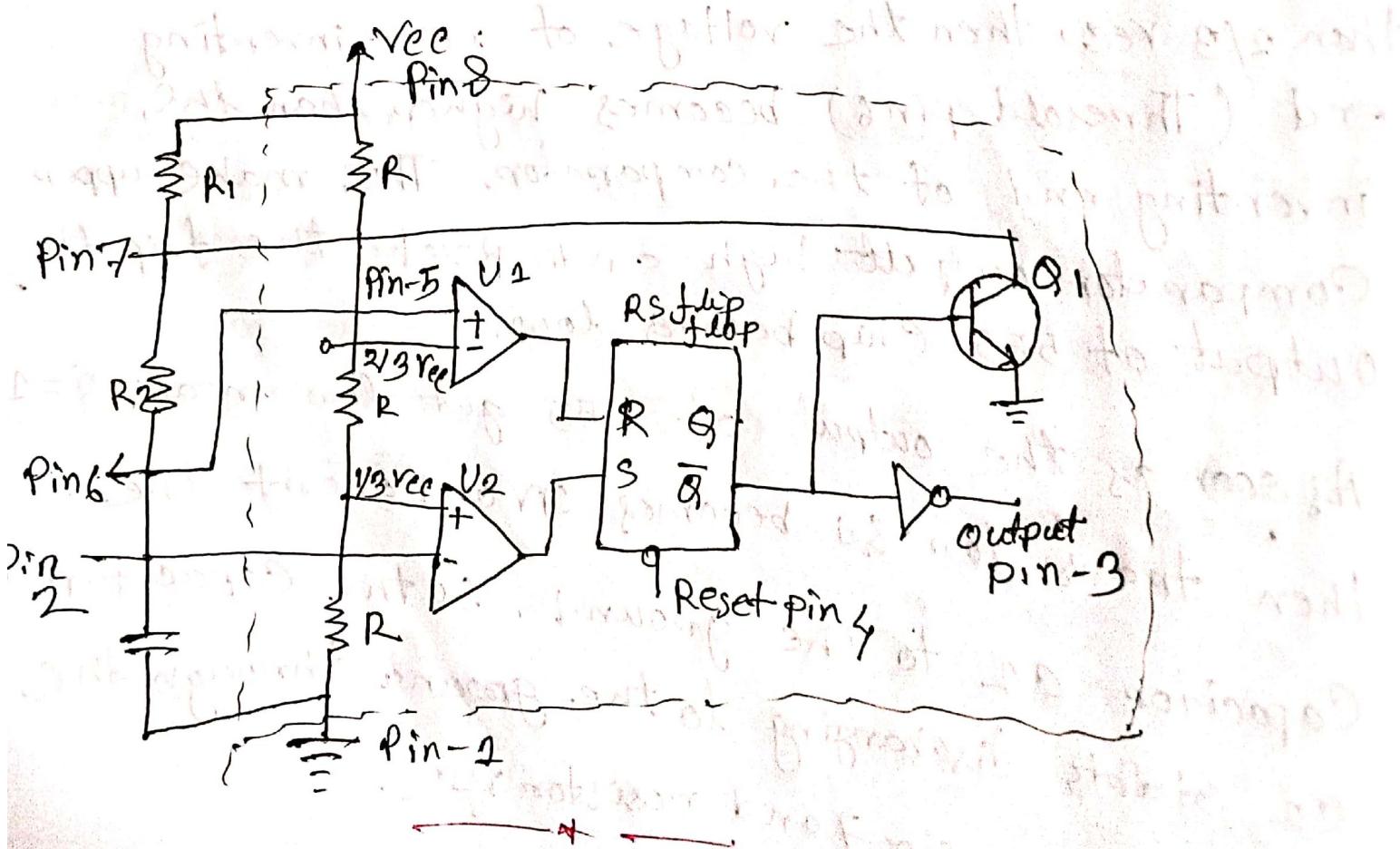
- i) When initially power is turned ON, Trigger pin voltage is below  $V_{CC}/3$ , that makes the lower comparator output high and sets the flip flop and output of the 555 chip high.
- ii)  $Q_1 = 0$ ,  $\bar{Q} = 0$  is directly applied to base of transistor. As the transistor is OFF, capacitor  $C_1$  starts charging and when it gets charged to a voltage above than  $V_{CC}/3$ , then lower comparator output becomes low and flip flop output remains the same as previous.
- iii) Now when capacitor charging gets to voltage above than  $2/3 V_{CC}$ , then the voltage of non-inverting end (Threshold pin 6) becomes higher than the inverting end of the comparators. This makes upper comparator output high and resets the flip flop output of 555 chip becomes low.
- iv) As soon as the output of 555 get low means  $\bar{Q} = 1$  then transistor  $\text{Q}_1$  becomes ON and short the capacitor  $C_1$  to the ground. So the capacitor  $C_2$  starts discharging to the ground through the Discharge pin 7 and resistor  $R_2$ .

v) As capacitor voltage get down below the  $V_{cc}$ , upper comparator output becomes low, now SR flip-flop remains in the previous state as both the comparators are low.

vi) While discharging, when capacitor voltage gets down below the  $V_{cc}/3$ , this makes the lower comparator output high and sets the flip-flop again and 555 output becomes high.

vii) Transistor  $Q_1$  becomes OFF and again capacitor  $C_1$  starts charging.

### Diagram of Astable multivibrator



2020.5(b) mention some applications of Latch.

- \* The applications of these basic digital elements are-
- i) These circuits are known for storing the information in the form of bits. These are known as memory elements.
  - ii) The usage of pulse latches follows the same behaviour of flip-flops but good enough to generate a quick response.
  - iii) In the two phase synchronous systems to avoid the transit count, the data latches (D-latches) are used.
  - iv) It is widely used to store the data and the codes for computations.

2019.6(a) Different between Flip-flop and Latch:

<u>Flip-flop</u>	<u>Latch</u>
1. Flip-flop is a bistable device i.e., it has two stable states that are represented as 0 and 1.	2. Latch is also a bistable device whose states are also represented as 0 and 1.
2. It is a edge triggered device.	2. It is a level triggered device.

3. Gates like NOR, NOT, AND, NAND are building blocks of flip flops.
3. These are also made up of gates.
4. A flip-flop always have a clock signal.
4. Latches doesn't have a clock signal.
5. Flip-flop can be build from Latches.
5. Latches can be build from gates.
6. D Flip-flop, JK flip flop
6. SR latch, D latch.
7. It checks the inputs but changes the output only at times defined by the clock signal or any other control signal.
7. It checks the inputs continuously and responds to the changes in inputs immediately.

2018. 5(a) what is Latch and flip-flop?

Latch: A latch is a special type of logical circuit. It is a storage device that holds the data using the feedback lane. The latches have low and high two stable states.

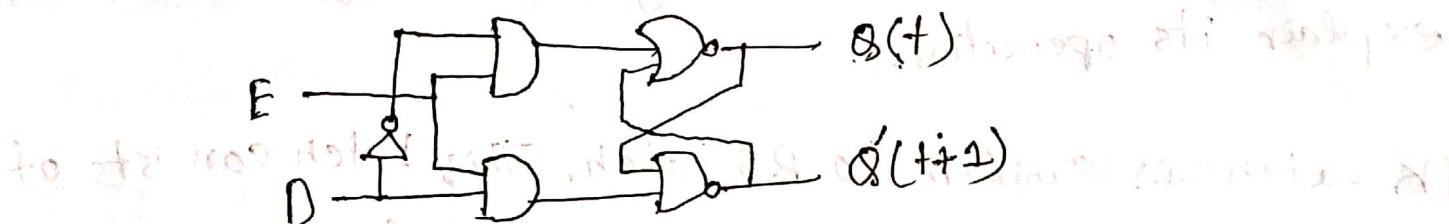
Flip-flop: A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "One" and the other

represents a "Zero". Flip-flops are used as memory elements in sequential circuit.

—\*—

2014. 8 5(c): Discuss how an SR latch is converted into D-latch.

→ There is one drawback of SR-Latch. That is the next state value can't be predicted when both the inputs S & R are one. So, we can overcome this difficulty <sup>also</sup> by D Latch. It is called as Data latch. The circuit diagram of D Latch is shown-



This circuit has single input D and two outputs  $Q(t)$  and  $Q'(t+1)$ . D Latch is obtained from SR latch by placing an inverter between S amp; R inputs and connecting D input to S. That means we eliminated the combinations of S & R one of same value.

If  $D=0$ ,  $S=0$  &  $R=1$ , then the next step  $Q'(t+1)$  will be equal to "0" irrespective of present ~~value~~ state  $Q(t)$  values.

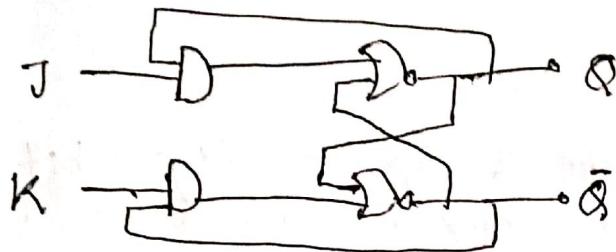
if  $D=1 \rightarrow S=1$  &  $R=0$  then the next state  $Q^{(t+1)}$  will be equal to "1" irrespective of present state,  $Q^{(t)}$  values,

the State table of D Latch.

D	$Q^{(t+1)}$
0	0
1	1

2018-6(b): Draw a circuit diagram of a J-K latch and explain its operations - 

JK Latch is similar to RS Latch. This Latch consists of 2 inputs J and K as shown in the below figure. The ambiguous state has been eliminated here. When the inputs of JK latch are high, then output toggles. The output feedback to inputs is the only difference we see here, which is not there in the SR Latch.



J	K	$Q(t)$	$Q'(t+1)$
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	1
0	1	1	0
1	0	1	0
1	1	1	0

## Flip-Flop

Flip-flop: A flip flop in Digital electronics is a circuit with <sup>stable</sup> two states that can be used to store binary Data.

## Applications of flip flop:

These are <sup>the</sup> various types of flip-flops being used in digital electronics circuits and the applications of flip flop are as specified below~

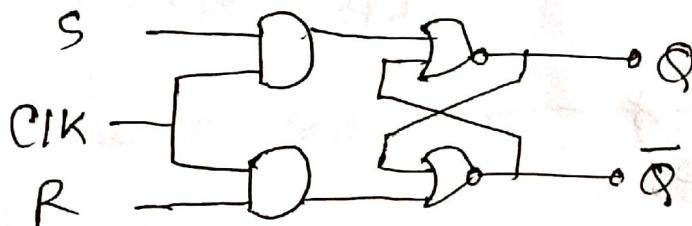
- i) Counters
- ii) Frequency dividers
- iii) Shift Registers
- iv) Storage
- v) Data storage
- vi) Latch
- vii) Memory
- viii) Registers

## Types of Flip-flop:

- 1) SR Flip-flop
- 2) JK "
- 3) D "
- 4) T "

The SR flip flop is a 1 bit memory bistable device having two input, Set and Reset.

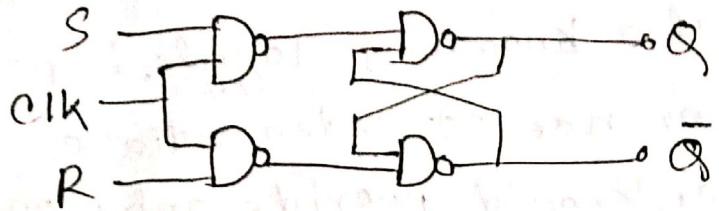
SR flip-flop: This is the most common flip flop among all. This simple flip flop circuit has a Set input (S) and Reset input (R). In this system when you set "S" as active, the output "Q" would be high, and "Q'" would be low. Once the outputs are established, the wiring of the circuit is maintained until "S" or "R" go high, or power is turned off.



SR flip flop used as a storage device for a single data bit.

CK	S	R	Q(t+1)
1	0	0	Hold
1	0	1	Reset
1	1	0	Set
1	1	1	Invalid

S	R	Q(t)	Q'(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	X
1	1	1	X



SR flip flop

clk S R Q Q̄

0 0 0 Ne Ne

1 0 0 Ne Ne

1 1 0 " 0 → Set

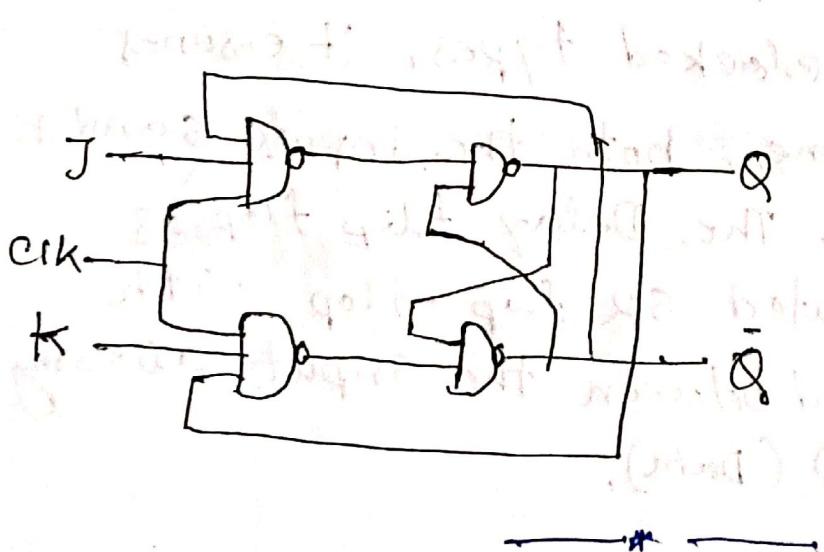
0 1 0 1 0 → Reset

1 1 1 1 1 →

SR flip flop has got 2 outputs Q and Q-bar  
and it has got 2 inputs S and R  
so it is a 2 bit flip flop or 1 bit register

JK Flip Flop:- A JK flip flop is called a universal programmable flip-flop because, using its inputs J, K preset and clear, function of any other flip-flop can be imitated.

A JK flip flop is the modification of SR flip-flop with no illegal state. In this the J input is similar to set ~~S~~ input of SR flip-flop and K input is similar to the Reset input of SR flip flop. The symbol of JK flip-flop



clk J K Q Q̄

0 0 0 Ne Ne

1 0 0 " "

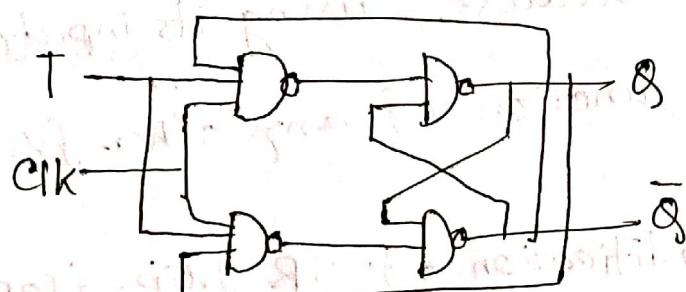
1 0 1 0 → Reset

0 1 0 1 → Set

1 1 0 } toggle

T Flip Flop: T flip flop is also known as Toggle Flip-flop. To avoid the occurrence of intermediate state in SR flip-flop, we should provide only one input to the flip flop called the Trigger input or Toggle input (T).

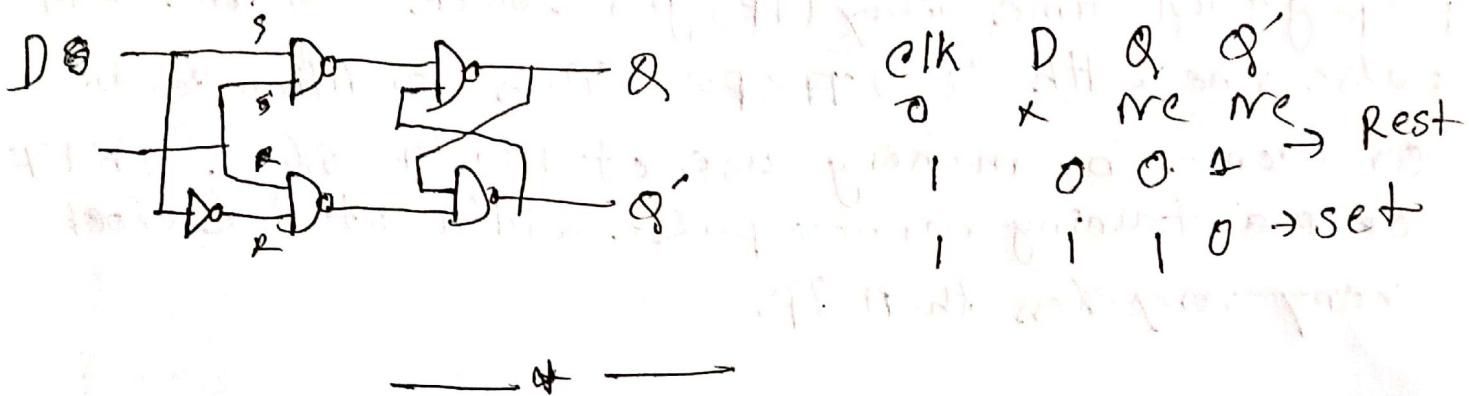
We can design the T flip-flop by making simple modifications to the JK flip-flop, we can convert a JK flip-flop into T flip flop. So, a T flip-flop is sometimes called as single input JK flip-flop.



Clk	T	Q	Q'
0	X	0	1
1	0	1	0

D Flip flop: The D flip flop is the most important flip flop from other clocked types. It ensures that at the same time, both the inputs S and R are never equal to 1. The Delay flip flop is designed using a gated SR flip-flop with an inverter connected between the inputs allowing for a single input D (Data).

The single data input, which is labeled as "D" is used in place of the "Set" input and for the complementary "Reset" input the inverter is used.



### \* Limitations of SR flip flop:

The limitation with a S-R flip-flop using NOR and NAND gate is the invalid state,  $(S=R=1)$ . The problem can be overcome by using a stable SR flip-flop that can change outputs when certain invalid states are met regardless of the conditions of either the set or the Reset inputs.

### Application of SR flip flop:

It is mainly used to store data or information, whenever operations, storage and sequencing are required. These signal circuits are used.

## Limitations of JK flip flop

When we give both J and K input as 1, then the output toggles more than once. This condition is called as "Race Around Condition". It occurs when the propagation time delay (TP) gets lower than the clock pulse width (PW). This condition can be overcome by making use of Master-Slave JK FF or maintaining narrow pulse width of the clock very very less than TP.

## Advantage of JK flip flop:

If both input J and K have high inputs assigned to them, then the output Q toggles between the high and low states. As a result, there are no ambiguous states and the JK FF can operate as a set/Reset FF.

when the two inputs are tied together, the JK flip-flop can act as a T flip-flop that is widely used in binary counters.

## Disadvantages

When both the inputs and clock pulse signal are at level 1 after the output is complemented once, output transmission will start getting repeated and continuous. This results in a raged condition.

→ Advantages of master-slave JK Flip Flop:

The master-slave configuration has the advantage of being edge-triggered, making it easier to use in larger circuits, since the inputs to a flip-flop often depend on the state of its output. The circuit consists of two D flip-flop connected together.

The purpose of the Master-slave is to overcome from from "Race-around condition".

Clocked SR FF:

FF are nothing but clocked latch. Thus if an additional clock pulse is applied to a latch then this kind of circuitry will be termed as flip F.