University of Rajshahi

Department of Computer Science and Engineering

B.Sc (Engg.) Part-II, Even Semester, Examination 2022

Course Code: CSE 2231

Course Title: Computer Architecture and Organization

Time: 3 hours **Marks: 52.5**

(Answer **SIX** questions taking at least **THREE** from each Section)

Section-A

1. a) Define Multiprocessor and multicore computer. How cache memory isused to speed up memory access? How a greater performance improvement be obtained by using multiple levels of cache? 2.75

   b) How does the control unit execute instructions? How it interacts with other components of a central processing unit (CPU)- Discuss with an example. 4

   A 200 MHz processor was used to execute a program with thefollowing instruction mix and clock cycle counts.

Instruction Type	Instruction Count	Clock Cycle Count
Integer arithmetic	450000	1
Data transfer	320000	2
Floating point	150000	2
Control transfer	80000	2

   Determine the effective CPI, MIPS rate, and execution time for this program.

   c) A 16 bits hypothetical machine has two I/O instructions: 2

   0011 Load AC from I/O and 0111 Store AC to I/O

   The 12-bit address identifies a particular I/O device. Show the program execution (contents of memory and registers in hexadecimal) for the following program:

   (1) Load AC from device 5. (2) Add contents of memory location 940. (3) Store AC to device 6.Assume that the next value retrieved from device 5 is 3 and that location 940 containsa value of 2.

2. a) Define interrupt. How Interrupts are provided primarily as a way to improve processing efficiency- Discuss with necessary diagrams. 2.75

   b) How to control the access to and the use of the system bus? Discuss mezzanine architecture with the necessary figure. 2+2

   Suppose a 16-bit register of the following format is used for storing binary floating point numbers. Mantissa (M) is denoted using normalized sign-magnitude fraction and Exponent (E) is expressed in excess-64 form. Then (1) How many bits are used for the fractional mantissa? (2) What should be the bit patterns for $(7.5)_{10}$ and $(-16.125)_{10}$?

   c) Define fetch cycle and execute cycle with and without interrupt. 2

P.T.O.

Time: 3 hours

3.	a)	What is the problem with signed-magnitude representations? How 2's complement method can be used to solve the problem? How a full adder can be realized using two half-adders?	3
	b)	Design an 8-bit 2's complement adder-subtractor (using 4-bit adder module) that can perform X-Y, X+Y, Y-X operations.	3
	c)	Discuss some cases where overflow occurs. Derive logical expression and draw logic circuit of overflow detection.	2.75
4.	a)	Draw and discuss the block diagram of a simple accumulator based CPU.	3
	b)	Discuss how a 16-bit Bit-Sliced ALU is designed by four 4-bit ALU slices.	3.75
	c)	Write the differences between Ripple carry adder and Carry-lookahead adder.	2

Section-B

5.	a)	Discuss any two characteristics that destroy information from memory. Draw the internal structure of the 8E1DRAM chip.	2.75
	b)	How TLB with the paging HW speeds up the address translation process- discuss with a necessary figure. Consider a system that has logical address = 6 bits, physical address 5 bits and page size= 16 words. Calculate the number of pages and number of frames. Also draw the page table.	2+1
	c)	What is internal fragmentation? Draw a schematic representation of hardware used for segmentation.	3
6.	a)	What is meant by thrashing? How the preemptive allocation technique is used for dynamic memory allocation?	2.75
	b)	How set-associative mappingworks- Discuss with an example. A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address formula?	3
	c)	How doesthe virtual memory concept increase the degree of multiprogramming? Discuss the steps in handling page faults with the necessary diagram. How effective access time is calculated?	1+2
7.	a)	Mention different approaches to the design of hardwired control units with benefits and limitations.	2
	b)	Design the control unit of the GCD controller: draw state transition graph, state table and also logic diagram using the one-hot method.	4.75
	c)	Draw the structure of a hardwired and microprogrammed control unit.	2
8.	a)	What do you mean by address translation? Explain a typical dynamic address-translation system.	3.75
	b)	Define the term bus arbitration. What are the basic schemes for it? Which one is better in which situation?	3
	c)	Explain the concept of I/O processor.	2

University of Rajshahi
Department of Computer Science and Engineering
B.Sc (Engg.) Part-II Even Semester Examination 2021
Course Code: CSE 2231
Course Title: Computer Architecture and Organization

Time: 3 hours **Marks: 52.5**

(Answer Six questions taking Three questions from each part)

Part-A

1. **a)** Define the functional elements of a core. Explain the structure of a multicore computer. **2.75**

   b) Mention the name of registers in the control unit and discuss their functions. **2+1**

   Calculate CPI and MIPS for a CPU with 100 MHz frequency which is executing a benchmark program with the following instruction mix.

   ALU: occurrence = 38% and cycle/instruction= 1
   LOAD & STORE: occurrence= 15% and cycle/instruction= 3
   Others: occurrence= 47% and cycle/instruction= 5

   c) Mention the classes of interrupts. How multiple interrupts can be handled? **3**

2. **a)** Draw the structure of a small accumulator-based CPU. Explain the functions of the following registers: register files, status register, and stack pointer. **3**

   b) Describe instruction-level pipelining with necessary diagram. **2+1**

   A Minicomputer has 12-bit address bus. What is the address space of these computers and what is the largest possible memory of these computers in bytes if the memory location is 1 Byte?

   c) What do you mean by CISC and RISC processors? Mention some features of RISC processors. **2.75**

3. **a)** Mention some drawbacks of signed magnitude representation. Derive the equation of 2's complement representation of signed integers. **2.75**

   b) Design an 8-bit adder-subtractor with a diagram. **3**

   c) How an overflow is handled in an adder circuit. Discuss logical expression and logic circuit of overflow detection. **3**

4. **a)** Why fixed-point multiplication requires more HW than fixed-point addition? Design a 2-bit binary multiplier circuit **2.75**

   b) Mention some features of Booth's algorithm in the multiplication process. How does the algorithm work? - Explain with an example. **3**

   c) What is multiport RAM? Draw its symbolic representation. Draw a generic datapath unit for implementing logical and arithmetic operations. **3**

Part-B

5. a) Discuss memory restoration in destructive readout memory. Design 16bit 2-D RAM using dynamic RAM cells and show the RAM addressing scheme. **2.75**

   b) Discuss the structure of the address-translation system using translation look-aside buffer with the paging hardware. **2+1**

   If main memory and TLB access times are 100ns and 60ns, respectively. The TLB hit ratio is 99%. What is effective access time?

   c) What is internal fragmentation? Draw a schematic representation of hardware used for segmentation **3**

6. a) "Nonpreemptive allocation is not efficient"- why? And how it is solved in the preemptive allocation technique? **2+1**

   A processor can support a maximum of 8GB where the memory is word addressable (a word = 4 bytes). What is the minimum size of the address bus of the processor?

   b) Draw the basic structure of a cache. What are the limitations of direct and associative cache mapping techniques? How those problems are overcome using set-associative mapping? - Discuss with an example. **2.75**

   c) Mention some benefits of using virtual memory. Discuss the steps in handling page fault. **2+1**

   Consider memory access time is 200ns and page fault service time is 8ms. If 1 access out of 1000 causes a page fault. Then calculate the effective access time.

7. a) How the Micro programmed control circuit can be designed? - give example. **2**

   b) Show the basic structure of the hardwired control unit in brief. **2**

   c) Design the control unit of the GCD processor using the classical method. **4.75**

8. a) Define the term bus arbitration. What are the basic schemes for it? Which one is better in which situation? **2.75**

   b) Define isolated I/O. How is the data transfer from the I/O device to the main memory carried out in the programmed I/O method? - discuss with the necessary figure. **3**

   c) What are the functions of DMA controller? Draw circuitry required for DMA Controller. Which component of the computer system initiated the DMA transfer- discuss with the necessary block diagram. **3**

University of Rajshahi

Department of Computer Science and Engineering

B. Sc. (Engg) Part-II Even Semester Examination 2020

Course: CSE 2231 (Computer Architecture and Organization)

Full Marks: 52.5 Duration: 3 (Three) Hours

Answer 06 (Six) questions taking any 03 (Three) from each section

Section-A

1. a) What is meant by 16-bit computer? Explain how operating system bridges the gap between software and hardware. 3.00
   b) Define latency and throughput. Explain the factors influencing computer speed. 3.00
   c) Suppose you have two processors A and B with clock period 5ns and 10ns respectively. On average 5.4 and 4.5 clock cycles are required to execute one instruction for A and B respectively. Compare the performance of the two processors. 2.75

2. a) Compare hardwired and microprogrammed controls. How PC works for branching instructions. 3.00
   b) Explain instruction cycle with example. 3.00
   c) Define addressing mode? Describe the instructions R1←M[B]+R3; R2←M[M[ADR]] + M[PC+H] with respect to addressing mode. 2.75

3. a) What is interrupt service routine? Compare vectored and non-vectored interrupts. 2.75
   b) Discuss about different types of data manipulation instructions. 3.00
   c) Explain I/O configuration with its proper block diagram. 3.00

4. a) Briefly describe the structure of a fixed point ALU with diagram. 3.00
   b) Shortly discuss how a 16-bit bit-sliced ALU is designed by four 4-bit ALU slices. 3.00
   c) Distinguish between Ripple-carry adder and Carry-lookahead adder with diagram. 2.75

Section-B

5. a) Discuss about program control instructions. 2.00
   b) Suppose you have a CPU with only 3 registers connected as input through two multiplexers MUX A and MUX B. They are also connected as output through a multiplexer MUX D. The CPU supports only 4 instructions (ADD, SUB, MUL, DIV). Draw the register organization of the mentioned CPU and write the codewords of the instructions: R3←R2+R1; R1←R3-R2; R2←R1*R3. 3.75
   c) Explain how pipelining improves the performance. Suppose you have a processor with 2.5GHz clock and 4 blocks for pipelining. You have a program with 3×10^5 instructions in which only 45% instructions can be executed through pipelining. Calculate speedup factor for pipelining. 3.00

6. a) Define peripherals with examples. Mention the requirements for I/O interface. 2.75
   b) Compare synchronous and asynchronous data transfer scheme. Explain asynchronous data transfer system and mention its advantages. 3.00
   c) Discuss about strobe-controlled data transfer system with necessary diagram. 3.00

7. a) Mention the advantages of DMA. Illustrate the steps of DMA transfer from I/O to memory. 3.00
   b) Illustrate the function of virtual memory. Suppose your computer system needs 512B RAM and 512B ROM. Only the memory chips (RAM and ROM) of size 256B are available. Draw the diagram to illustrate the memory connection. 3.00
   c) Explain the function of cache memory to speedup computer system? Consider that 420 of memory references are available in the cache out of 600. Calculate the cache performance. 2.75

8. a) Design a micro-programmed control unit based on Wilkes design. 4.00
   b) Explain the concepts of interleaved memories. 2.75
   c) Distinguish between CISC and RISC processors. 2.00

University of Rajshahi

Department of Computer Science and Engineering

B.Sc. Engg. Part - II, Semester – Even, Examination 2019

Course: CSE2231 (Computer Architecture and Organization)

Full Marks-52.5 Time: 3 hours

[N.B. Answer any **SIX** questions taking **THREE** from each of the Section]

Section-A

1. (a) Define structure and function of computer. Discuss the structural development among different generation of computer in brief. 4
   (b) Distinguish between RISC and CISC machines. 1.75
   (c) Draw and briefly discuss the structure of an I/O processor. 3

2. (a) Specify the different I/O transfer mechanisms available. 3
   (b) Derive and explain an algorithm for adding and subtracting 2 floating point binary numbers. 4
   (c) Explain the representation of floating point numbers in detail. 1.75

3. (a) Write the logical expression of a full adder and half adder. Draw the circuit of an n-bit two's complement adder-subtractor. 3.75
   (b) What is carry lookahead adder? Draw a 2 bit carry lookahead adder in detail. 5

4. (a) Explain spatial and temporal expansion of bit sliced ALU. Also show the organization of the 2901 4 bit ALU slice. 4
   (b) Draw the symbol and logic diagram of a three port RAM. Also discuss a generic datapath unit with an ALU and a multiport RAM. 4.75

Section-B

5. (a) Define destructive and nondestructive readout. Discuss how restoration is carried out automatically with necessary diagram. 3
   (b) Draw the organization of 2D DRAM. 1.75
   (c) How do you increase the data transfer rate between RAM and CPU. Draw Rambus DRAM interface. 4

6. (a) What is address mapping? What is the function of address generation logic? Explain. 1.75
   (b) What is Translation look aside buffer? Discuss two stage address translation with segments and pages. 3
   (c) Consider a paging system in which M has a capacity of four pages. The execution of a program Q requires references to six distinct pages P_i where i = 1, 2, 3, 4, 5, 6 and i is the page address. The page address stream formed by execution Q is 2, 3, 6, 2, 1, 5, 2, 4, 5, 6, 2, 1. Show the action of three replacement policies in a common address trace. 4

7. (a) What is the function of control unit? Show the control signals that implement a subtraction instruction of the form SUB A, B. 3.75
   (b) Design a processor that perform factorial of a positive integer. 5

8. (a) In a cache-based memory system using FIFO for cache page replacement, it is found that the cache hit ratio H is low. The following proposals are made for increasing. 5
      (i) Increase the cache page size.
      (ii) Increase the cache storage capacity.
      (iii) Increase the main memory capacity.
      (iv) Replace the FIFO replacement policy by LRU.

   Analyze each proposal to determine its probable impact on H.
   (b) Explain synchronous DRAM technology in detail. 3.75

University of Rajshahi

Department of Computer Science and Engineering

B.Sc. (Engg.) Part-2 Even Semester Examination-2018

Course: CSE2231 (Computer Architecture and Organization)

Marks: 52.50 Time: 3 Hours

[N.B. Answer SIX questions taking THREE from each section.]

Section-A

1. (a) Distinguish between computer architecture and computer organization. 2.75
   (b) Define IAS computer. Discuss the organization of the CPU and main memory of the IAS computer. 4
   (c) Mention some important features of third generation computers. 2

2. (a) What do you mean by memory-mapped I/O and I/O mapped I/O. Give example. 2
   (b) Discuss the architectural extension of recent CPUs compared with a small accumulator-based CPU with necessary figures. 4.75
   (c) Define instruction pipelining. 2

3. (a) Design a multiplier that can multiply two fixed-point signed binary numbers. Give the algorithm and flowchart for the multiplication process. 5.75
   (b) Describe the data processing part of a simple floating-point arithmetic unit with diagram. 3

4. (a) Define overflow. How overflow detection logic is implemented. 2
   (b) Draw the overall structure of a high speed adder. 2.75
   (c) Discuss the register-level view of the 74181 4-bit ALU. 4

Section-B

5. (a) What are the functions of control unit in a computer system? Discuss the possible control signal generated to implement a subtraction instruction of the form SUB A,B with DP unit figure. 3.75
   (b) Design DMA controller: draw state transition graph, state table and also logic diagram using One-hot design method 5

6. (a) Define destructive read out (DRO). Give example. 2
   (b) Define address mapping. Discuss the structure of a dynamic address-translation system. 4
   (c) Define preemptive allocation with necessary figure. 2.75

7. (a) Distinguish between synchronous and asynchronous buses. Give example. 2.75
   (b) Discuss bus interfacing using tri-state logic with necessary figure. 3
   (c) Discuss bus arbitration using daisy chaining. Mention some problems with this scheme. 3

8. (a) Discuss how cache memory helps to speed up the operation of a computer system. 3
   (b) Explain the concept of virtual memory and interleaved memory. 3
   (c) What do you mean by addressing mode? Shortly discuss indirect addressing mode. 2.75

University of Rajshahi
Department of Computer Science and Engineering
B.Sc. (Engg.) Part-2 Even Semester Examination-2017
Course: **CSE2231** (Computer Architecture and Organization)
Full Marks: 52.5 Time: 3:00 Hours

Section A

Answer any THREE questions.

1. (a) Mention some important features of second generation computers. 02
   (b) Discuss the organizational differences between EDVAC and IAS computers with necessary diagrams. 04
   (c) Explain some important speedup features of modern computers – in brief. 2.75

2. (a) How do you design overflow detection logic for 2's complement addition or subtraction? Design an 8-bit adder-subtractor using necessary diagram. 04
   (b) Define Booth's algorithm. Design a combinational array multiplier using full-adder array of 4x4 bit unsigned numbers. 03
   (c) Define fetch and execution cycle. 1.75

3. (a) Discuss how cache memory speeds up the operation of a computer system. 03
   (b) Explain the concepts of interleaved memories. 2.75
   (c) What do you mean by addressing mode? Discuss indirect and indexed addressing modes. 03

4. (a) Define the features of spatial and temporal expansion of ALU. 03
   (b) Discuss the organization of the 2901 4 bit ALU slice. 1.75
   (c) Write down some features of sequential ALU. Discuss in brief about the main internal features of a combinational ALU. 04

Section B

Answer any THREE questions.

5. (a) Explain the general condition of pipelining. 02
   (b) Design a control unit that computes the gcd of two positive integers. Draw the hardwired inter-connectivity, state diagram, state table and also logic diagram using one hot design methodology. 05
   (c) List the control signal needed to execute the following instruction A:=A+B. 1.75

6. (a) Distinguish the organizational differences between SRAM and DRAM. Discuss the organization of Rambus DRAM interface. 03
   (b) Define translation look-aside buffer. Discuss the two-stage address translation with segments and pages with necessary diagram. 04
   (c) Mention some reasons for using virtual memory. 1.75

7. (a) Draw and briefly discuss the structure of an I/O processor. 2.75
   (b) Discuss the operation of a typical DMA controller with block diagram. 3.5
   (c) Write the advantages and disadvantages of Programmed I/O over DMA controller with respect to program design complexity, I/O bandwidth and interface hardware cost. 2.5

8. (a) What is meant by bus arbitration? Shortly discuss different bus arbitration schemes. 04
   (b) What is interrupt? Write the steps taken by a CPU during an interrupt service handling. 03
   (c) What do you mean by CISC and RISC processors? Mention some features of RISC processors. 1.75