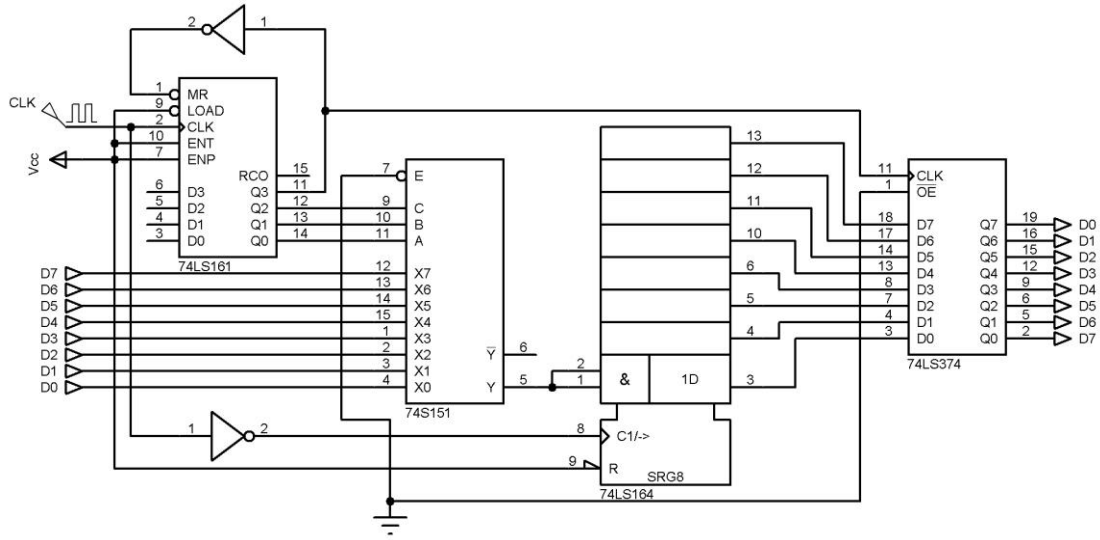
Lab Content
Course: CSE3112 (Computer Architecture and Organization Lab)

- **Experiment 1**

Title	Synchronous Data Transfer
Outline	• To design and implement a digital circuit to transfer data serially • At the sender end the parallel data is converted to serial data to transfer the data to receiver using a single data line. • At the receiver end the serial data will be reconstructed to its parallel form. • Both sender and receiver circuits should be synchronized using a single clock.
Apparatus	• 4-bit Binary Counter, 74LS161 • 8-input Multiplexer, 74LS151 • 8-bit Serial-in Parallel-out Shift Register, 74LS164 • Octal D-type Flip-Flop, 74LS374 • Hex Inverter, 74LS04 • Digital IC Trainer
Circuit Diagram	

Task	• Design of the digital circuit
	• Implementation of the design
	• Testing of the circuit
	• Report writing
	  ○ Name of the experiment
	  ○ Objective
	  ○ Apparatus
	  ○ Design of the circuit
	  ▪ Detail design methodology
	  ▪ Truth table (if required)
	  ○ Circuit Diagram
	  ○ Experimental data
	  ○ Result and discussion
	  ○ Precautions

Mode of Evaluation	Experiment, Viva and Report
Percentage of Weight	16%

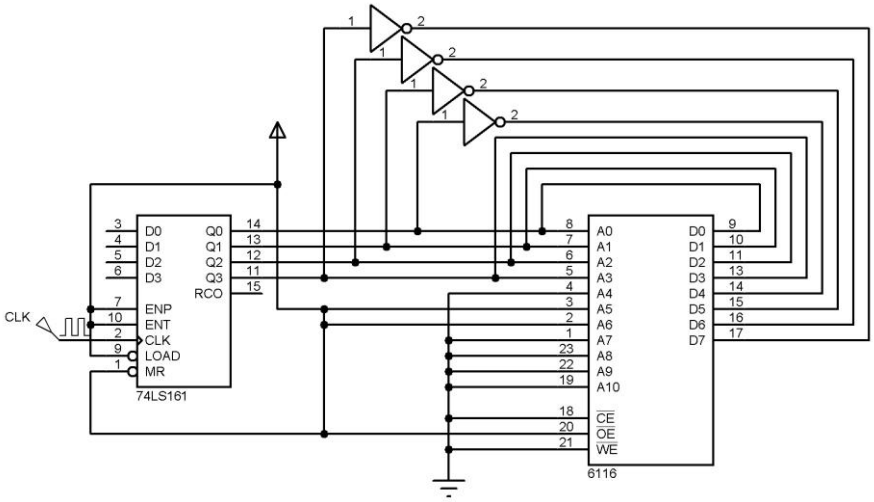
- **Experiment 2**

Title	Memory operations
Outline	• To design and implement a memory subsystem to store data in memory and then display the stored data into LED • Writing the following data into corresponding memory addresses using synchronized counter • Display the stored data into LED
Apparatus	• 4-bit Binary Counter, 74LS161 • Static RAM, 6116 • Hex Inverter, 74LS04 • Digital IC Trainer

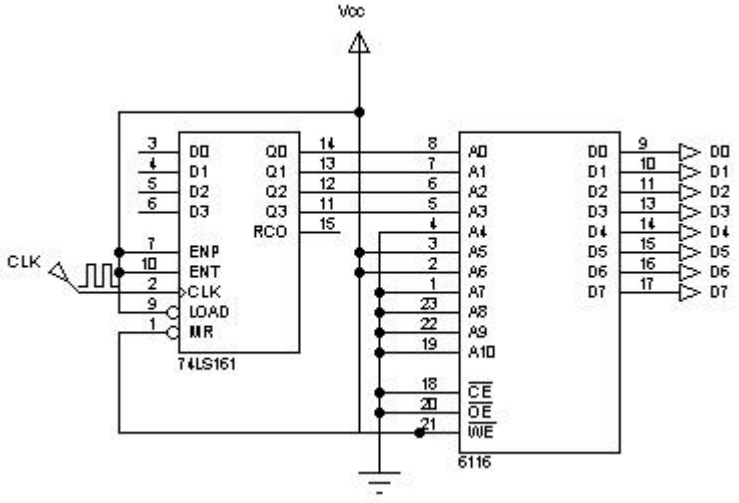
Address	Data
60	F0
61	E1
62	D2
. . .	. . .
6F	0F

Circuit Diagram

Data Write



Data Read



Task	• Design of the digital circuit
	• Implementation of the design
	• Testing the circuit
	• Report writing
	  ○ Name of the experiment
	  ○ Objective
	  ○ Apparatus
	  ○ Design of the circuit
	  ▪ Detail design methodology
	  ▪ Truth table (if required)
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	  ○ Precautions

Mode of Evaluation	Experiment, Viva and Report
Percentage of Weight	15%

- **Experiment 3**

Title	Frequency counter
Outline	• To design and implement a frequency counter. The input frequency will be divided by a constant divisor N (N=1, 2, …, 15) before feeding it to desired frequency counter. The output of the frequency counter should be show on a 7-segment display • Design a circuit for dividing the input frequency by a constant divisor N, where N is integer and variable. N should be easily changeable. • Design a circuit to count frequency and show the output on a 7-segment display.

Task	• Design of the digital circuit
	• Implementation of the design
	• Testing the circuit
	• Report writing
	  ○ Name of the experiment
	  ○ Objective
	  ○ Apparatus
	  ○ Design of the circuit
	  ▪ Detail design methodology
	  ▪ Truth table (if required)
	  ○ Circuit Diagram
	  ○ Experimental data
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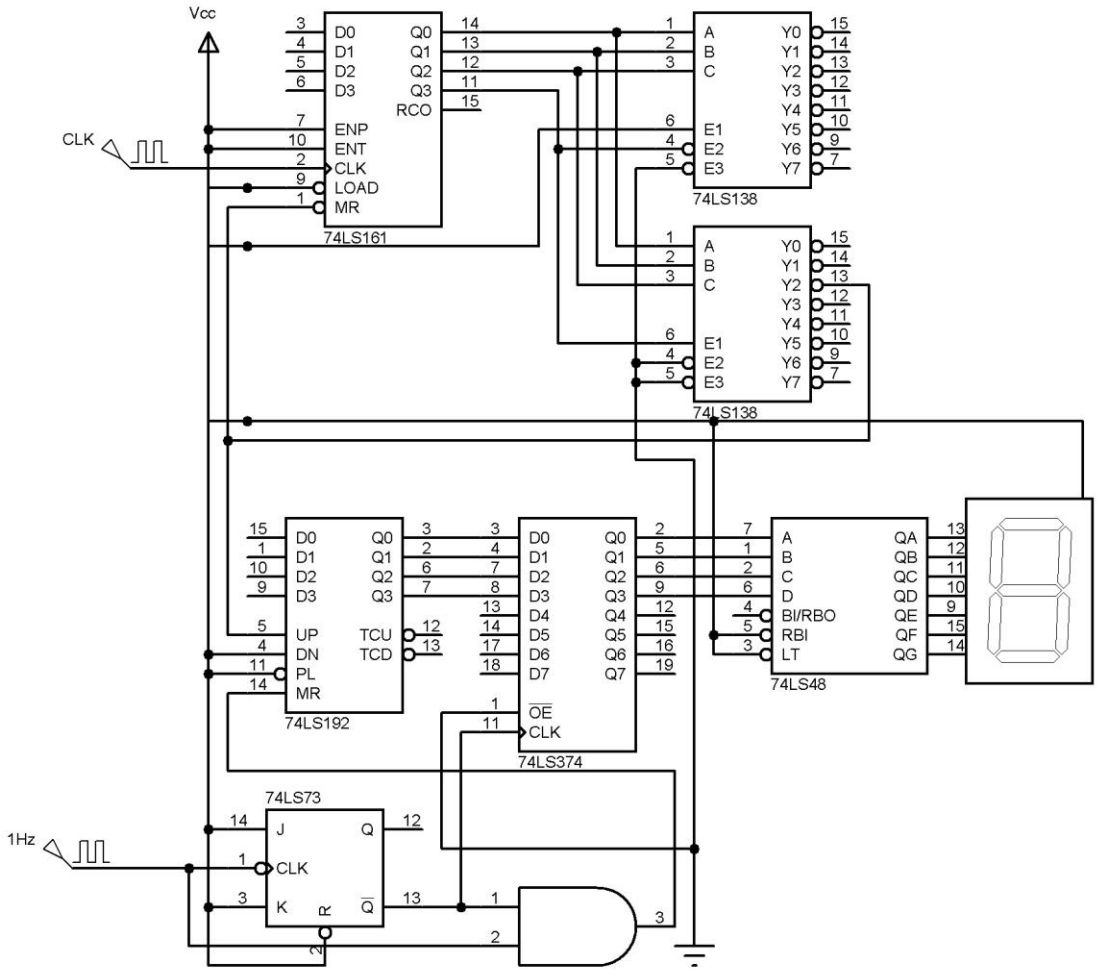
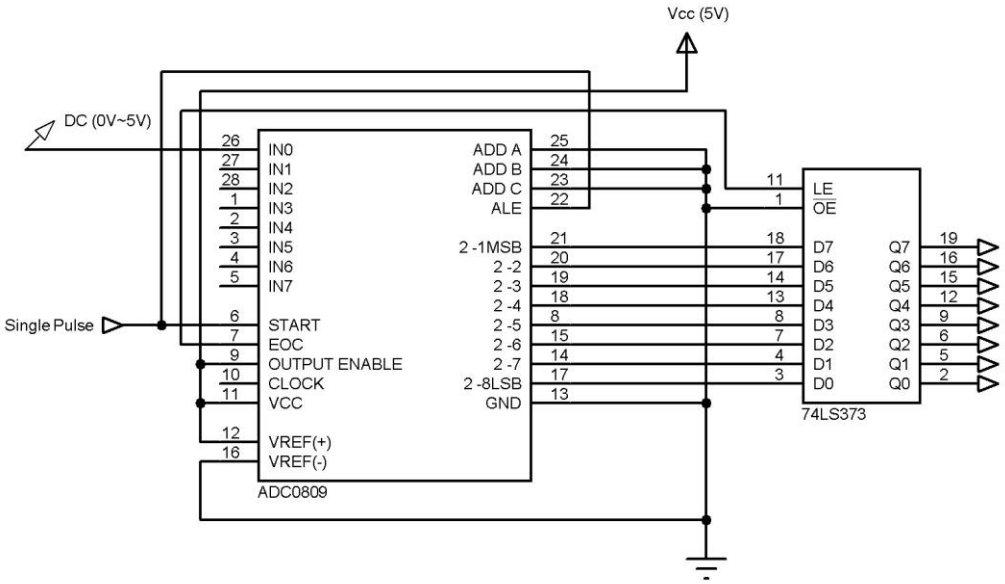
	  ○ Precautions

Circuit Diagram 	
Apparatus	• 4-bit Binary Counter, 74LS161 • 3 to 8 line Decoder, 74LS138 • 4-bit BCD Counter, 74LS191 • Dual J-K Flip-Flop, 74LS76 • Quad 2-input AND gate, 74LS08 • Octal D-type Flip-Flop, 74LS374 • BCD to 7-Segment Decoder, 74LS47 • 7-Segment Display LED • Digital IC Trainer
Mode of Evaluation	Experiment, Viva and Report
Percentage of Weight	19%

- **Experiment 4**

Title	Analog to Digital Convertion
Outline	• To design and implement a circuit to convert analog signal (potential difference) into digital data by using an Analog to Digital Converter than store the data in a latch and display the converted digital data using LED • Design a circuit with controls to initialize the conversion process. • Decode port if multiple input analog input lines available on ADC IC and required to digitize multiple analog input signals. • Design circuit to store digital signal in a letch automatically. (Required to synchronized with ADC IC)
Apparatus	• 8-bit µP Compatible A/D Converter ADC0809 • Octal D-type Letch, 74LS373 • Digital IC Trainer
Circuit Diagram	

Task	• Design of the digital circuit
	• Implementation of the design
	• Testing the circuit
	• Report writing
	  ○ Name of the experiment
	  ○ Objective
	  ○ Apparatus
	  ○ Design of the circuit
	  ▪ Detail design methodology
	  ▪ Truth table (if required)
	  ○ Circuit Diagram
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	  ○ Precautions

Mode of Evaluation	Experiment, Viva and Report
Percentage of Weight	14%

- **Experiment 5**

Title: Arithmetic circuit control design

Outline

- To design and implement arithmetic circuits with selection variable S_0 & S_1 and operand A (4 bits), B (4 bits) & C_{in} that generates the following operations:

S_0	S_1	$C_{in}=0$	$C_{in}=1$
0	0	F=A+B	F=A+B+1
0	1	F=A	F=A+1
1	0	F=B'	F=B'+1
1	1	F=A+B'	F=A+B'+1

- Construct truth table and K-Map to generate Boolean equations for the arithmetic circuit.
- Implement the circuit for according to the Boolean equations.

Apparatus

- 4-bit Binary Full Adder, 74LS283
- Quad 2-input AND gate, 74LS08
- Quad 2-input OR gate, 74LS32
- Hex Inverter, 74LS04
- Quad 2-input Exclusive-OR gate, 74LS86
- Digital IC Trainer

Truth Table

Input				Output	
S_0	S_1	A_i	B_i	X_i	Y_i
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	0	1	0	0
1	1	1	0	1	1
1	1	1	1	1	0

K-Map

X_i:

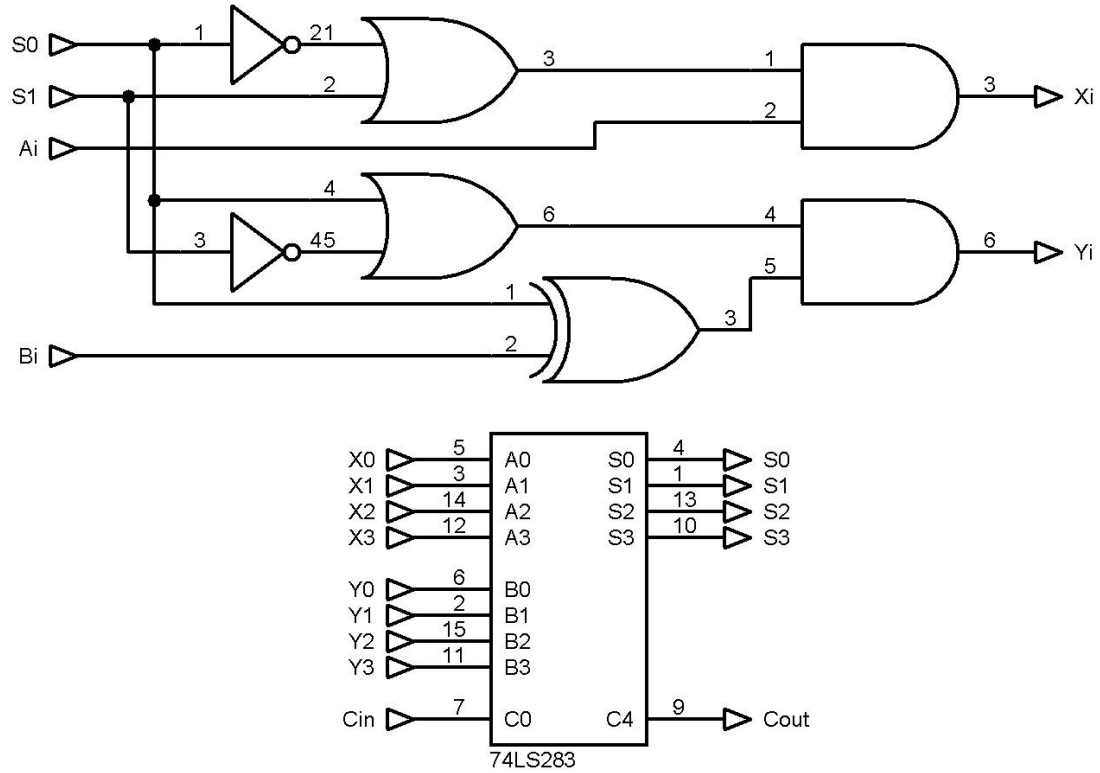
	$S_0'S_1'$	$S_0'S_1$	S_0S_1	S_0S_1'
$A_i'B_i'$	0	0	0	0
$A_i'B_i$	0	0	0	0
A_iB_i	1	1	1	0
A_iB_i'	1	1	1	0

$X_i = (S_0' + S_1)A_i$

Y_i:

	$S_0'S_1'$	$S_0'S_1$	S_0S_1	S_0S_1'
$A_i'B_i'$	0	0	1	1
$A_i'B_i$	1	1	0	0
A_iB_i	1	1	0	0
A_iB_i'	0	0	1	1

$Y_i = (S_0 + S_1')(B_i \oplus S_0)$

Circuit Diagram 	
Task	• Design of the digital circuit • Implementation of the design • Testing the circuit • Report writing o Name of the experiment o Objective o Apparatus o Design of the circuit ▪ Detail design methodology ▪ Truth table (if required) o Circuit Diagram o Experimental data o Result and discussion o Precautions
Mode of Evaluation	Experiment, Viva and Report
Percentage of Weight	13%

- **Experiment 6**

Title	Arithmetic circuit control design
Outline	• To design and implement arithmetic circuits with selection variable S_0 & S_1 and operand A (4 bits), B (4 bits) & C_{in} that generates the following operations:

S_0	S_1	C_{in}=0	C_{in}=1
0	0	F=A	F=A+1
0	1	F=A-B-1	F=A-B
1	0	F=B-A-1	F=B-A
1	1	F=A+B	F=A+B+1

• Construct truth table and K-Map to generate Boolean equations for the arithmetic circuit.
• Implement the circuit for according to the Boolean equations.

Apparatus	• 4-bit Binary Full Adder, 74LS283 • Quad 2-input AND gate, 74LS08 • Quad 2-input OR gate, 74LS32 • Hex Inverter, 74LS04 • Quad 2-input Exclusive-OR gate, 74LS86 • Digital IC Trainer

Truth Table

Input				Output	
S_0	S_1	A_i	B_i	X_i	Y_i
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	1	0	1
1	1	0	0	0	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	1	1

K-Map

X_i:

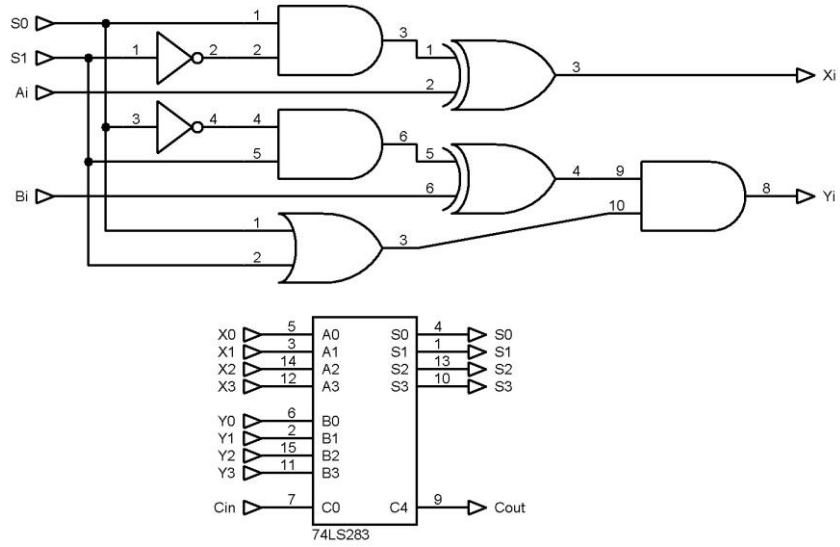
	$S_0'S_1'$	$S_0'S_1$	S_0S_1	S_0S_1'
$A_i'B_i'$	0	0	0	1
$A_i' B_i$	0	0	0	1
A_iB_i	1	1	1	0
A_iB_i'	1	1	1	0

$X_i = S_0S_1' \oplus A_i$

Y_i:

	$S_0'S_1'$	$S_0'S_1$	S_0S_1	S_0S_1'
$A_i'B_i'$	0	1	0	0
$A_i'B_i$	0	0	1	1
A_iB_i	0	0	1	1
A_iB_i'	0	1	0	0

$Y_i = (S_0 + S_1)(S_0'S_1 \oplus B_i)$

Circuit Diagram 	

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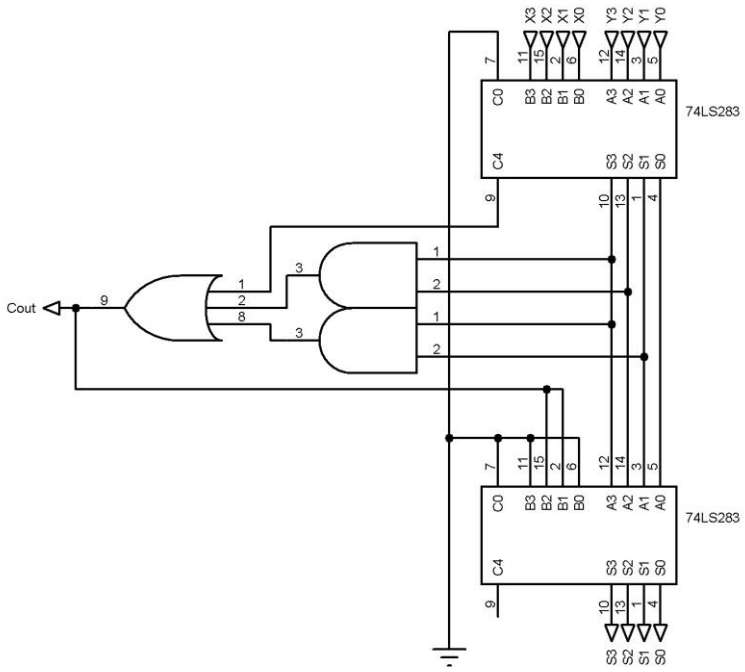
	  ○ Precautions

Mode of Evaluation	Experiment, Viva and Report
Percentage of Weight	13%

- **Experiment 7**

Title	ALU design
Outline	• To design and implement a BCD Adder circuit. • A BCD Adder is a digital combinational circuit that is used for the addition of two numbers in BCD arithmetic's. • Generate Boolean equations for the circuit. • Implement the circuit for according to the Boolean equations.
Apparatus	• 4-bit Binary Full Adder, 74LS283 • Quad 2-input AND gate, 74LS08 • Quad 2-input OR gate, 74LS32 • Digital IC Trainer
Circuit Diagram	
Task	• Design of the digital circuit • Implementation of the design • Testing the circuit • Report writing o Name of the experiment o Objective o Apparatus o Design of the circuit ▪ Detail design methodology ▪ Truth table (if required) o Circuit Diagram o Experimental data o Result and discussion o Precautions
Mode of Evaluation	Experiment, Viva and Report
Percentage of Weight	10%