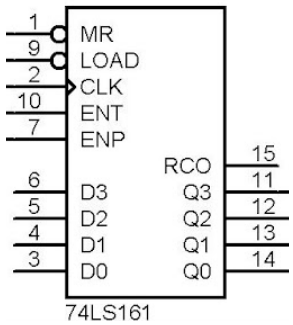
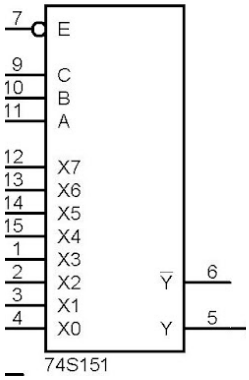
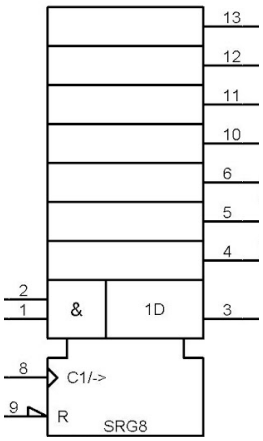
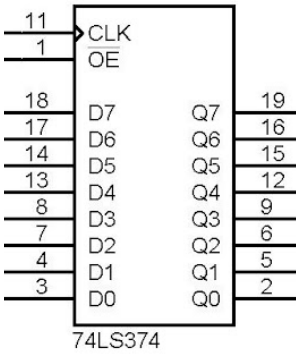
All Circuits for LAB Exam :



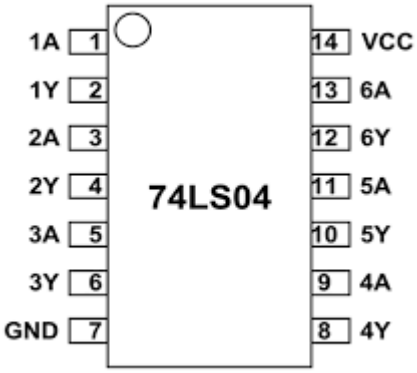




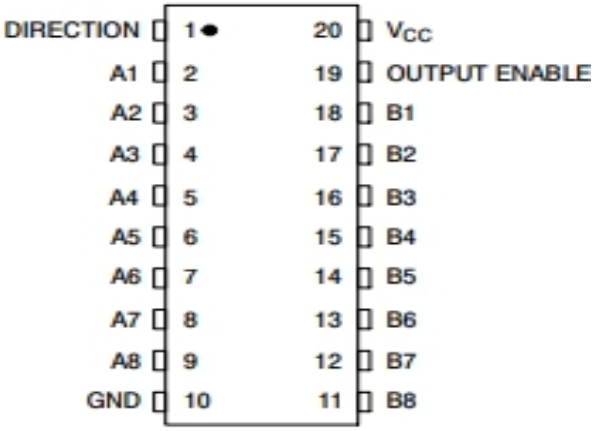
74ls 164

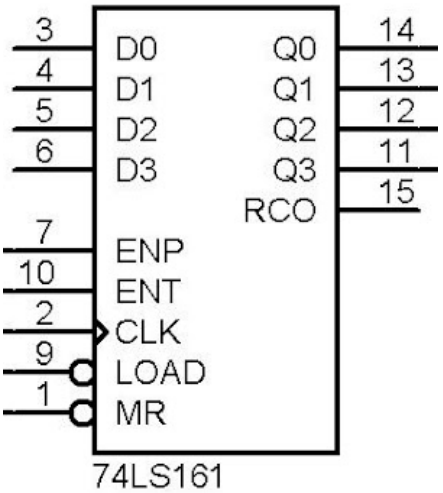


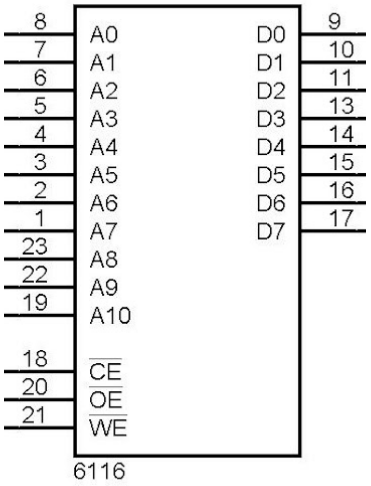
.



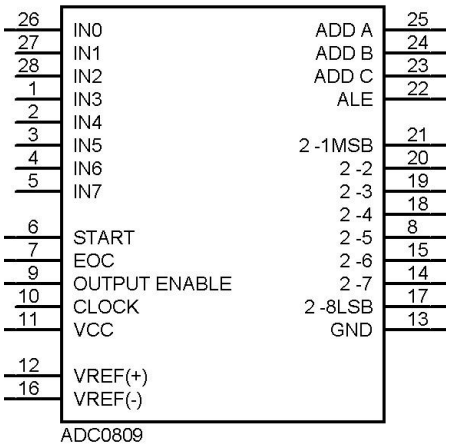
.

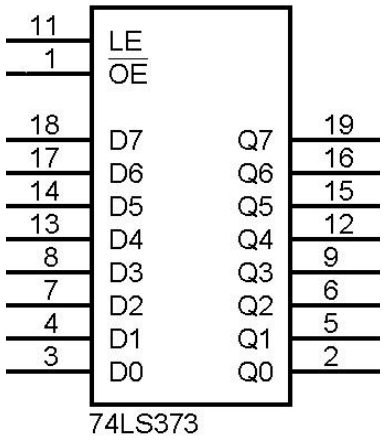


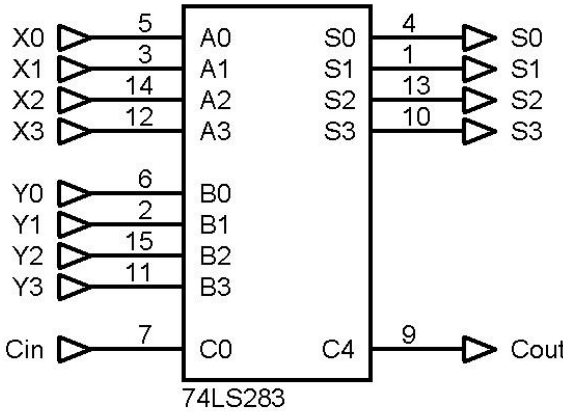




.


26 IN0
27 IN1
28 IN2
1 IN3
2 IN4
3 IN5
4 IN6
5 IN7
6 START
7 EOC
9 OUTPUT ENABLE
10 CLOCK
11 VCC
12 VREF(+)
16 VREF(-)
25 ADD A
24 ADD B
23 ADD C
22 ALE
21 2 -1MSB
20 2 -2
19 2 -3
18 2 -4
8 2 -5
15 2 -6
14 2 -7
17 2 -8LSB
13 GND
ADC0809


11
1
LE
OE
18 D7
17 D6
14 D5
13 D4
8 D3
7 D2
4 D1
3 D0
Q7 19
Q6 16
Q5 15
Q4 12
Q3 9
Q2 6
Q1 5
Q0 2
74LS373


X0 5
X1 3
X2 14
X3 12
A0
A1
A2
A3
Y0 6
Y1 2
Y2 15
Y3 11
B0
B1
B2
B3
Cin 7
C0
S0 4
S1 1
S2 13
S3 10
C4 9
S0
S1
S2
S3
Cout
74LS283