

Name of the experiment: Synchronous data transfer.

Objective: To design and implement a digital circuit to transfer data serially.

Apparatus:

| Sl. No. | Component | Specification | QTY. |
|---------|----------------------|---------------|------|
| 1 | 4-bit counter | 74LS161 | 1 |
| 2 | 8-input Multiplexer | 74LS151 | 1 |
| 3 | 8-bit Shift Register | 74LS164 | 1 |
| 4 | D Flip-Flop | 74LS373 | 1 |
| 5 | Not Gate | 74LS04 | 1 |
| 6 | Digital IC Trainer | - | 1 |
| 7 | Patch Cords | - | 50 |
| 8 | LED | - | 1 |
| 9 | Resistor | - | 1 |

Detail design methodology:

1. At first, we implemented the counter to count from 0 to 7. The 4th bit of the counter output was connected to the Master Reset pin of the counter through a inverter.
2. The 3 output lines of the counter was connected to the Multiplexer as select lines.

The input of the Multiplexer was given from the data switches.

3. The only output of the Multiplexer was connected to the input of the serial in parallel out shift register. The shift register was clocked by the same clock signal of the counter but invertedly.

4. The outputs of the shift register were connected to the inputs of the D FF. The D FF was clocked by the 4th bit of the counter output to stabilize the output.

Finally, the output lines were connected to the LEDs in reverse order.

5. Additionally, a LED was connected to the output of the multiplexer to confirm the serial data transfer.

Circuit Diagram:

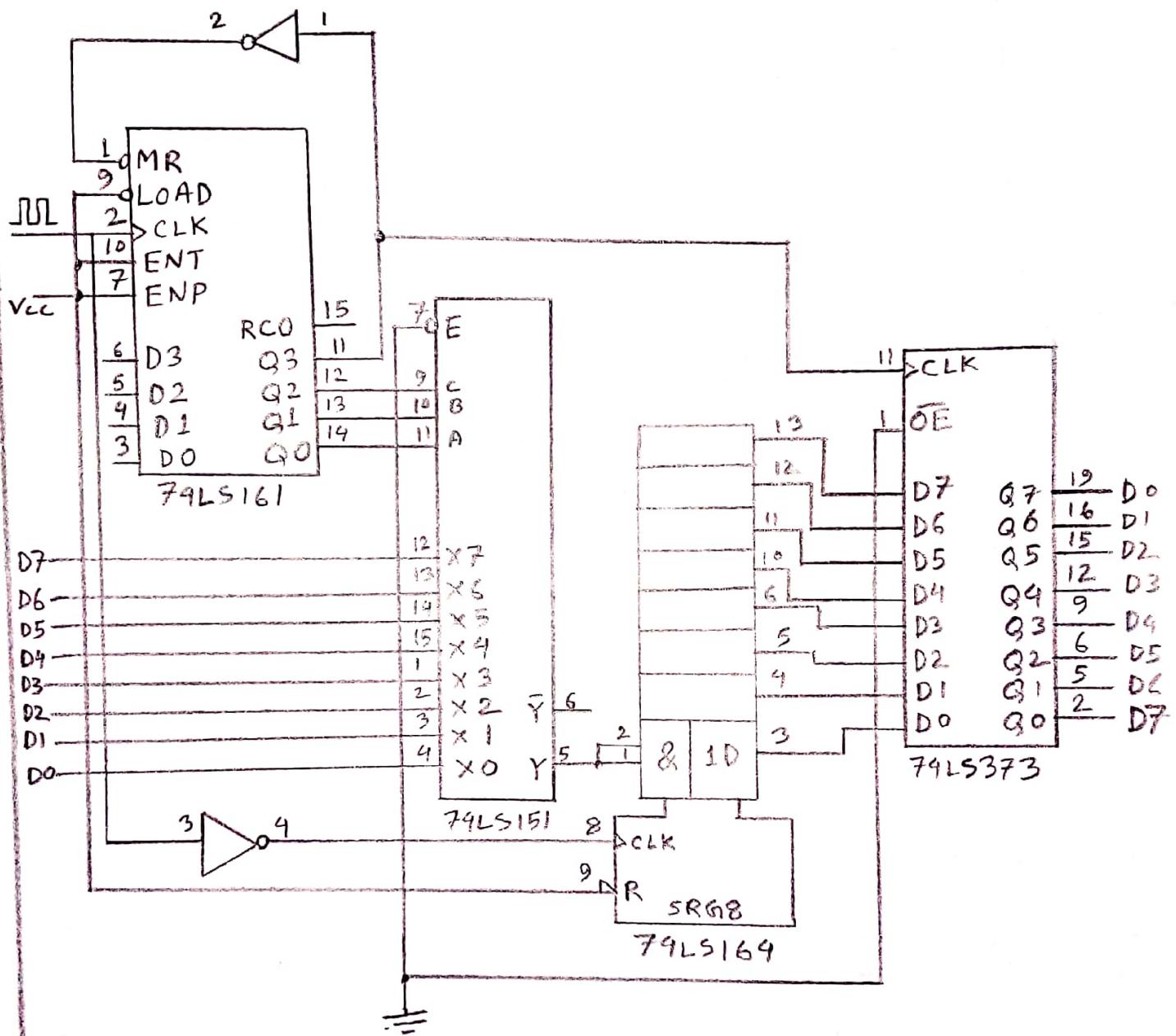


Figure: Digital Circuit for
Synchronous Data Transfer

Experimental data:

| Input | | | | | | | | Output | | | | | | | |
|-------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Result and Discussion: After implementing the circuit, it was tested for several random inputs. For 8-bit inputs, the outputs are listed in the previous table. The table shows that, the output was same as the input. That implies, the circuit was implemented correctly and it was working properly.

Precautions:

1. All ICs were checked before implementation.
2. At each stage, the output was checked if it was working properly or not.
3. Power connection was turned off during any circuit change.
4. Patch cords were connected properly.

Name of the experiment: Memory operations.

Objective: To design and implement a digital circuit to perform memory write and read.

Apparatus:

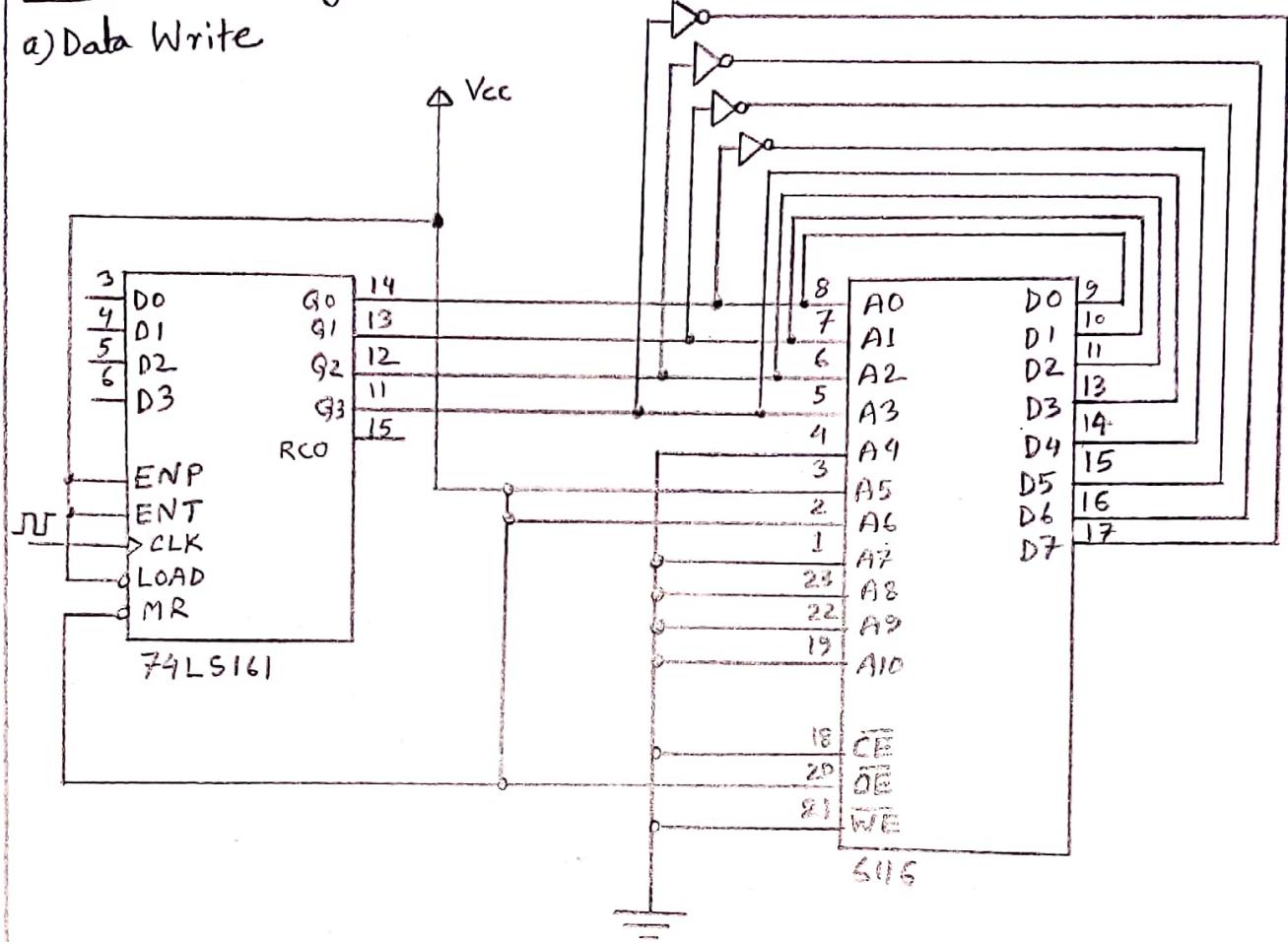
| Sl. No. | Component | Specification | QTY. |
|---------|--------------------|---------------|------|
| 1 | 4-bit counter | 74LS161 | 1 |
| 2 | Static RAM | 6116 | 1 |
| 3 | Not Gate | 74LS04 | 1 |
| 4 | Patch Cords | - | 40 |
| 5 | Digital IC Trainer | - | 1 |

Truth Table:

| Address | Data |
|---------|------|
| 60 | F0 |
| 61 | E1 |
| 62 | D2 |
| 63 | C3 |
| 64 | B4 |
| 65 | A5 |
| 66 | 96 |
| 67 | 87 |
| 68 | 78 |
| 69 | 69 |
| 6A | 5A |
| 6B | 4B |
| 6C | 3C |
| 6D | 2D |
| 6E | 1E |
| 6F | 0F |

Circuit Diagram:

a) Data Write



b) Data Read

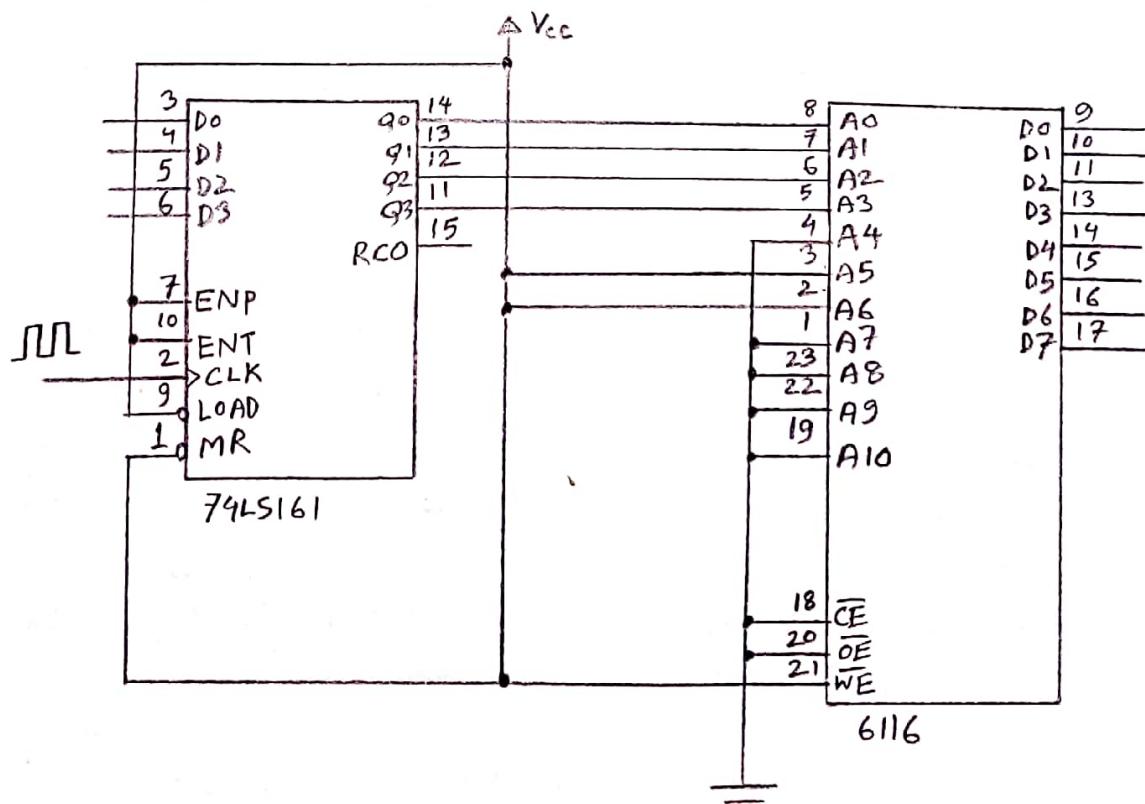


Fig: Circuit for memory write and read

This data is valid for Group - 4 only

Experimental Data:

| Address | Data |
|---------|------|
| 60 | 70 |
| 61 | 61 |
| 62 | 52 |
| 63 | 43 |
| 64 | 34 |
| 65 | 25 |
| 66 | 16 |
| 67 | 07 |
| 68 | 78 |
| 69 | 69 |
| 5A | 5A |
| 6B | 4B |
| 6C | 3C |
| 6D | 2D |
| 6E | 1E |
| 6F | 0F |

Result and Discussion: After implementing the circuit, it was tested several times. First time the write and read operation was performed successfully. We got the same output as shown in the truth table. But after that, there was an error. The most significant bit was not responding for the data output. The bit was always '0' because we are not getting any output at the LED. The resulting output data is listed in the experimental data table.

This error may be occurred due to improper connection of patch cords or any hardware problem in static ram.

Precaution:

1. All ICs were checked before implementation.
2. Output was checked several times.
3. Patch cords were connected properly.

Name of the experiment: Frequency counter.

Objective: To design and implement a frequency counter.

Apparatus:

| Sl. No. | Component | Specification | QTY. |
|---------|----------------------|---------------|------|
| 1 | 4-bit binary counter | 74LS161 | 1 |
| 2 | 3 to 8 line decoder | 74LS138 | 2 |
| 3 | BCD counter | 74LS192 | 1 |
| 4 | D Flip-Flop | 74LS377 | 1 |
| 5 | JK Flip-Flop | 74LS73 | 1 |
| 6 | 2-input AND gate | 74LS08 | 1 |
| 7 | Patch cords | - | 50 |
| 8 | Function Generator | - | 1 |
| 9 | Digital IC Trainer | - | 1 |

Truth Table:

| Input frequency (Hz) | Divisor N | Output | | | | Decimal representation |
|----------------------|-----------|----------------|----------------|----------------|----------------|------------------------|
| | | Q ₃ | Q ₂ | Q ₁ | Q ₀ | |
| 10 | 10 | 0 | 0 | 0 | 1 | 1 |
| 15 | 10 | 0 | 0 | 0 | 1 | 1 |
| 20 | 10 | 0 | 0 | 1 | 0 | 2 |
| 20 | 6 | 0 | 0 | 1 | 1 | 3 |
| 20 | 5 | 0 | 1 | 0 | 0 | 4 |
| 40 | 10 | 0 | 1 | 0 | 0 | 4 |
| 50 | 10 | 0 | 1 | 0 | 1 | 5 |
| 50 | 8 | 0 | 1 | 1 | 0 | 6 |
| 90 | 14 | 0 | 1 | 1 | 0 | 6 |
| 125 | 13 | 1 | 0 | 0 | 1 | 9 |
| 195 | 15 | 1 | 0 | 0 | 1 | 9 |
| 130 | 19 | 1 | 0 | 0 | 1 | 9 |
| 130 | 15 | 1 | 0 | 0 | 0 | 8 |

Circuit Diagram:

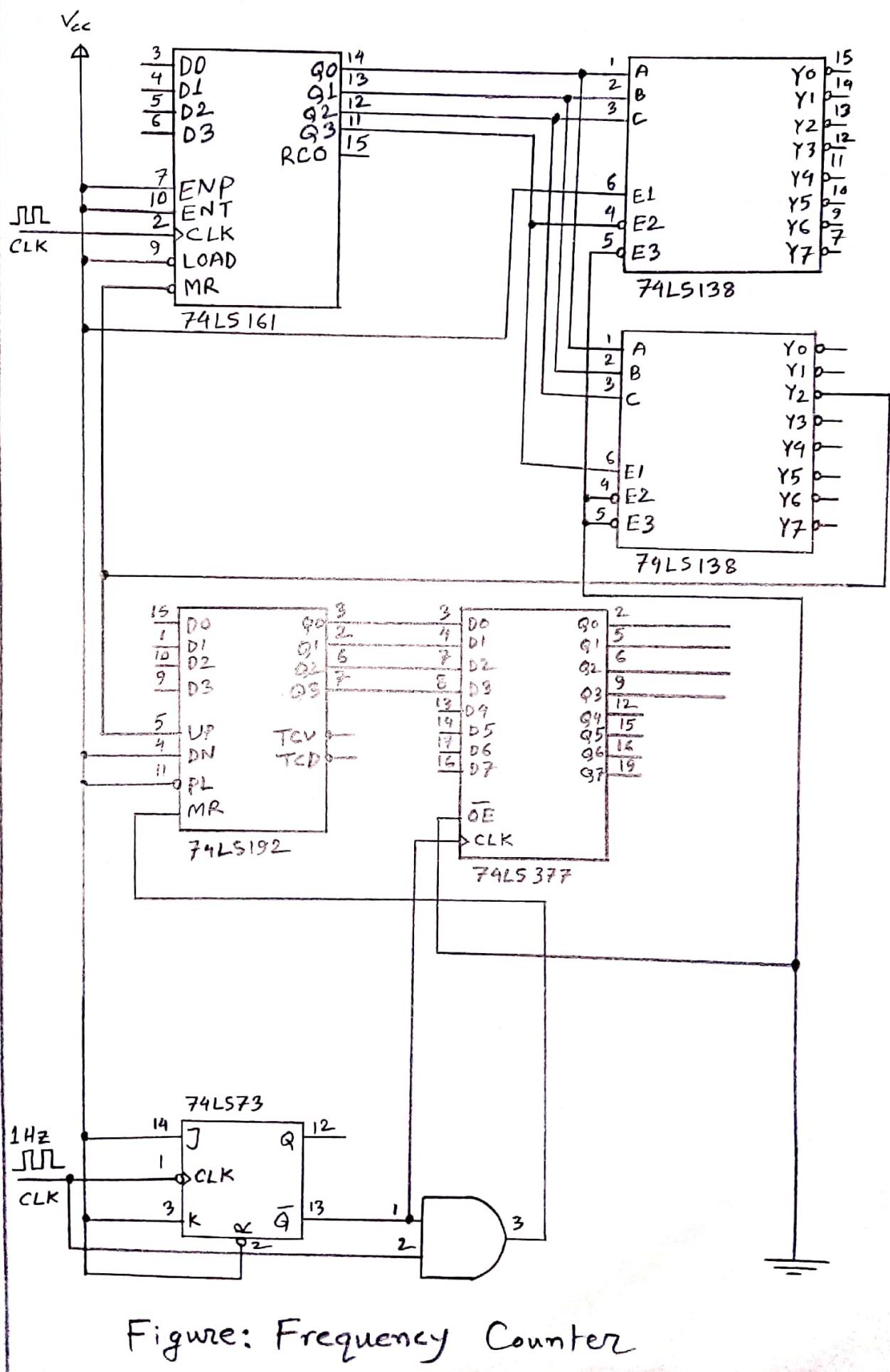


Figure: Frequency Counter

Experimental Data:

| Input frequency (Hz) | Divisor N | Output | | | | Decimal representation |
|----------------------|-----------|----------------|----------------|----------------|----------------|------------------------|
| | | Q ₃ | Q ₂ | Q ₁ | Q ₀ | |
| 10 | 10 | 0 | 0 | 0,1 | 1,0 | 1,2 |
| 15 | 10 | 0 | 0 | 0,1 | 1,0 | 1,2 |
| 20 | 10 | 0 | 0 | 1 | 0,1 | 2,3 |
| 20 | 6 | 0 | 0,1 | 1,0 | 1,0 | 3,4 |
| 20 | 5 | 0 | 1 | 0 | 0,1 | 4,5 |
| 40 | 10 | 0 | 1 | 0 | 0,1 | 4,5 |
| 50 | 10 | 0 | 1 | 0,1 | 1,0 | 5,6 |
| 50 | 8 | 0 | 1 | 1 | 0,1 | 6,7 |
| 90 | 14 | 0 | 1 | 1 | 0,1 | 6,7 |
| 125 | 13 | 1 | 0 | 0 | 0,1 | 8,9 |
| 145 | 15 | 1 | 0 | 0 | 0,1 | 8,9 |
| 130 | 14 | 1 | 0 | 0 | 0,1 | 8,9 |
| 130 | 15 | 1 | 0 | 0 | 0,1 | 8,9 |

Result and Discussion: After implementing the circuit, it was tested for several input frequencies and constant divisors. The output of the circuit is provided in the experimental data table. There is a difference between the theoretical data and experimental data. The output was switching between two consecutive numbers. This error occurred due to the 1 Hz clock frequency. It was tough to provide exactly 1 Hz clock frequency. As the difference was not more than unity, the circuit was working properly.

Precaution:

1. All ICs were checked before using.
2. Patch cords were connected properly.
3. Clock frequency was provided from function generator.
4. Circuit was turned off, when any circuit change needed.

Name of experiment: Arithmetic circuit control design.

Objective: To design and implement arithmetic circuits with selection variable S_0 and S_1 , and operand A (4 bits), B (4 bits) and C_{in} that generates the following operations.

| S_0 | S_1 | $C_{in}=0$ | $C_{in}=1$ |
|-------|-------|------------|------------|
| 0 | 0 | $F=A+B$ | $F=A+B+1$ |
| 0 | 1 | $F=A$ | $F=A+1$ |
| 1 | 0 | $F=B'$ | $F=B'+1$ |
| 1 | 1 | $F=A+B'$ | $F=A+B'+1$ |

Apparatus:

| Sl. No. | Component | Specification | QTY. |
|---------|--------------------|---------------|------|
| 1 | 4-bit Full Adder | 74LS283 | 1 |
| 2 | AND Gate | 74LS08 | 2 |
| 3 | OR Gate | 74LS32 | 2 |
| 4 | NOT Gate | 74LS09 | 2 |
| 5 | XOR Gate | 74LS86 | 1 |
| 6 | Digital IC Trainer | - | 1 |
| 7 | Patch chords | - | 50 |

Truth table:

| Input | | | | Output | |
|-------|-------|-------|-------|--------|-------|
| S_0 | S_1 | A_i | B_i | X_i | Y_i |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

K-Map:

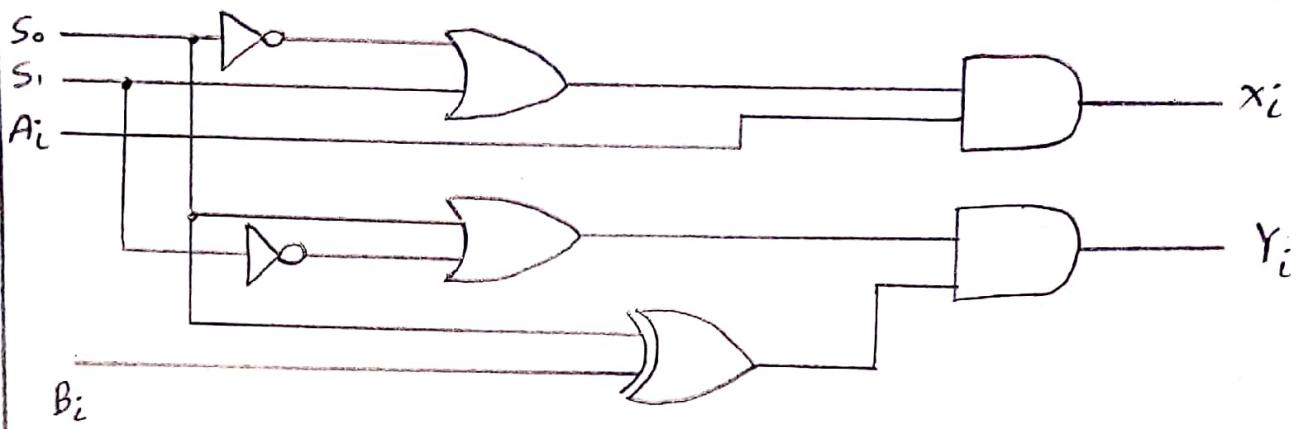
| X_i | $\bar{S}_0\bar{S}_1$ | \bar{S}_0S_1 | $S_0\bar{S}_1$ | S_0S_1 |
|----------------------|----------------------|----------------|----------------|----------|
| $\bar{A}_i\bar{B}_i$ | 0 | 0 | 0 | 0 |
| \bar{A}_iB_i | 0 | 0 | 0 | 0 |
| $A_i\bar{B}_i$ | 1 | 1 | 1 | 0 |
| A_iB_i | 1 | 1 | 1 | 0 |

$$X_i = (\bar{S}_0 + S_1) A_i$$

| $\bar{A}_i\bar{B}_i$ | 0 | 0 | 1 | 1 |
|----------------------|---|---|---|---|
| \bar{A}_iB_i | 1 | 1 | 0 | 0 |
| $A_i\bar{B}_i$ | 1 | 1 | 0 | 0 |
| $A_i\bar{B}_i$ | 0 | 0 | 1 | 1 |

$$Y_i = (S_0 + \bar{S}_1)(B_i \oplus S_0)$$

Circuit Diagram:



| | | | | | |
|----------|----|----|----|-------|------|
| X_0 | 5 | A0 | 5 | S_0 | 4 |
| X_1 | 3 | A1 | 3 | S_1 | 1 |
| X_2 | 14 | A2 | 14 | S_2 | 13 |
| X_3 | 12 | A3 | 12 | S_3 | 10 |
| y_0 | 6 | B0 | | | |
| y_1 | 2 | B1 | | | |
| y_2 | 15 | B2 | | | |
| y_3 | 11 | B3 | | | |
| C_{in} | 7 | C0 | | C_0 | 9 |
| | | | | | Cout |

74LS283

Figure: Arithmetic Circuit

Experimental data:

| Input | | | | | | | | | | | Output | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----------|-----------|-------|-------|-------|-------|
| S_0 | S_1 | A_3 | A_2 | A_1 | A_0 | B_3 | B_2 | B_1 | B_0 | C_{in} | C_{out} | S_3 | S_2 | S_1 | S_0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |

Result and Discussion: After implementing the circuit for 4 bits, it was tested for all the operations. The outputs are listed in the above table and they are correct. So the circuit was working properly.

Precautions:

1. All ICs were checked before circuit implementation.
2. The circuit was build step by step and checked for output at each step.
3. power connection was turned off during circuit change.
4. Patch chords were connected properly.

Name of experiment: Arithmetic circuit control design.

Objective: To design and implement arithmetic circuits with selection variable S_0 and S_1 , and operand A (4 bits), B (4 bits) and C_{in} that generates the following operations:

| S_0 | S_1 | $C_{in}=0$ | $C_{in}=1$ |
|-------|-------|-----------------|-----------------|
| 0 | 0 | $F = A$ | $F = A + 1$ |
| 0 | 1 | $F = A - B - 1$ | $F = A - B$ |
| 1 | 0 | $F = B - A - 1$ | $F = B - A$ |
| 1 | 1 | $F = A + B$ | $F = A + B + 1$ |

Apparatus:

| Sl. No. | Component | Specification | QTY. |
|---------|--------------------|---------------|------|
| 1 | 4-bit Full Adder | 74LS283 | 1 |
| 2 | AND Gate | 74LS08 | 2 |
| 3 | OR Gate | 74LS32 | 1 |
| 4 | NOT Gate | 74LS04 | 2 |
| 5 | XOR Gate | 74LS86 | 2 |
| 6 | Patch chords | - | 40 |
| 7 | Digital IC Trainer | - | 1 |

Truth Table:

| Input | | | | Output | |
|-------|-------|-------|-------|--------|-------|
| S_0 | S_1 | A_i | B_i | X_i | Y_i |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

K-Map:

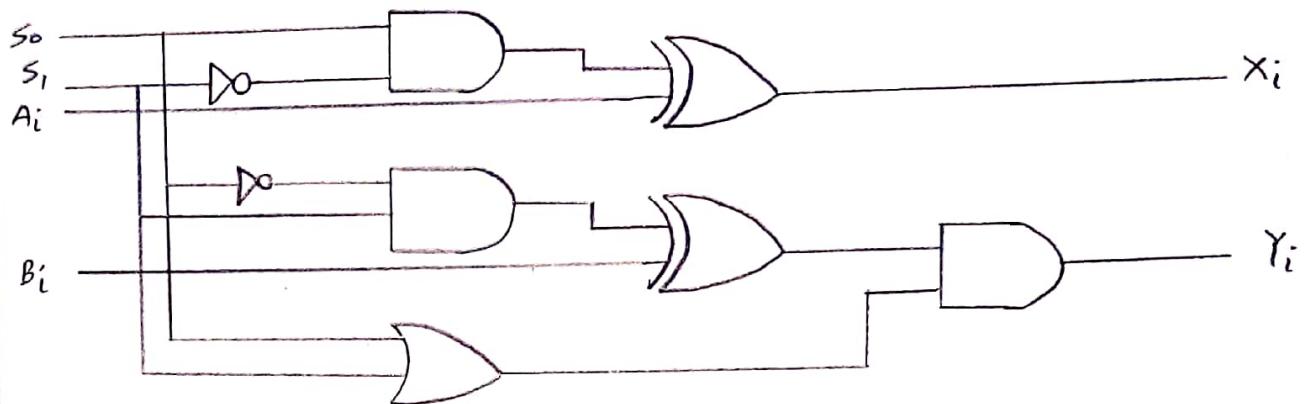
| | | | | |
|----------------------|----------------------|----------------|----------|----------------|
| X_i | $\bar{S}_0\bar{S}_1$ | \bar{S}_0S_1 | S_0S_1 | $S_0\bar{S}_1$ |
| $\bar{A}_i\bar{B}_i$ | 0 | 0 | 0 | 1 |
| \bar{A}_iB_i | 0 | 0 | 0 | 1 |
| $A_i\bar{B}_i$ | 1 | 1 | 1 | 0 |
| A_iB_i | 1 | 1 | 1 | 0 |

$$X_i = S_0\bar{S}_1 \oplus A_i$$

| | | | |
|----------------------|----------------|----------|----------------|
| $\bar{S}_0\bar{S}_1$ | \bar{S}_0S_1 | S_0S_1 | $S_0\bar{S}_1$ |
| $\bar{A}_i\bar{B}_i$ | 0 | 1 | 0 |
| \bar{A}_iB_i | 0 | 0 | 1 |
| $A_i\bar{B}_i$ | 0 | 0 | 1 |
| A_iB_i | 0 | 1 | 0 |

$$Y_i = (S_0 + S_1) (S_0\bar{S}_1 \oplus B_i)$$

Circuit Diagram:



| | | | |
|----------|----|-------|-----------|
| x_0 | 5 | A_0 | 9 |
| x_1 | 3 | A_1 | S_1 |
| x_2 | 14 | A_2 | S_2 |
| x_3 | 12 | A_3 | S_3 |
| y_0 | 6 | B_0 | |
| y_1 | 2 | B_1 | |
| y_2 | 15 | B_2 | |
| y_3 | 11 | B_3 | |
| C_{in} | 7 | C_0 | 9 |
| | | | C_{out} |

Figure: Arithmetic Circuit

Experimental Data:

| Input | | | | | | | | | | | Output | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----|--------|----------------|----------------|----------------|----------------|
| S ₀ | S ₁ | A ₃ | A ₂ | A ₁ | A ₀ | B ₃ | B ₂ | B ₁ | B ₀ | Cin | Cout | S ₃ | S ₂ | S ₁ | S ₀ |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

Result and Discussion: After implementing the circuit for 4 bits, it was tested for all the operations. The outputs are listed in the above table and they are correct. So the circuit was working properly.

Precaution:

1. All ICs were checked before circuit implementation.
2. The circuit was build step by step and checked for output at each stage.
3. Power connection was turned off during circuit change.
4. Patch chords were connected properly.

Name of experiment: Analog to Digital Conversion.

Objective: To design and implement a circuit to convert analog signal (potential difference) into digital data by using an Analog to Digital Converter than store the data in a latch and display the converted digital data using LED.

Apparatus:

| Sl. No. | Component | Specification | QTY. |
|---------|--------------------|---------------|------|
| 1 | A/D Converter | ADC0809 | 1 |
| 2 | D-Latch | 74LS373 | 1 |
| 3 | Patch chords | - | 20 |
| 4 | Digital IC Trainer | - | 1 |

Circuit Diagram:

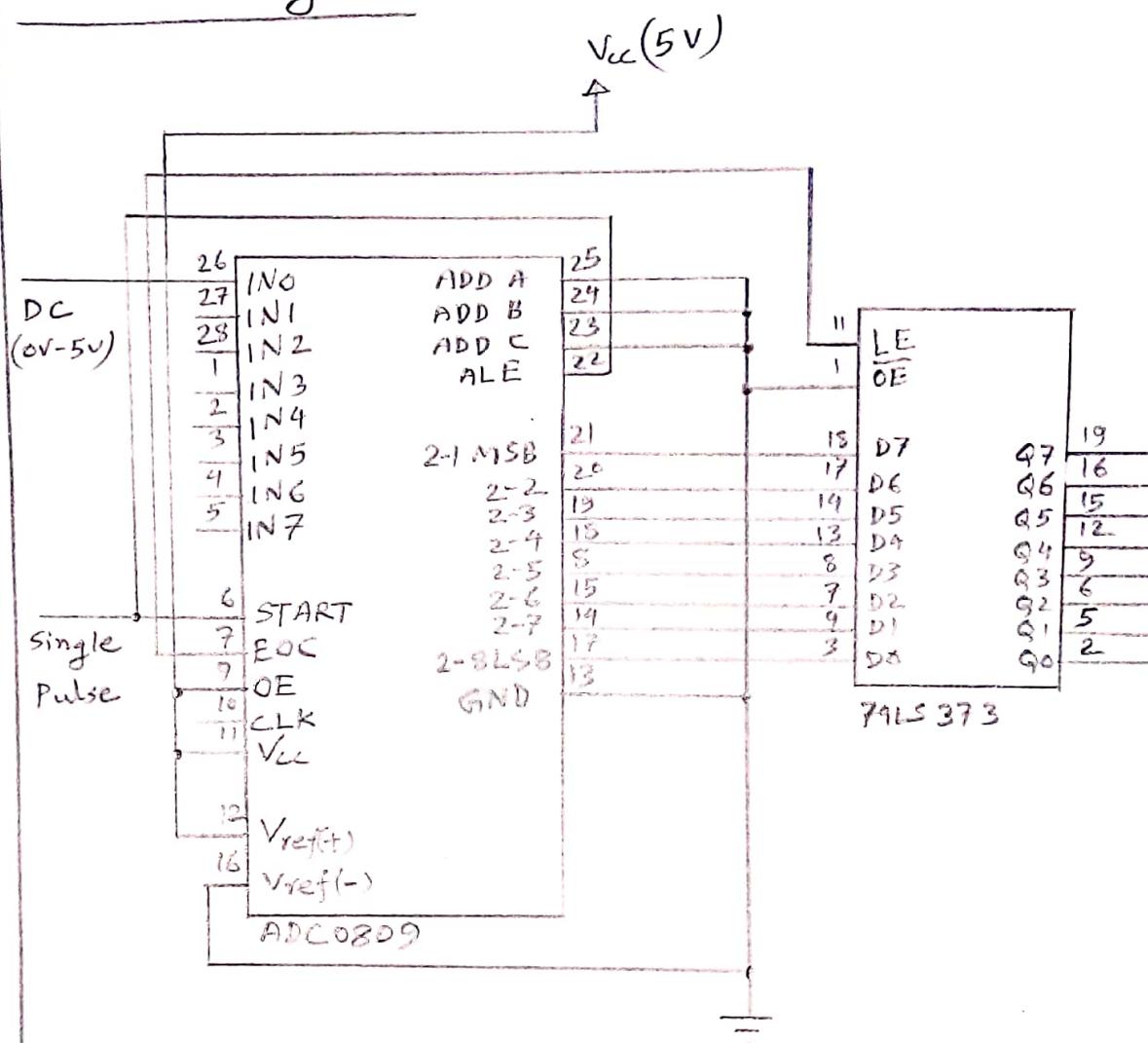


Figure: Analog to Digital Converter

Experimental Data:

| $V_{ref(+)}$ | $V_{ref(-)}$ | Input Voltage (V) | $\frac{V - V_{ref(-)}}{\frac{V_{ref(+)} - V_{ref(-)}}{2^8 - 1}}$ | Output |
|--------------|--------------|-------------------|--|--------|
| 5 | 0 | 1.5 | 76.5 | 78 |
| 5 | 0 | 2 | 102 | 97 |
| 5 | 0 | 2.7 | 137.7 | 135 |
| 5 | 0 | 3.2 | 163.2 | 169 |
| 5 | 0 | 3.9 | 198.9 | 200 |
| 5 | 0 | 4.2 | 214.2 | 210 |
| 5 | 0 | 4.5 | 229.5 | 228 |
| 5 | 0 | 4.8 | 244.8 | 250 |

Result and Discussion: After implementing the circuit it was tested for several input voltage. The calculated and circuit output is listed above. The difference is due to the fluctuation of voltage.

Precaution:

1. All ICs were checked before using.
2. Patch chords were connected properly.
3. Voltage was regulated using a voltage regulator.