2.1.3 Clock Generator

The main task of Clock Generator block is generated clock signals which is needed to audio processing. The Wolfson's Audio Codec needs three four different clock signals named: XCK, BCLK, ADCLRCLK and DACLRCLK. XCK is master clock to Audio Codec, and XCK clock is always enabled. XCK is derived from 50 MHz system clock , dividing it by four. BCLK is derived from XCK, dividing it by 8 and *LRCLK clocks is derived dividing BCLK by 32. The block diagram of Clock Generator is shown in figure 2.7.

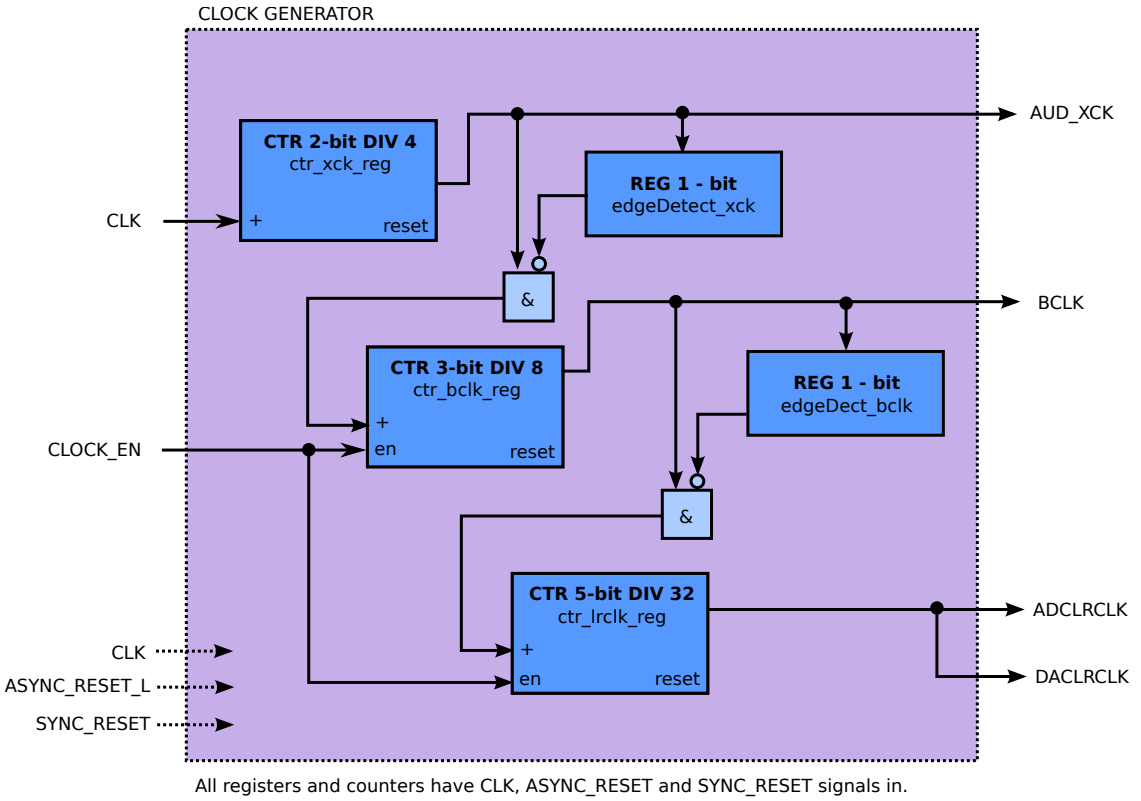

Figure 2.7: The Clock Generator block diagram

BCLK clock is bit clock which is needed to synchronize serial bit transmission from Audio Codec to Audio Interface and from Audio Interface to Audio Codec. BCLK signal goes through the Audio Interface module to the Audio Codec. ADCLRCLK clock needed to synchronize left and right channel ADC data transmission from the Audio Codec to the Audio Interface. DACLRCLK clock is needed to synchronize left and right channel DAC data from the Audio Interface to the Audio Codec. When ADC/DACLRCLK is logical one, it means that left channel data is transmitted and case of logical zero, right channel data is transmitted. Both of clocks goes trough the Audio Interface to Audio Codec. BCLK, ADCLRCLK and DACLRCLK is only enabled when CLOCK_EN is set, so in other words always when audio processing is going on (the Control Unit's START_DSP signal is logical one).

2.1.4 Audio Interface

The Audio Interface is used to receive ADC audio data from The Audio Codec (input signal AUD_ADC_DAT) and transmit DAC data (processed by Audio DSP) to the Audio Codec (output signal AUD_DAC_DAT). Transmitting and receiving is synchronized by using BCLK, ADCLRCLK and DACLRCLK clock signals. The block diagram of the Audio Interface is shown in figure 2.1.4.

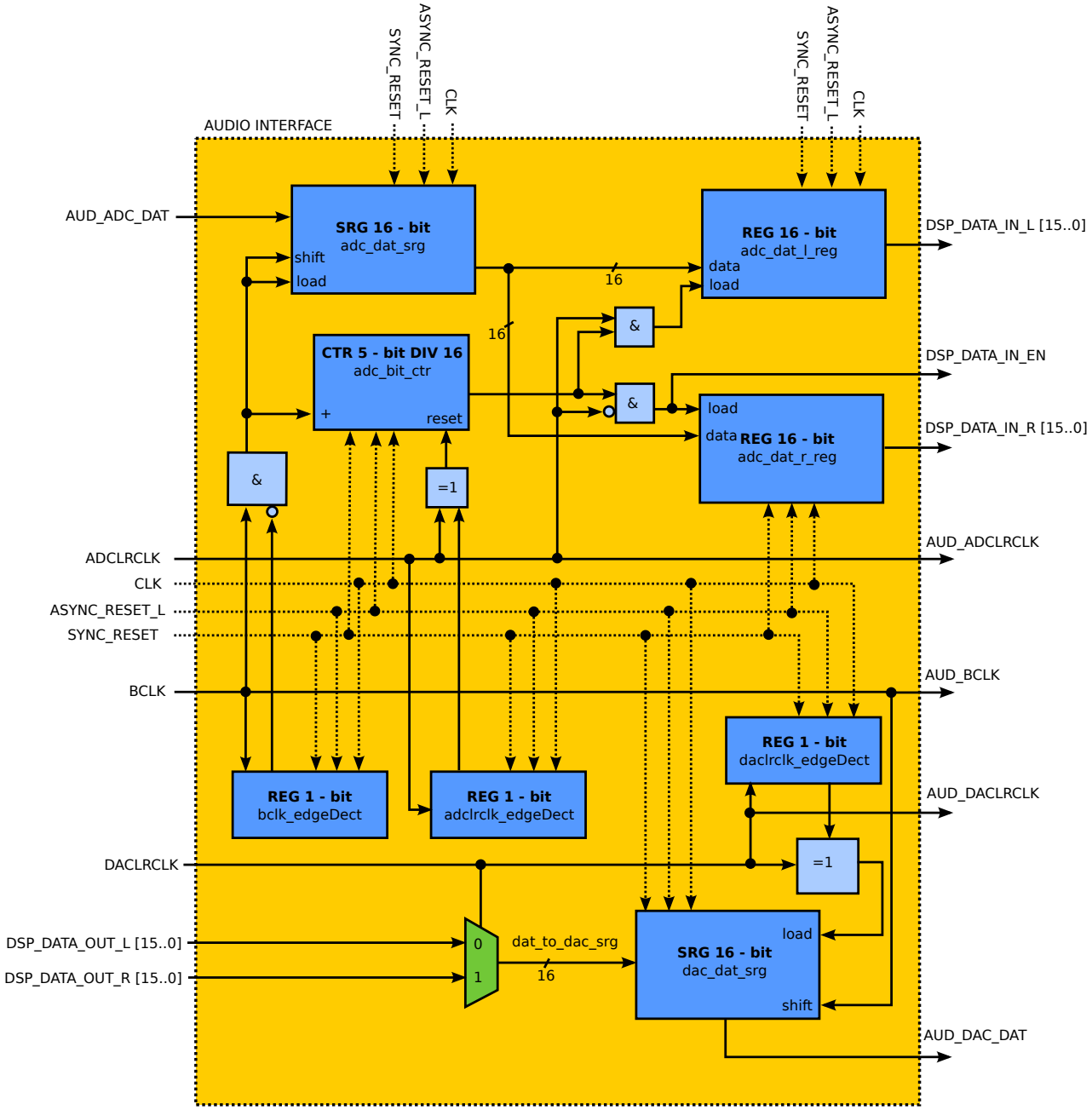

Figure 2.8: The Audio Interface block diagram

Received ADC data is in serial format so data is transformed to parallel format before data is passed to Audio DSP (signals DSP_DATA_IN_L and DSP_DATA_IN_R). The Audio Interface get processed DAC data from the Audio DSP (signals DSP_DATA_OUT_L and DSP_DATA_OUT_R) in parallel format and transform it to serial format for transmission to the Audio Codec. The Audio Interface report to the Audio DSP when parallel ADC data is ready to load, using DSP_DATA_IN_EN signal. The DACLRCLK and the ADCLRCLK clock signals defines which audio channel data is transmitted and received.