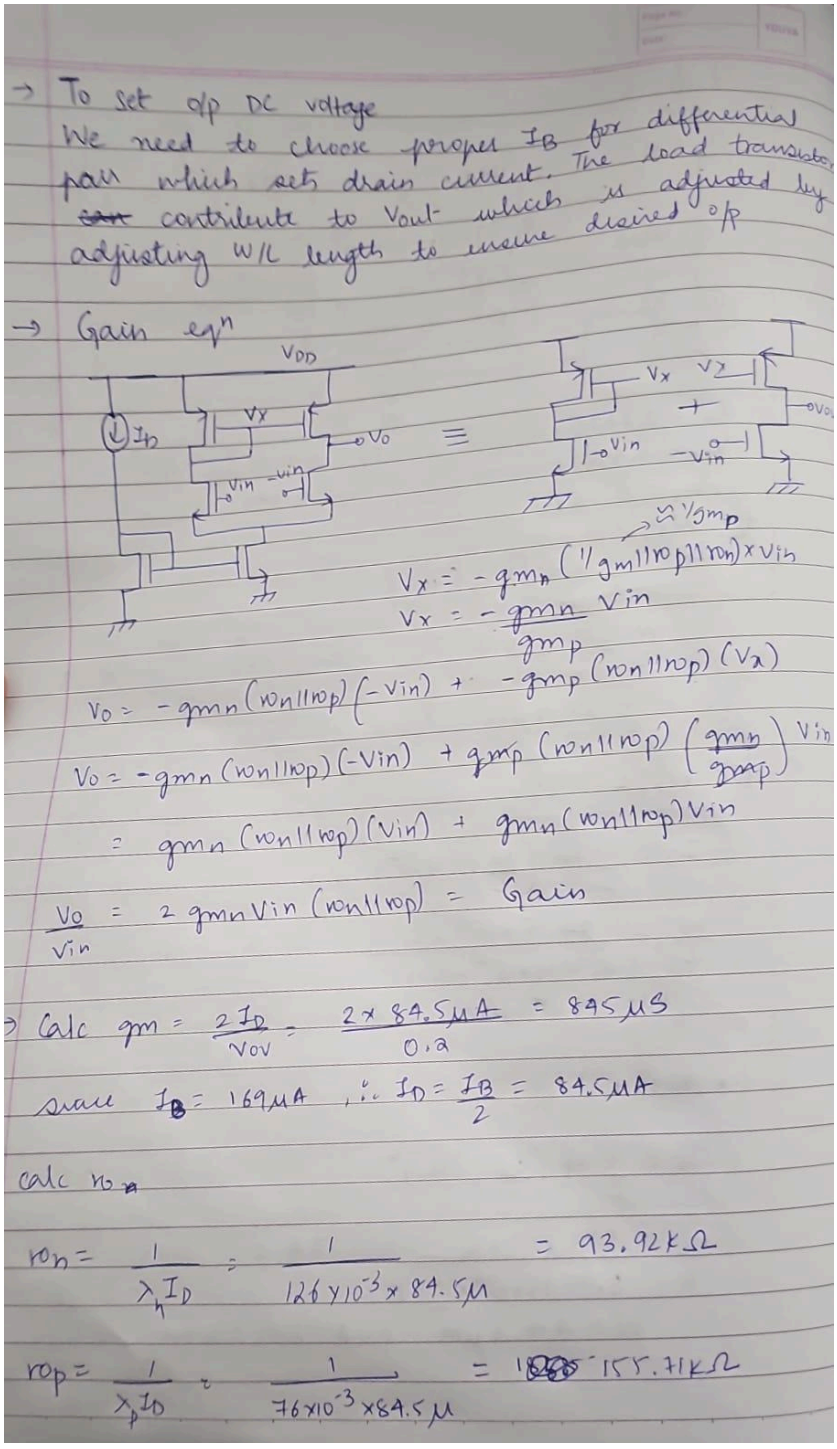
EEE 591:Analog Integrated Circuits
Differential amplifier with active load

Hand calculations



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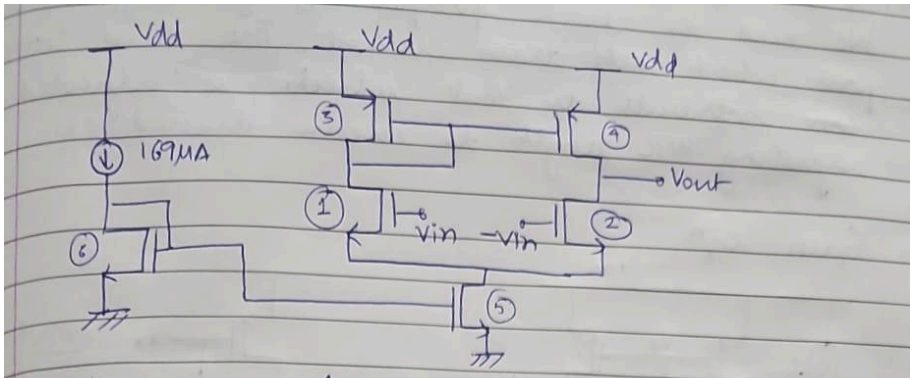

$k_n' = 2.7475 \times 10^{-4} A/V^2$ $\quad K_p' = 0.9575 \times 10^{-4} A/V^2$

$V_{tn} = 0.49V$ $\quad V_{tp} = 0.54V$

$V_{ov} = 0.15V$

for $W_{5,6}$

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{ov})^2$$

$$\therefore \frac{W}{L} = \frac{I_D \times 2}{k_n' \times V_{ov}^2} = \frac{169 \times 10^{-6} \times 2}{2.7475 \times 10^{-4} \times (0.15)^2} = 51.8$$

$\therefore W = 30.9 \mu m$ and $L = 600nm$

for $W_{1,2}$

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{ov})^2$$

$$\frac{W}{L} = \frac{84.5 \times 10^{-6} \times 2}{2.7475 \times 10^{-4} \times (0.15)^2} = 25.9$$

$\therefore W = 15.56 \mu m$ and $L = 600nm$

for $W_{3,4}$

$$I_D = \frac{1}{2} k_p \left(\frac{W}{L}\right) (V_{ov})^2$$

$$\frac{W}{L} = \frac{84.5 \times 10^{-6} \times 2}{0.9575 \times 10^{-4} \times (0.15)^2} = 74.4$$

$\therefore W = 44.6 \mu m$ and $L = 600nm$

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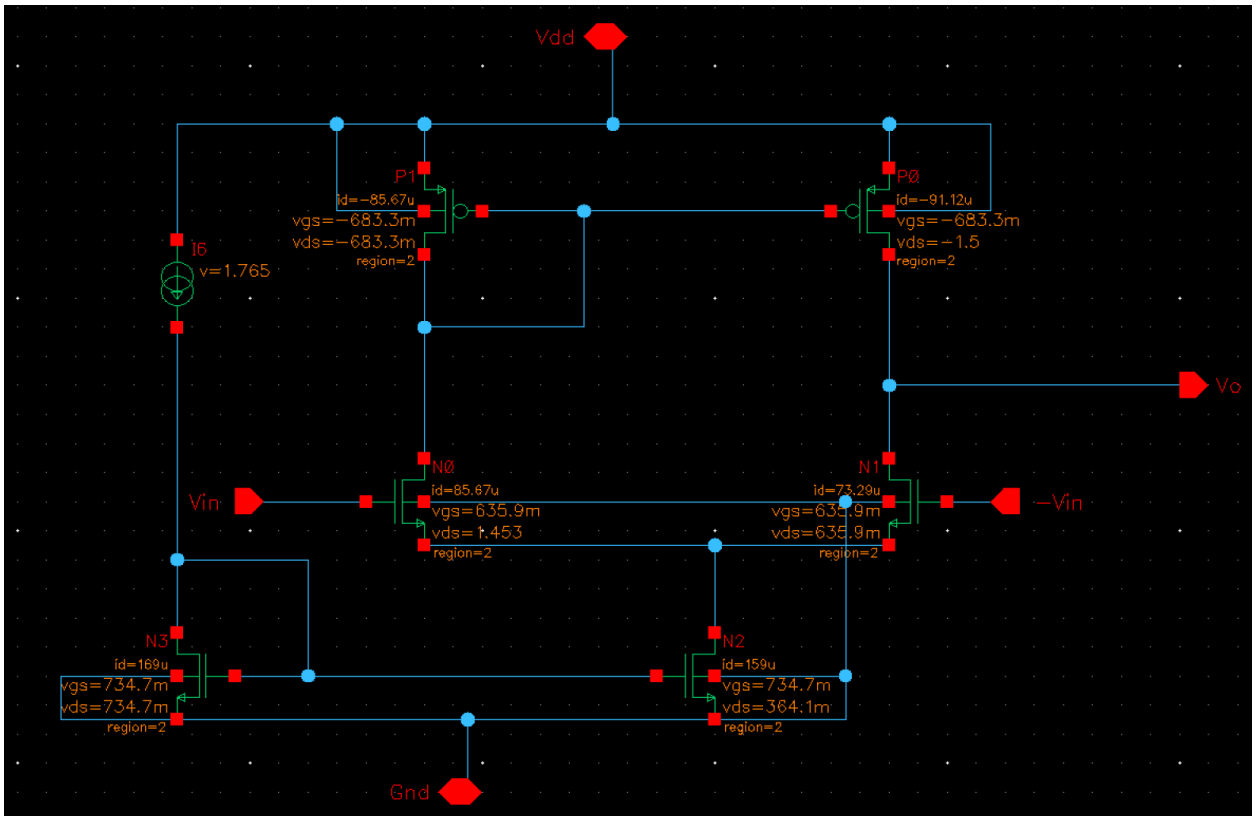
The schematic diagram:



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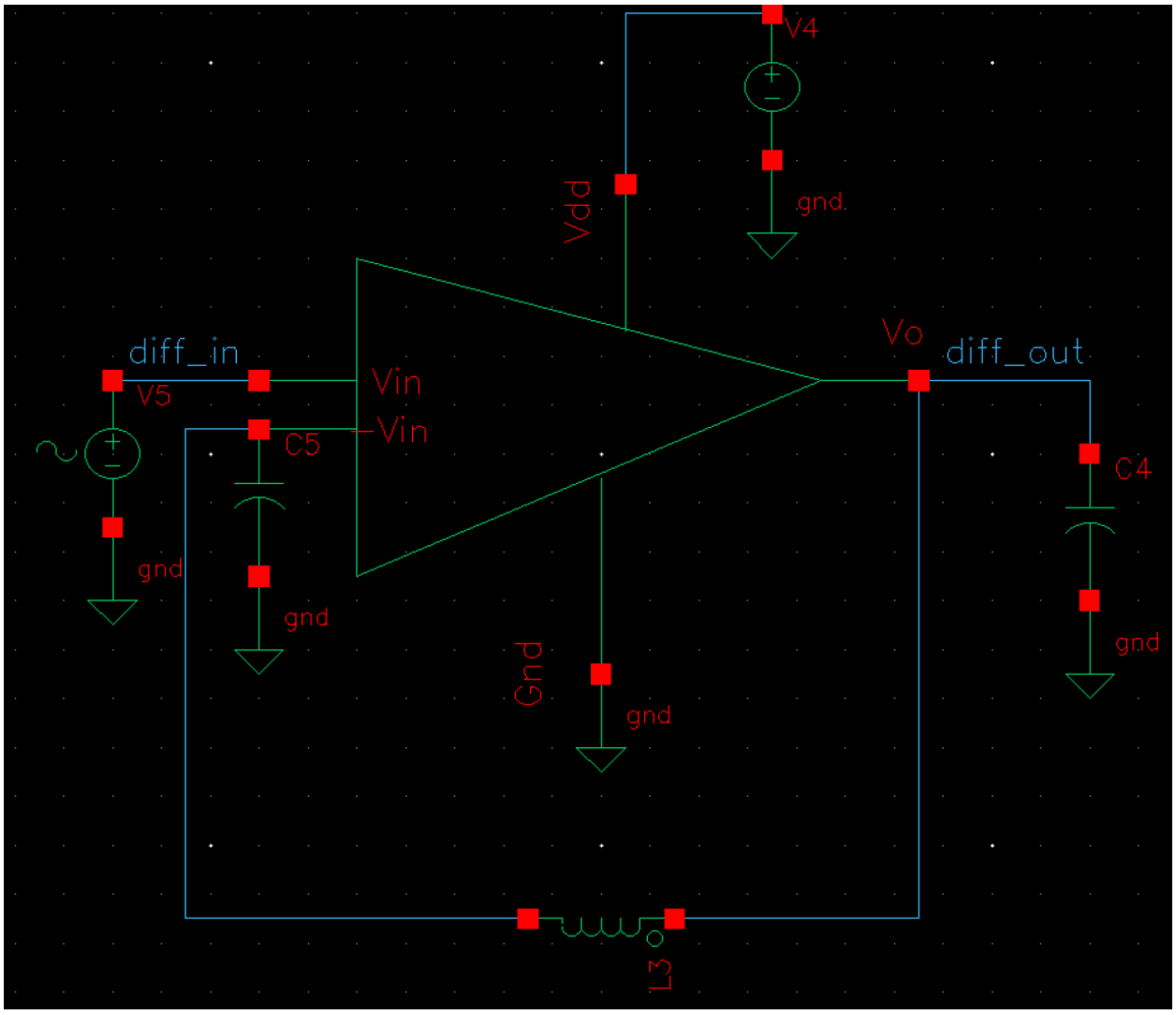
Differential Amplifier:



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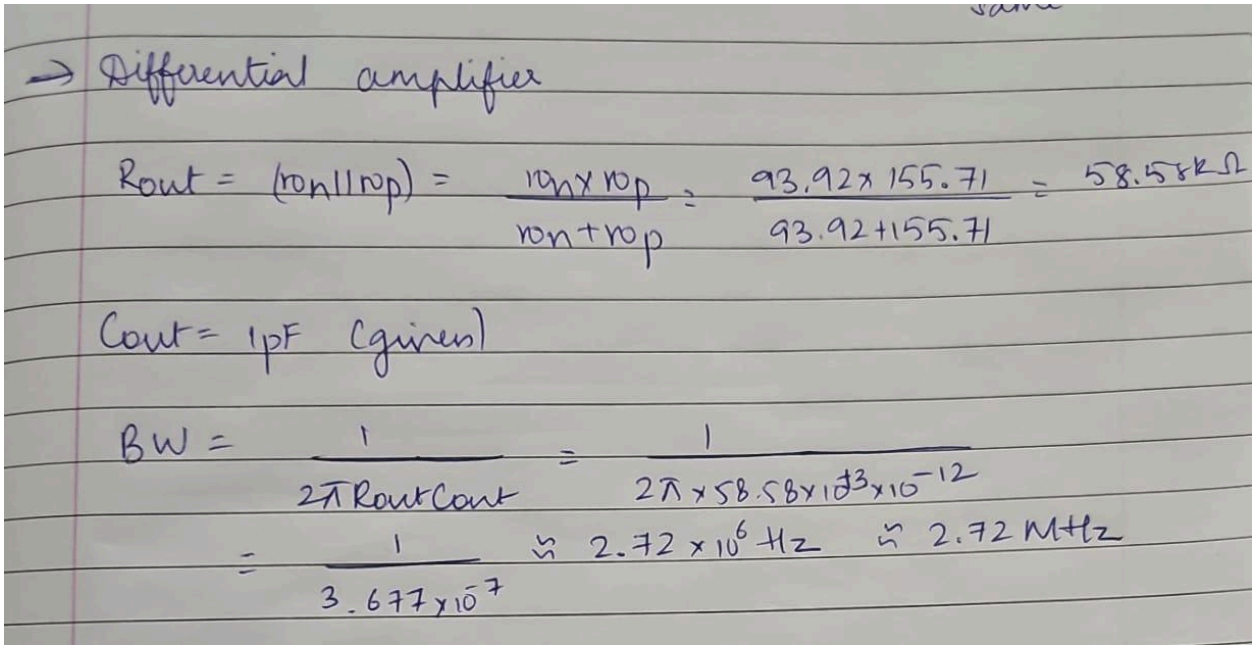
Bandwidth calc



Gain and Phase vs Frequency

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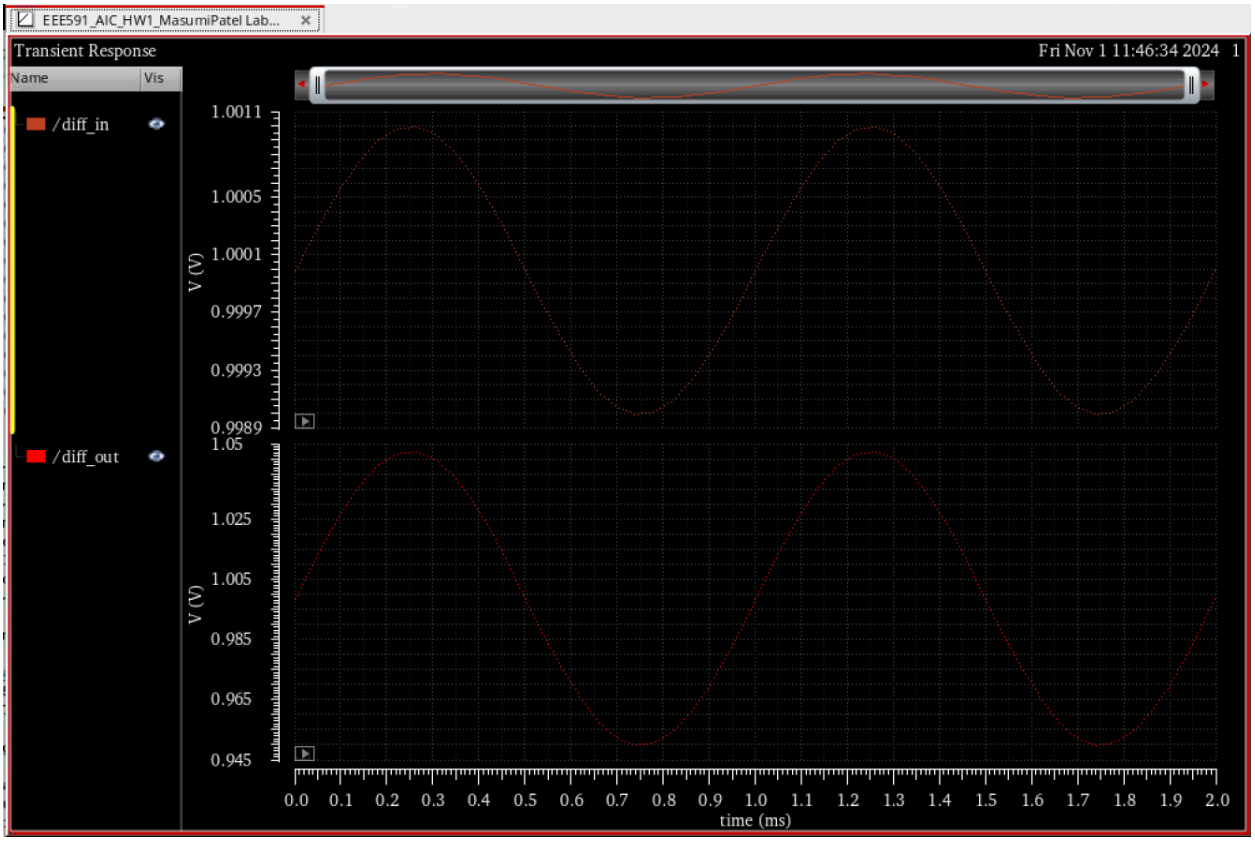
Transient response for 1mV amplitude



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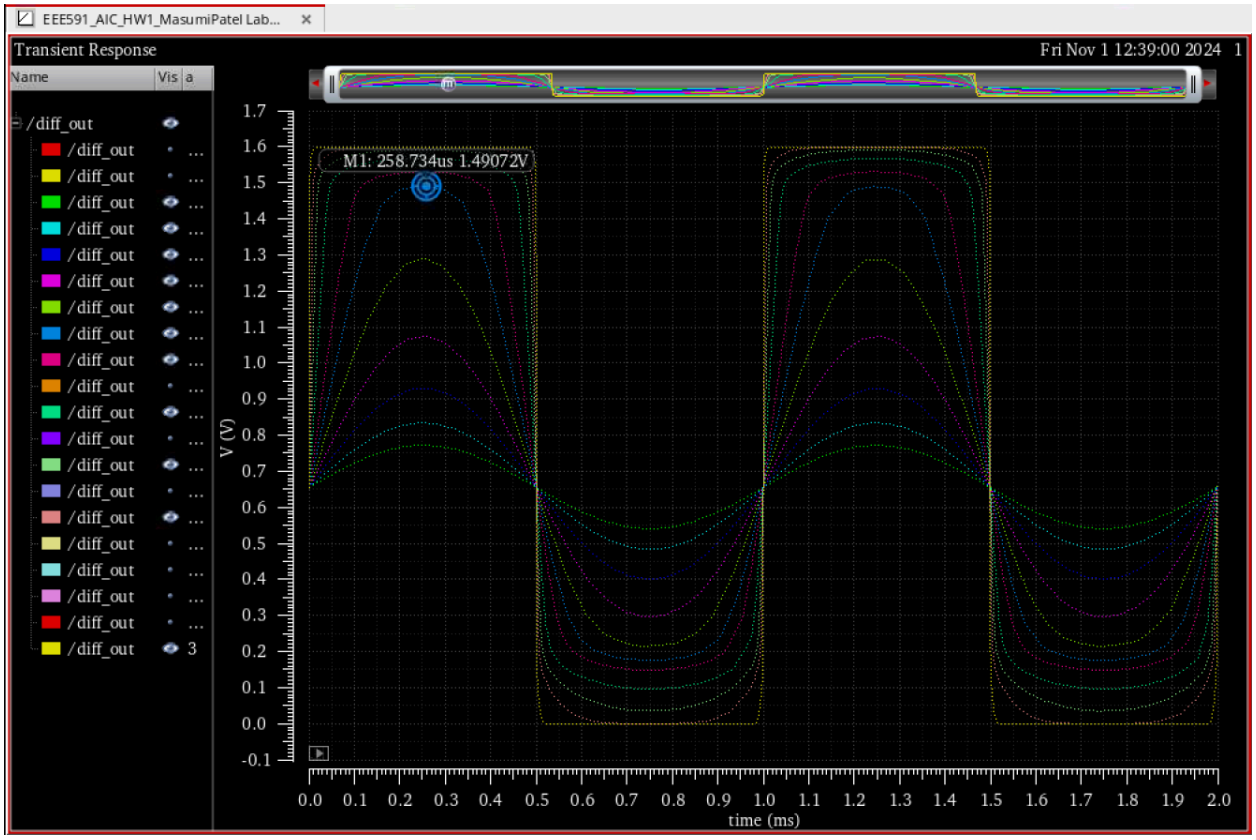
The output starts clipping when **Vswing>1.29072V**



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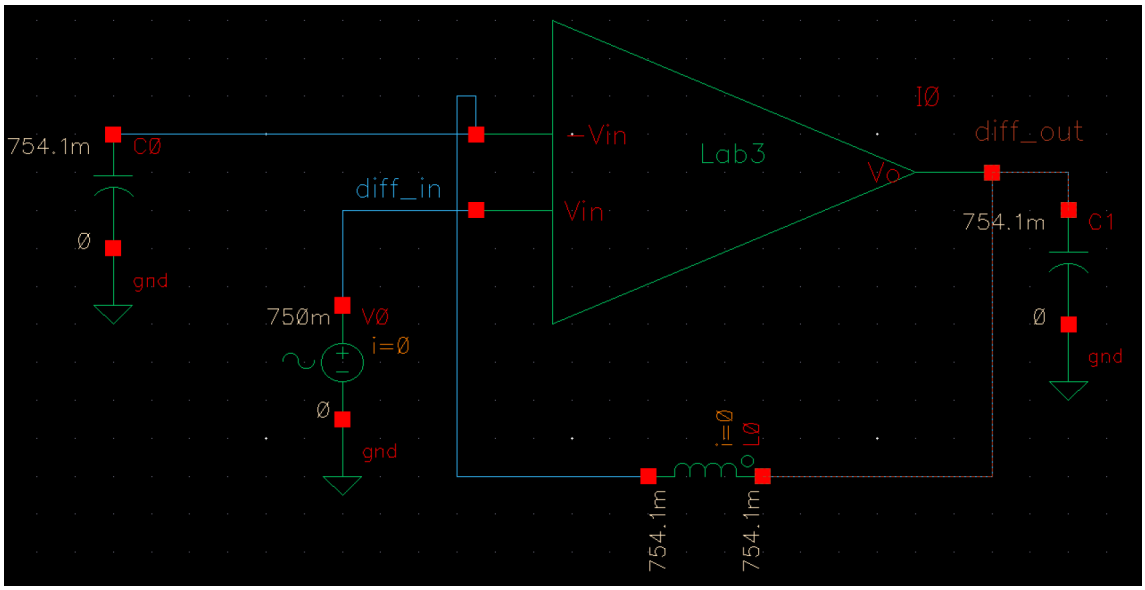
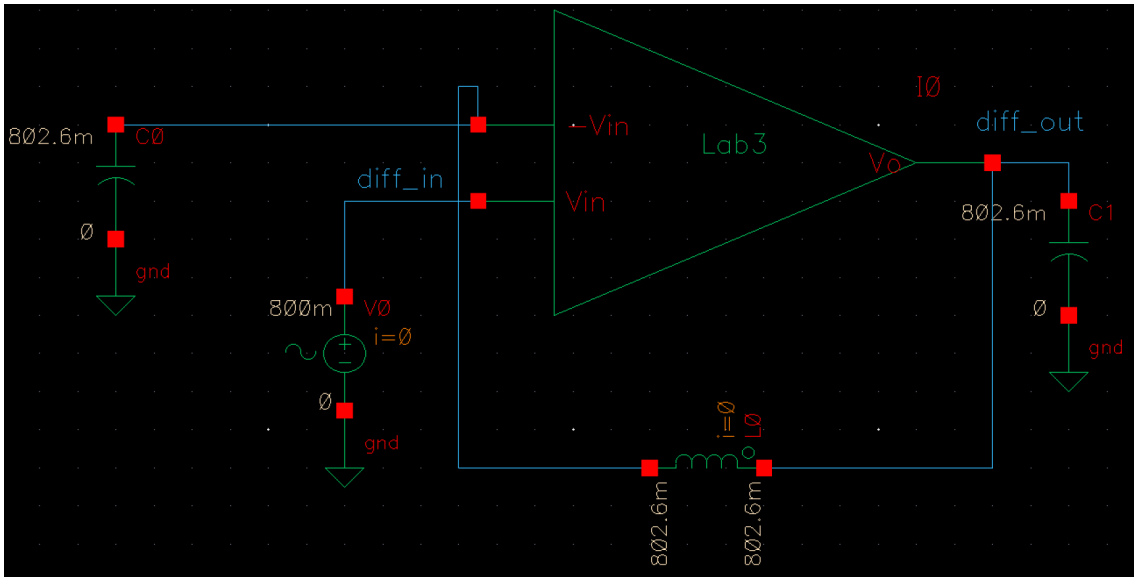
Before offset was applied



After 5mv DC offset was applied



We observe that change in DC input offset even by slight margins leads to change in DC output voltage

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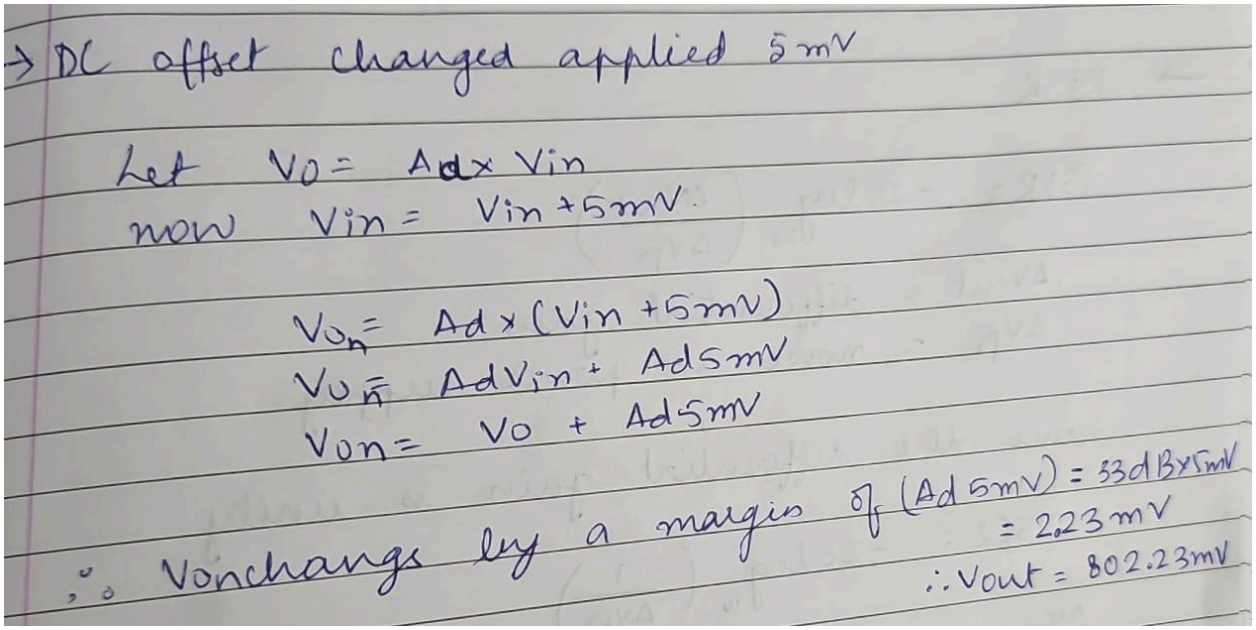

The simulation results for the differential amplifier revealed that the gain remained stable at low frequencies, as expected, before rolling off due to parasitic capacitance, with the -3 dB bandwidth aligning closely with our calculated estimates using Bandwidth was 2.72Mhz. The phase response indicated a smooth transition from 0° to approximately -180°, suggesting good stability. When applying a 1 mV differential input signal, the output mirrored the input accurately, exhibiting minimal distortion. However, as the input signal was increased, clipping occurred, illustrating the amplifier's limitations when pushed beyond its linear operating range. Introducing a 5 mV DC offset resulted in a calculated output voltage of 802.33 mV, which was slightly different from the simulation result of 802.3, highlighting potential non-ideal behaviors in the circuit. Overall, while the differential amplifier performed well within its expected parameters, the observed clipping and offset discrepancies emphasize the need for careful design considerations in real-world applications to maintain signal integrity and ensure precision.

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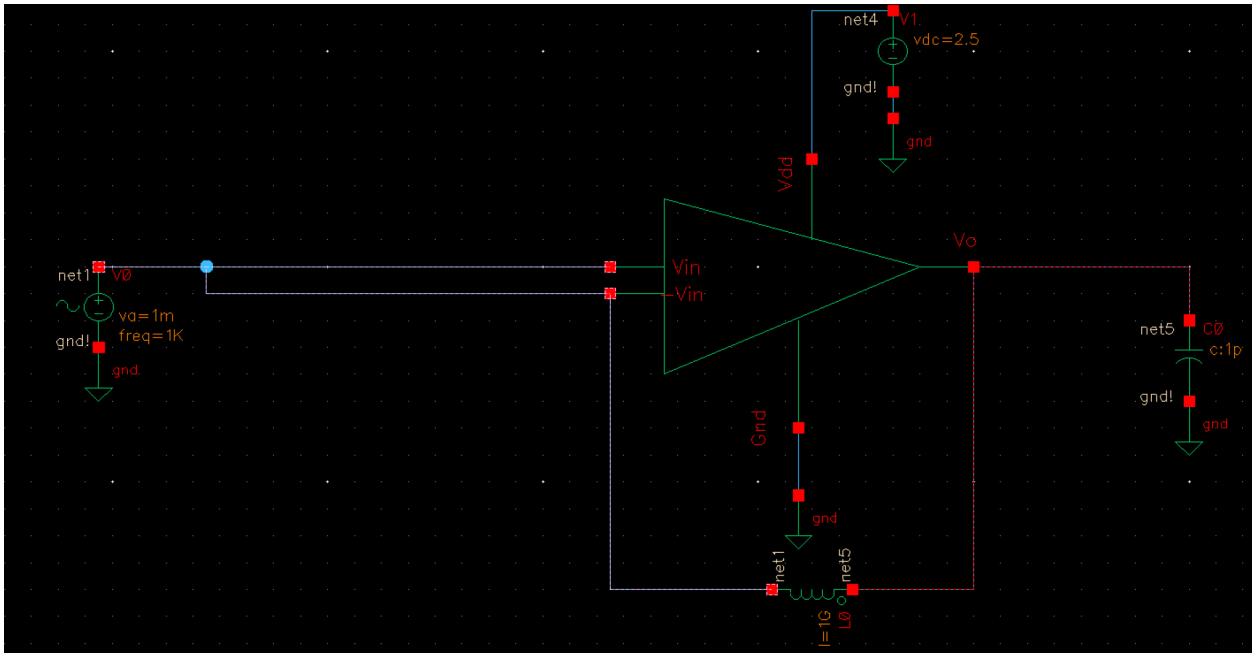
Common Mode:



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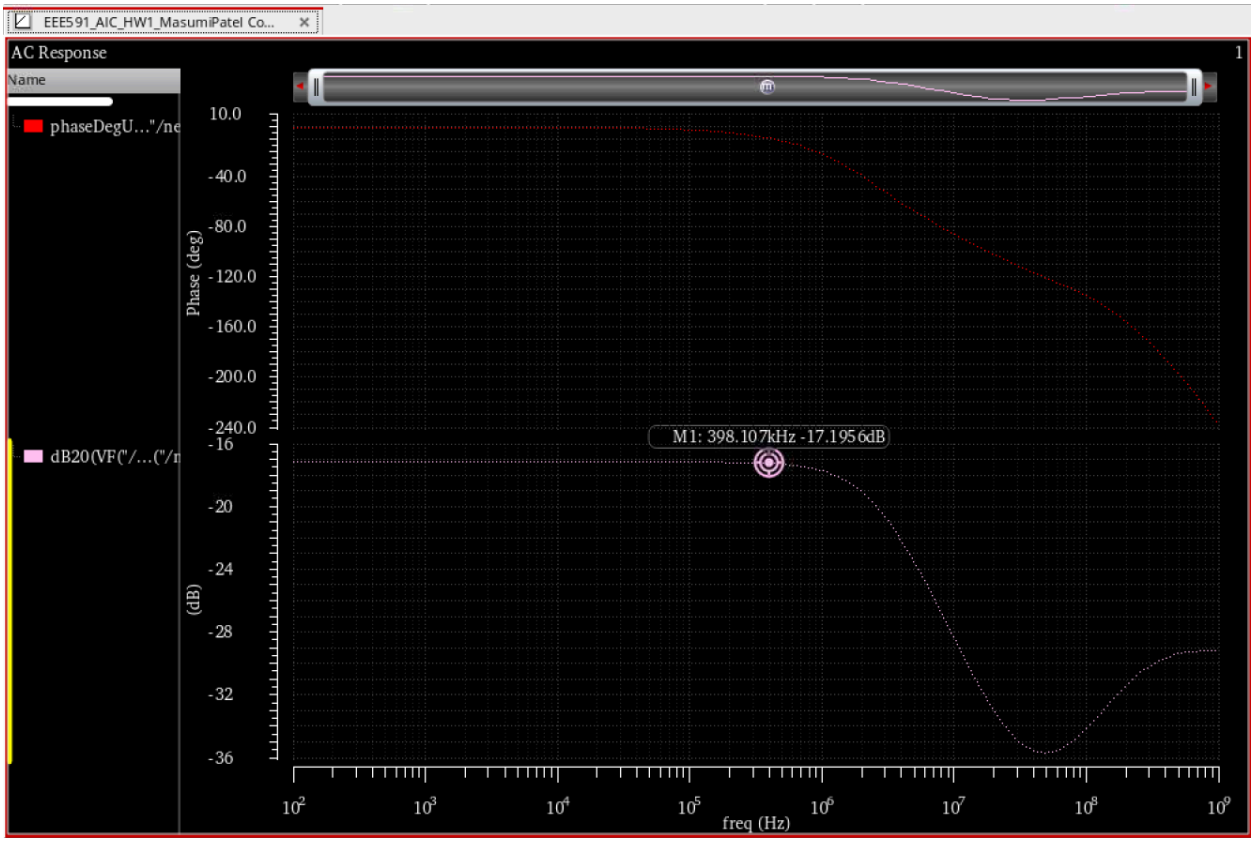

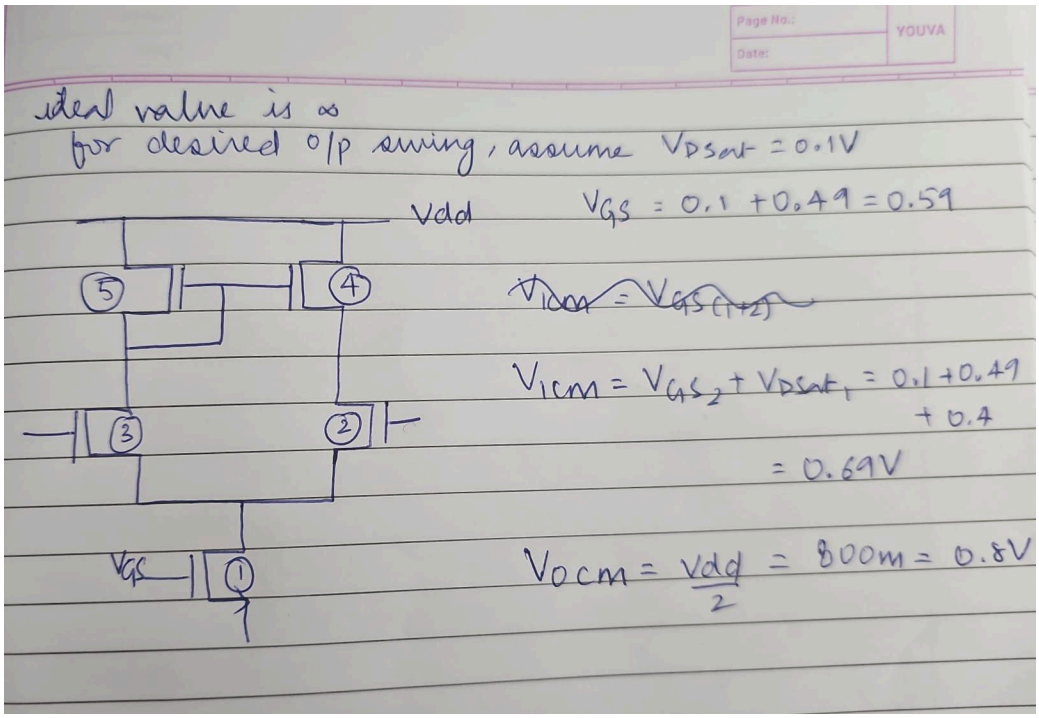

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→ Common mode

$$g_{m_2} = \frac{2 I_D}{V_{OV}} = \frac{2 \times 84.5\mu}{0.2} = 845\mu S$$

$$g_{os} = \frac{I_D}{V_n} = \frac{84.5}{4.75} = 1.778\mu S$$

$$A_{cm} = \frac{g_{os}}{2 g_{m_2}} = \frac{1.778}{2 \times 84.5} = 0.0105 = -20.55 dB$$

$$CMRR = A_{V_0} - A_{cm} = -20.55 - 33 = -52.55 dB$$

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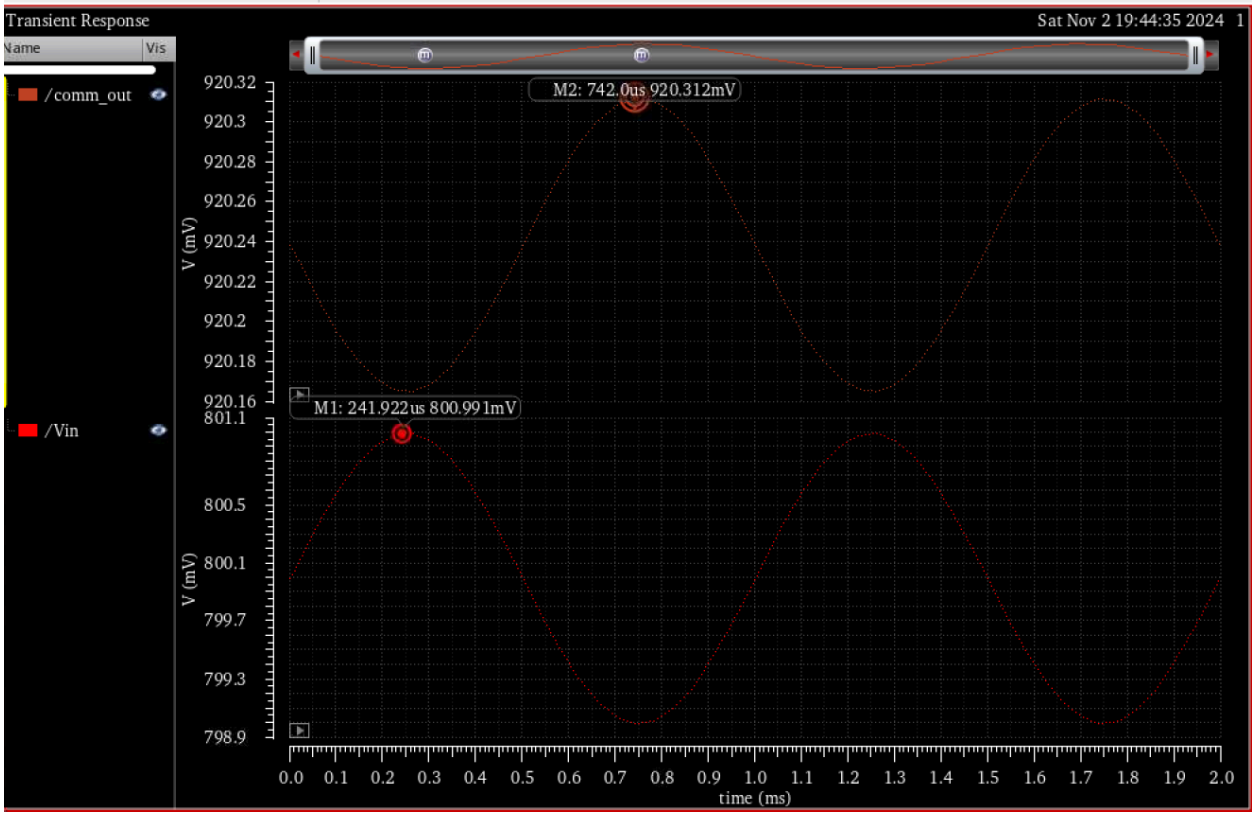
Finding Vocm from Vicm value via simulation



Ideally, Vocm should not change for any change in Vicm. However, as we observe in simulation that Vocm changes for change in Vicm until Vocm = Vdd/2.

Common mode gain with Dc voltage increased by 0.5V
0.5 V changes in Vicm leads to 0.16mV change in Vocm

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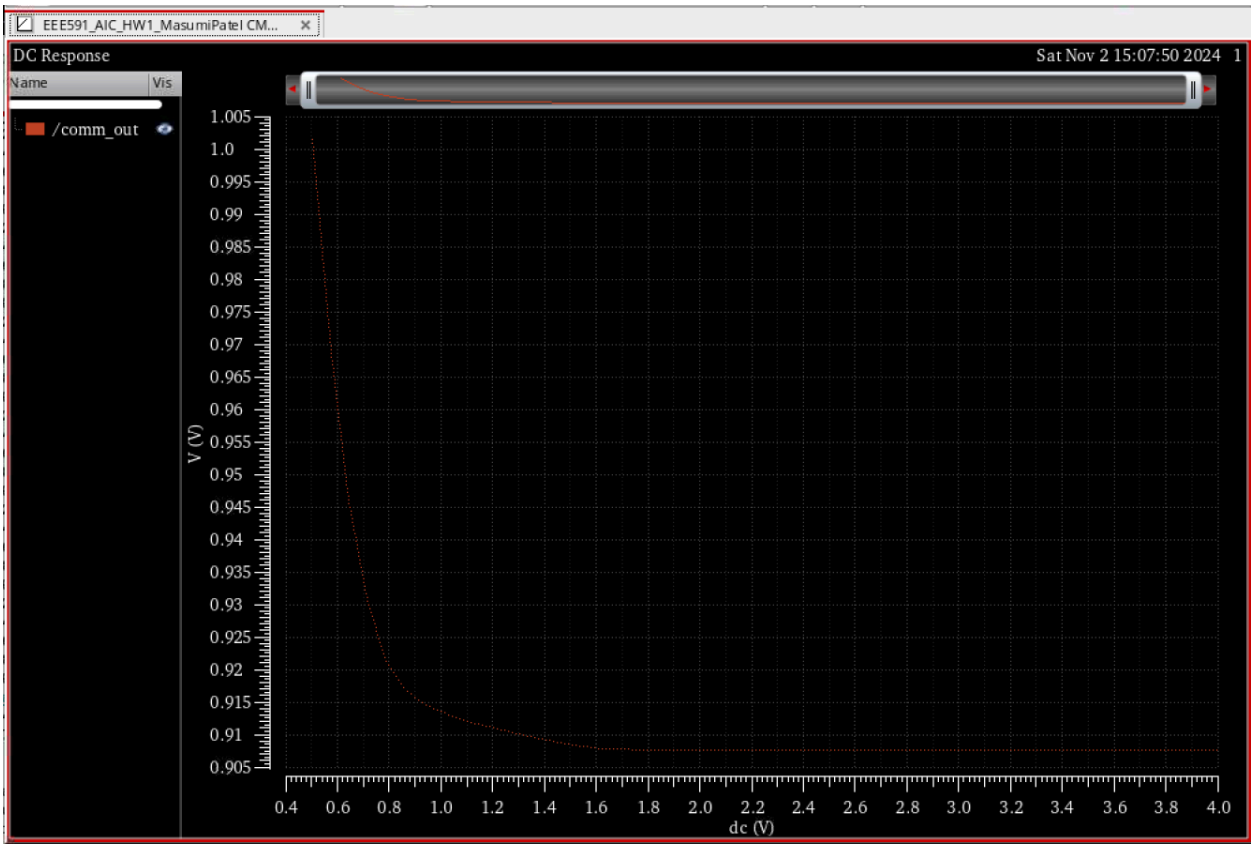

CMRR:

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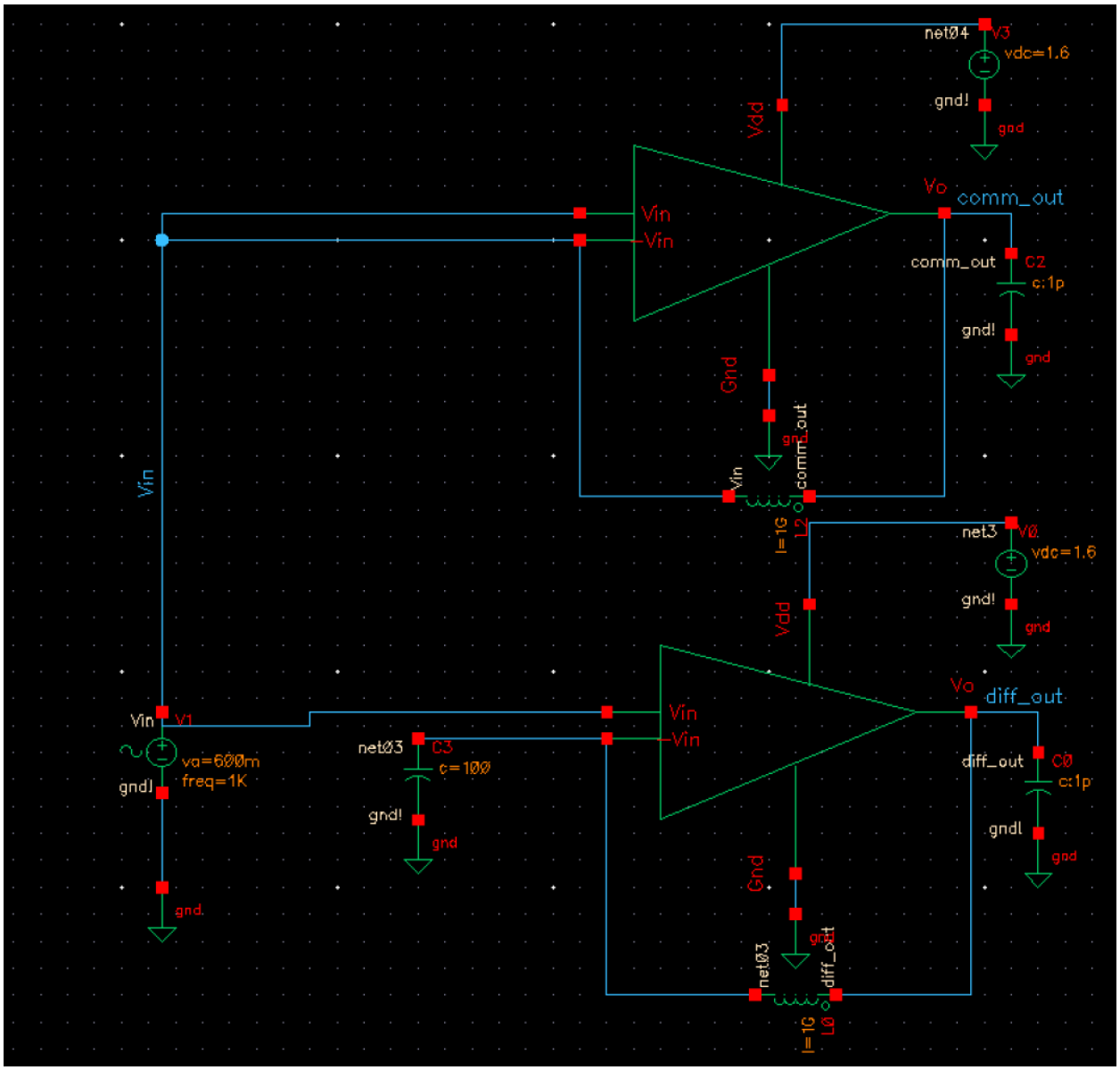
Circuit



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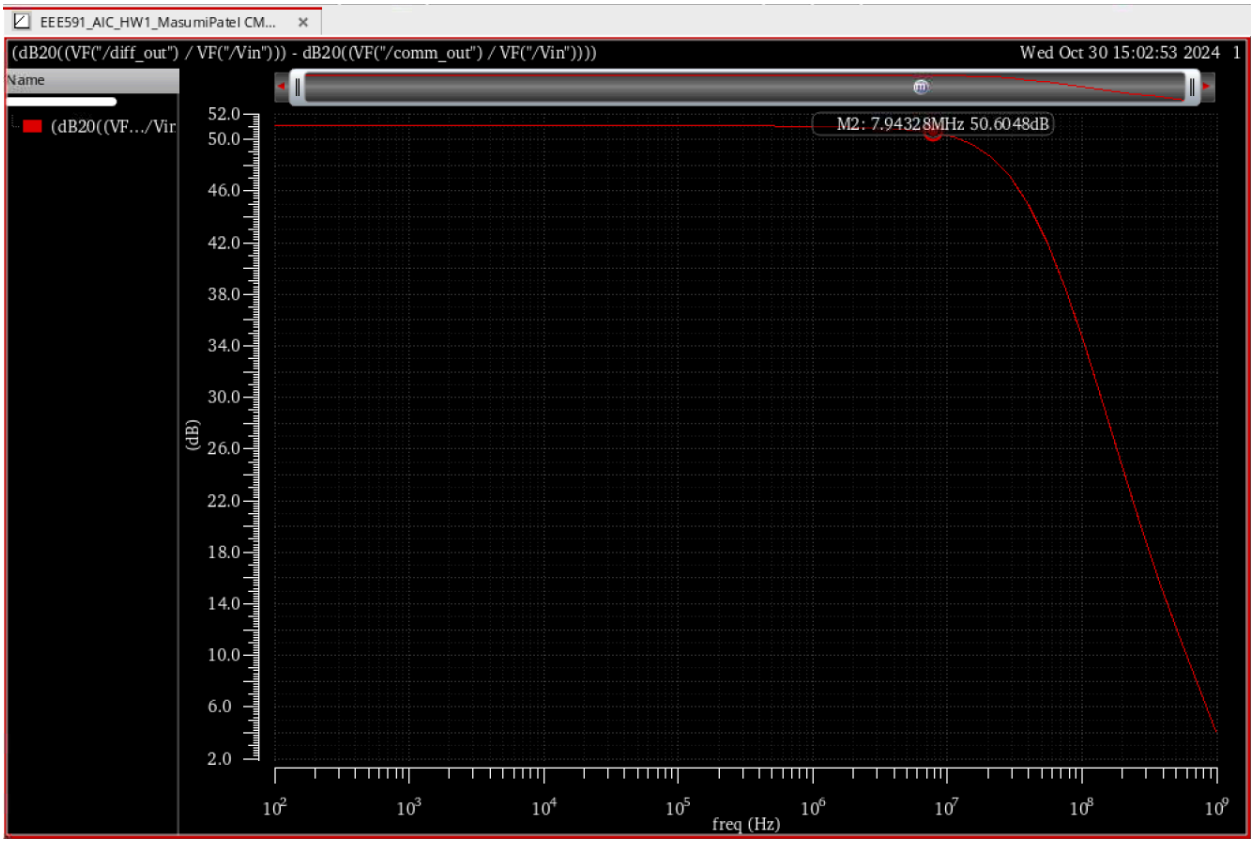
Common mode gain



The analysis of the differential amplifier revealed critical insights into its performance regarding common mode voltages and rejection capabilities. By calculating the input common mode voltage (VICM) and output common mode voltage (VOCM), we derived the common mode gain, indicating the amplifier's effectiveness in rejecting unwanted common mode signals. Upon increasing VICM by 0.5 V, the calculated VOCM increases with increase in VICM until VOCM reaches a value of Vdd/2 after which the value is stable was compared with simulation results, showing the values were close. The CMRR versus frequency plot illustrated a strong rejection of common mode signals at lower frequencies, consistent with expectations, but showed a decline at higher frequencies due to bandwidth limitations and phase shifts. This decline emphasizes the amplifier's susceptibility to noise in high-speed applications, underscoring the importance of robust design considerations to maintain performance. Overall, the results affirm the amplifier's capability to handle common mode inputs effectively, while highlighting areas for potential improvement in high-frequency scenarios.

Supply Rejection

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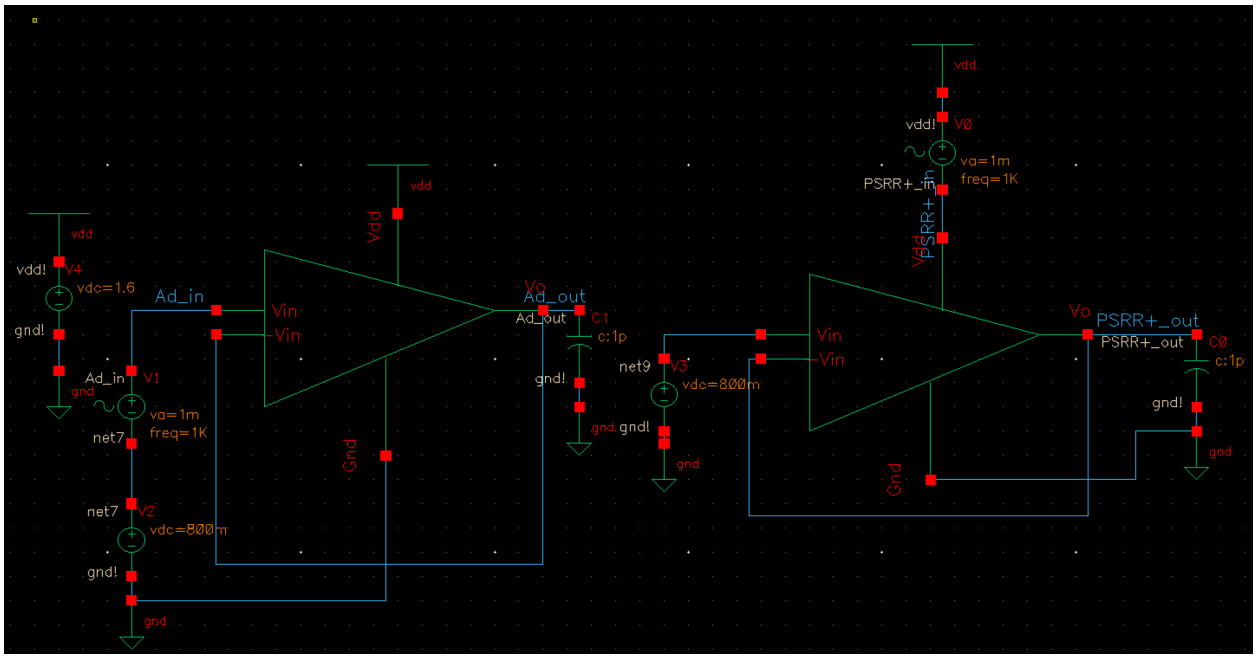
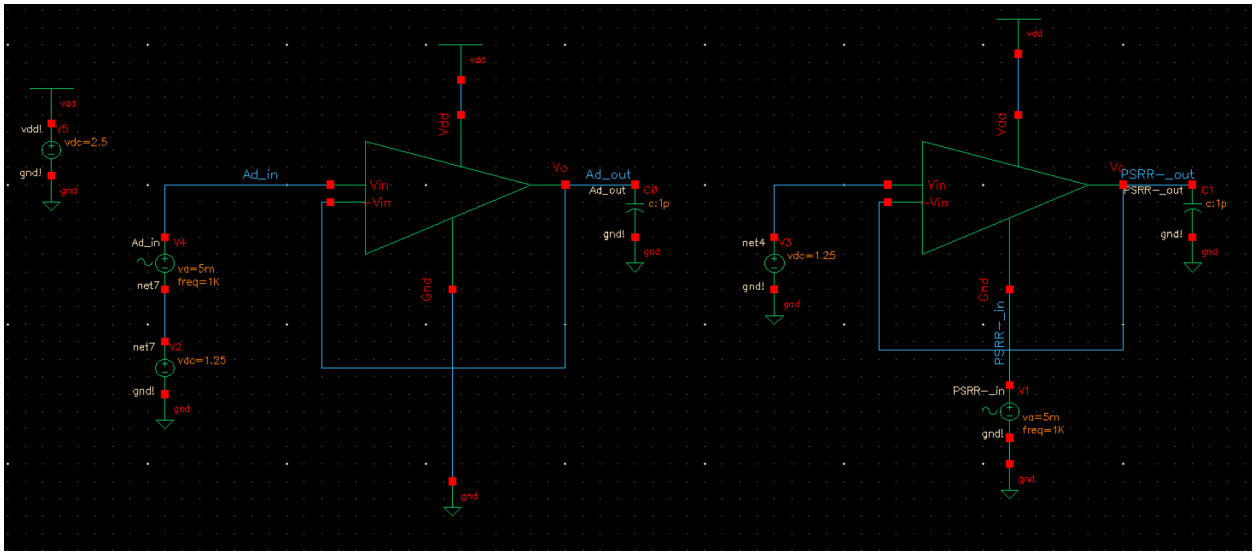
PSRR+ circuit



PSRR- circuit



Vs_noise and vos_noise

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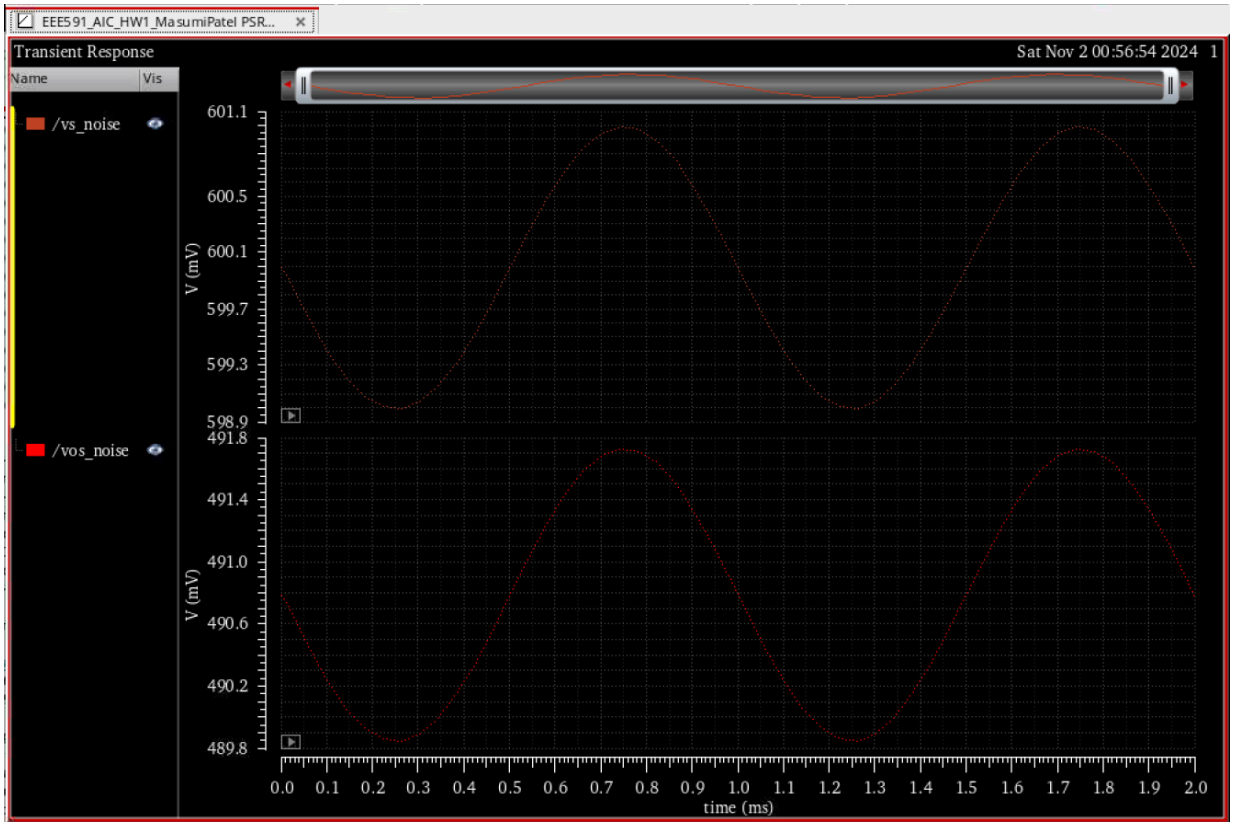

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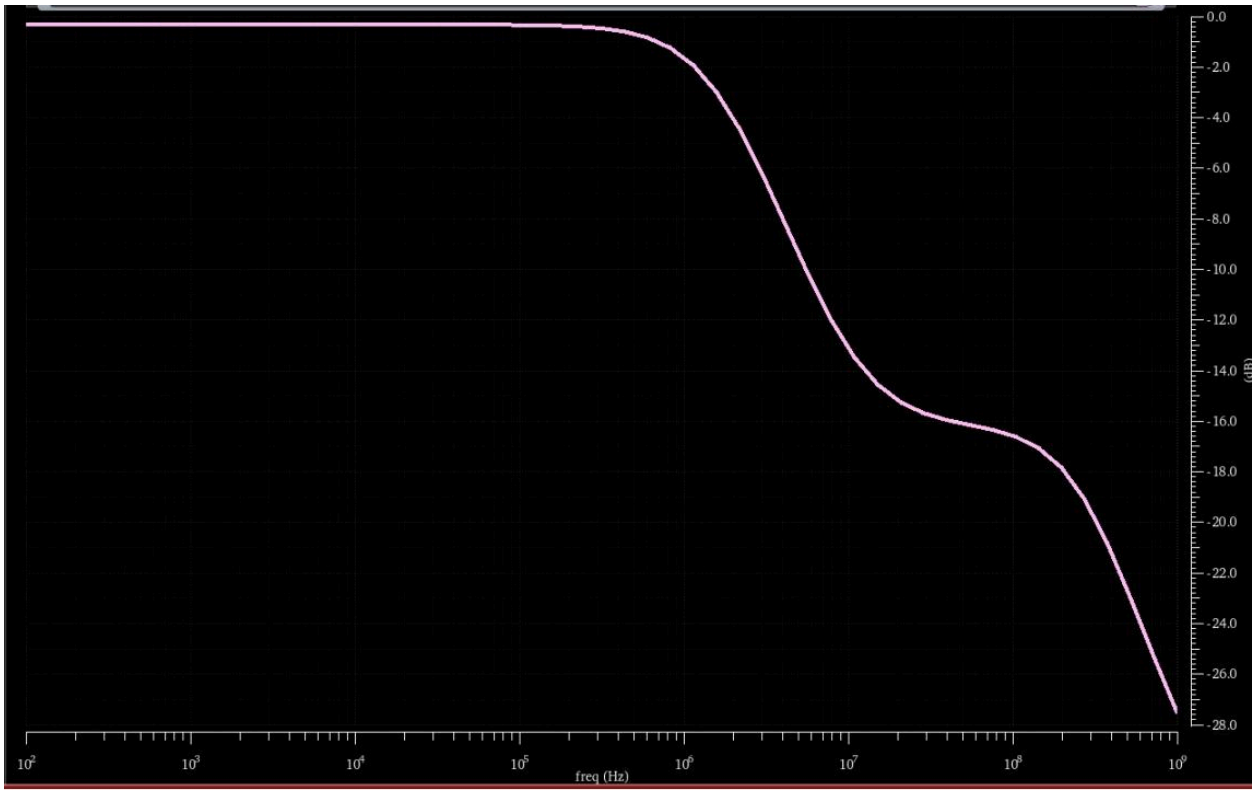
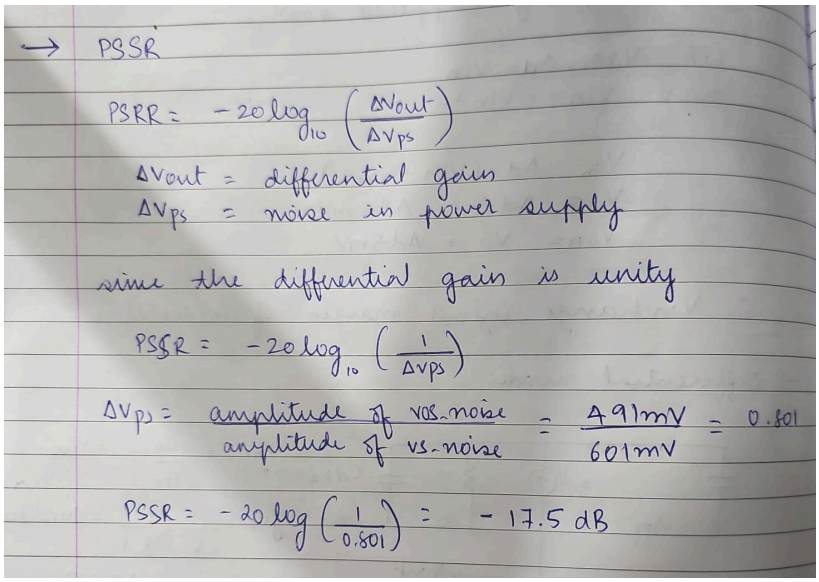
As_noise gain for PSRR+





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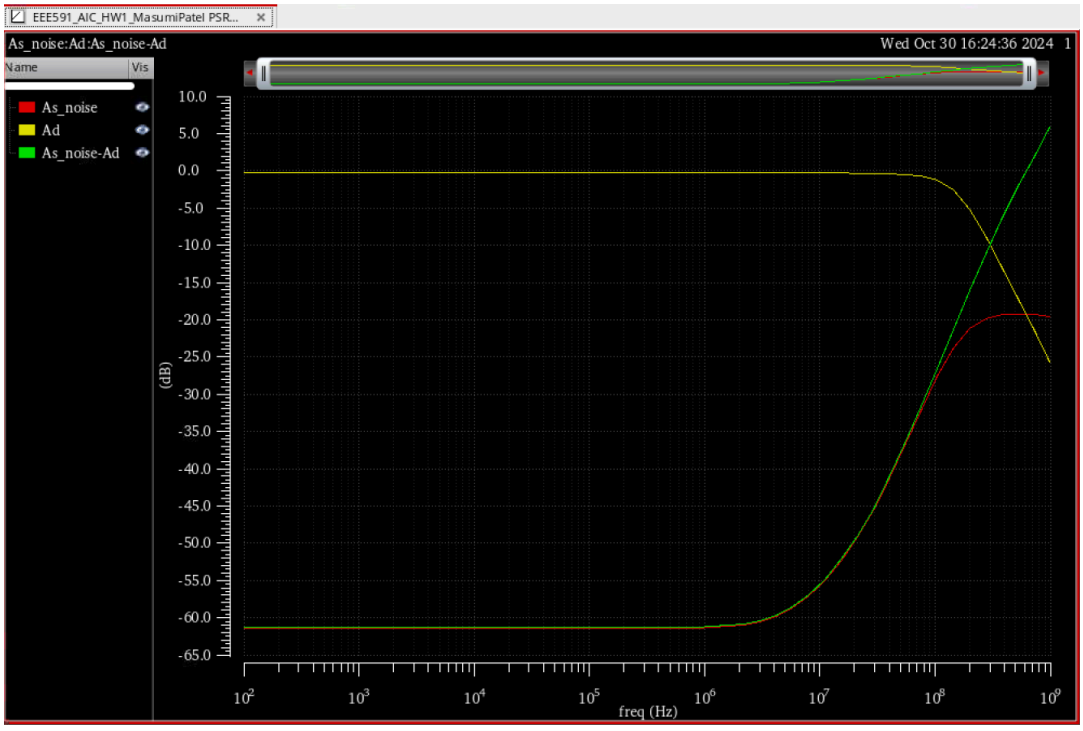
PSSR+

As_noise, Ad and PSRR-



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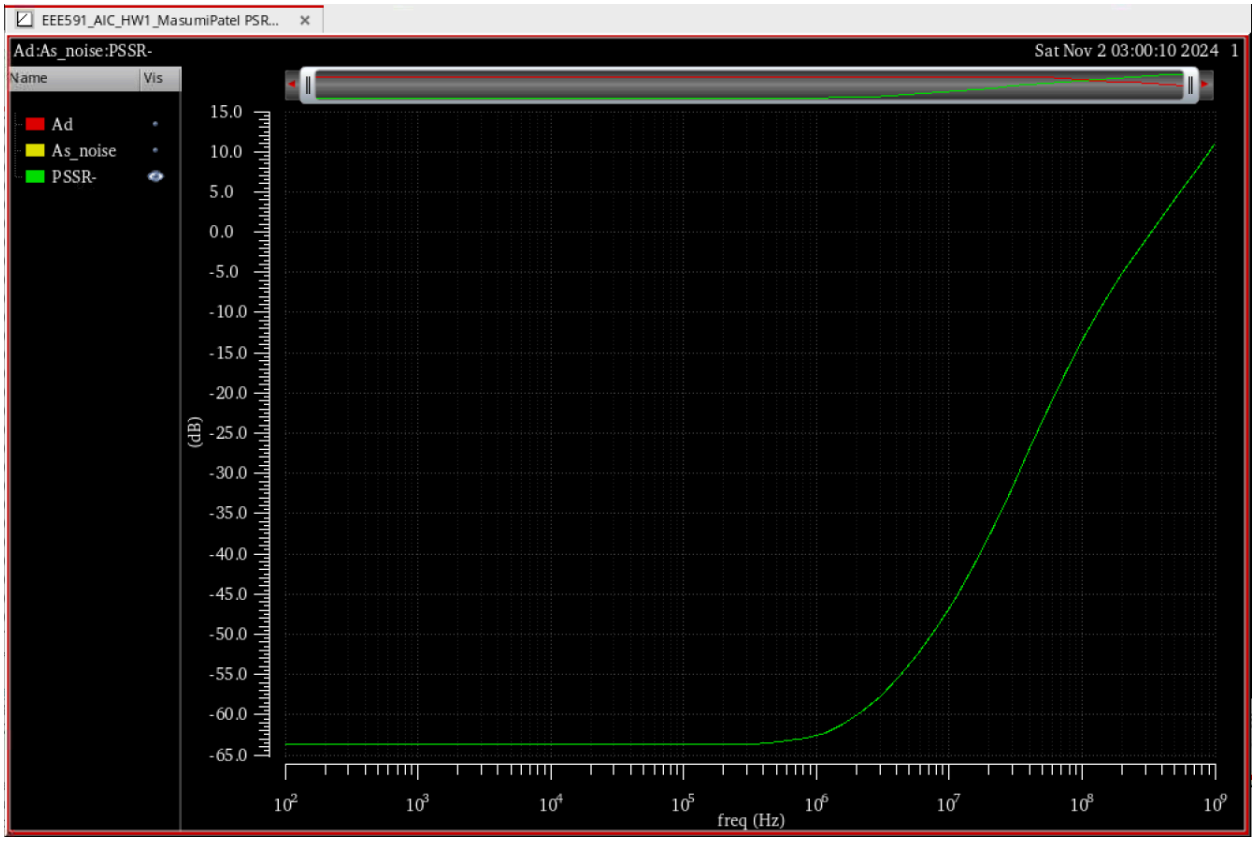
PSSR-



Conclusion:

The lab experiment on the differential amplifier provided valuable insights into its performance across key parameters. The amplifier exhibited a high DC gain and maintained effective operation across a range of frequencies, as demonstrated by its bandwidth capabilities. The high CMRR confirmed its efficiency in rejecting common-mode signals, which is essential for minimizing interference. However, the asymmetry in transistor characteristics relative to power and ground influenced the differences observed in PSRR+ and PSRR-, underlining how circuit topology and device mismatches can impact performance. The experiment emphasized the significance of optimizing power supply design to closely approach ideal conditions, which could enhance PSRR and overall stability. These findings underscore the need to consider both circuit configuration and component characteristics to achieve optimal results in future amplifier designs.

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