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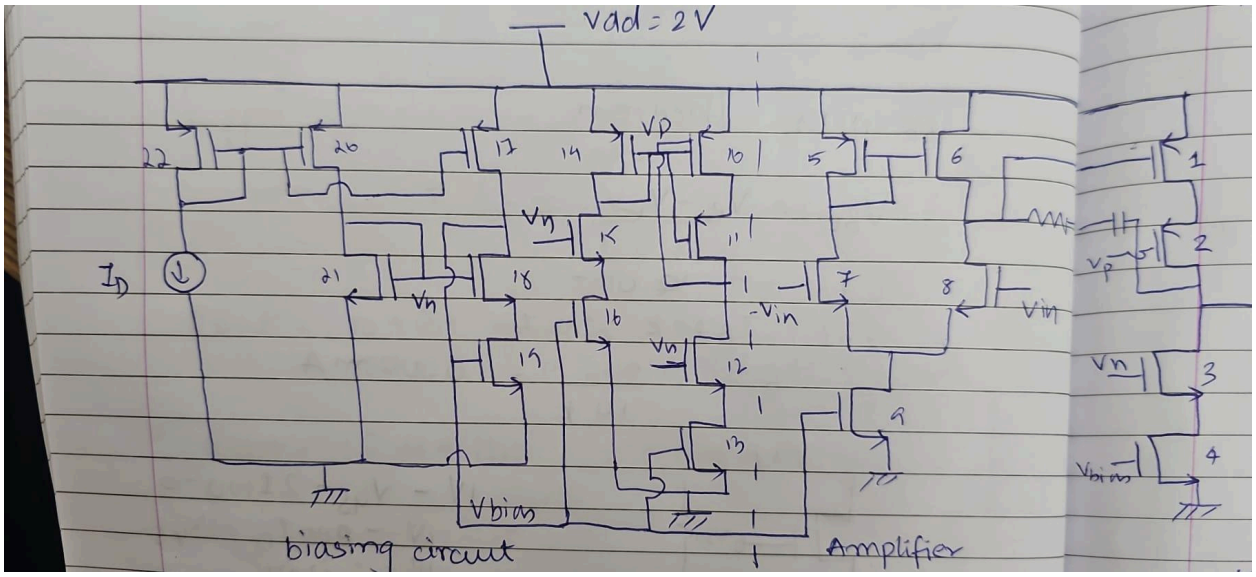
# EEE:591: Lab 4: Two-Stage Compensated Amplifier

1a. Hand Calculations




$k_n' = 2.7475 \times 10^{-4}$ A/V²  $k_p' = 0.95745 \times 10^{-4}$ A/V²

$V_{thn} = 0.49$V  $|V_{thp}| = 0.54$V

$V_{OV} = 0.2$V

Power $P = VI$  max power = 1mW

$I_m = 2 \times I$

$I = 0.5mA = 500\mu A$ (max current to be used

Current in bias circuit: 135 μA

current in diff amp : 53.75 ≈ 54 μA

current in cascode amp: 254.4 ≈ 255 μA

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Biasing current

$I_{bias} = 10\mu A$

$I_D = \frac{1}{2} k_p' \left(\frac{W}{L}\right)_{22} (V_{ov})^2$

$\left(\frac{W}{L}\right)_{22} = \frac{10 \times 10^{-6} \times 2}{0.9575 \times 10^{-4} \times 0.04} = 5.22$

$L = 600nm \quad \therefore W = 3.133 \approx 3.15\mu m$

$\left(\frac{W}{L}\right)_{20}$

Increasing current in consequent current mirror branches by 3 times

$\left(\frac{W}{L}\right)_{20} = 3 \times \left(\frac{W}{L}\right)_{22} = 15.66$

$L = 600nm \quad W = 9.3\mu m \approx 9\mu m$

$\left(\frac{W}{L}\right)_{21} = \frac{30 \times 10^{-6} \times 2}{2.7475 \times 10^{-4} \times 0.04} = 16.75$

$L = 600nm \quad W = 10.05\mu m$

Therefore

$\left(\frac{W}{L}\right)_{20} = \left(\frac{W}{L}\right)_{17} = \left(\frac{W}{L}\right)_{14} = \left(\frac{W}{L}\right)_{11}$

Similarly

$\left(\frac{W}{L}\right)_{21} = \left(\frac{W}{L}\right)_{18} = \left(\frac{W}{L}\right)_{19} = \left(\frac{W}{L}\right)_{15} = \left(\frac{W}{L}\right)_{16} = \left(\frac{W}{L}\right)_{12} = \left(\frac{W}{L}\right)_{13}$

Differential amplifier

$I = \frac{1}{2} k_p' \left(\frac{W}{L}\right)_9 V_{ov}^2$

$\left(\frac{W}{L}\right)_9 = \frac{54 \times 10^{-6} \times 2}{2.7475 \times 10^{-4} \times 0.04} = 18.43$

$L = 600nm \quad W = 11.058\mu m$

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$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_8 = \frac{1}{2}\left(\frac{W}{L}\right)_9 = 9.215$

$L = 600nm \quad W = 5.52\mu m$

$\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = 3 \times \left(\frac{W}{L}\right)_7 = 16.587\mu m$

since the only difference is $kp' = 3kn$

→ Cascode biasing

Current in current mirror with transistor 10 is to be multiplied and replicated in cascode branch

$I_{10} = 36.3\ \mu A \qquad I_{remain} = 255\ \mu A$

$\frac{I_r}{I_{10}} = \frac{254.4}{36.3} = 7.008 \approx 7$

$\left(\frac{W}{L}\right)_1 = 7 \times \left(\frac{W}{L}\right)_{10} = 7 \times 75\mu = 525\mu$

Similarly

$\left(\frac{W}{L}\right)_2 = 7 \times \left(\frac{W}{L}\right)_{11} = 7 \times 36 = 252\mu$

$\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_3 = 7 \times \left(\frac{W}{L}\right)_{12} = 7 \times 10 = 70\mu.$

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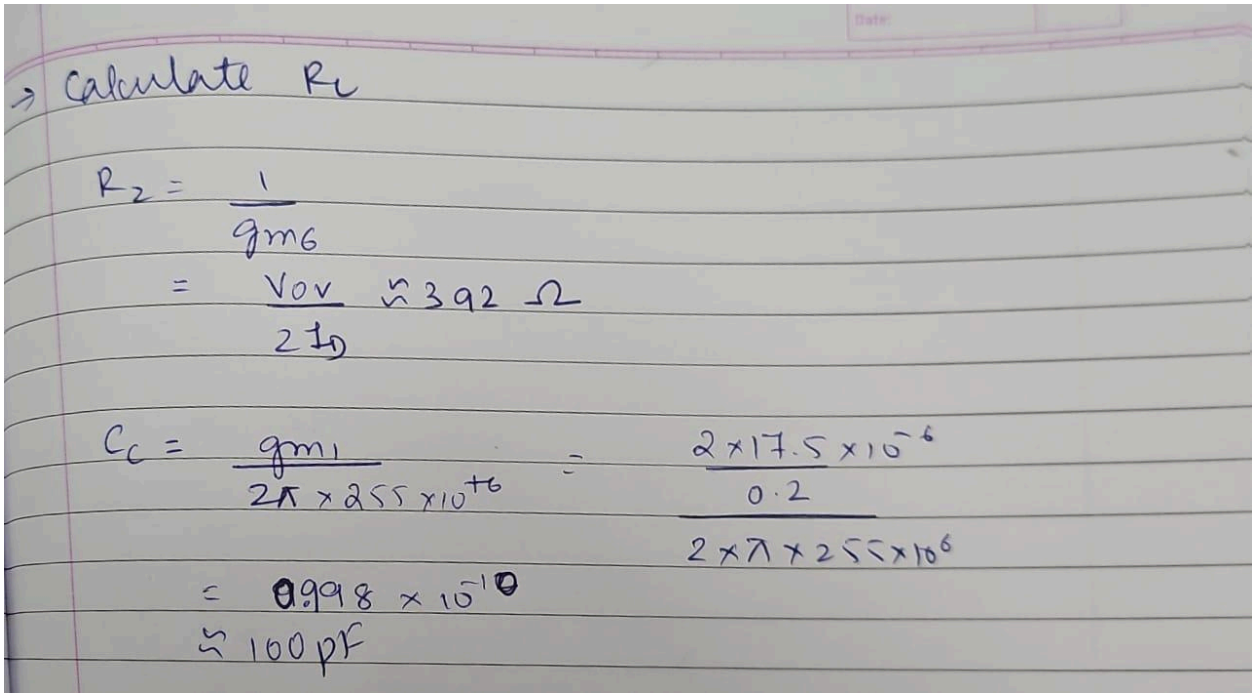
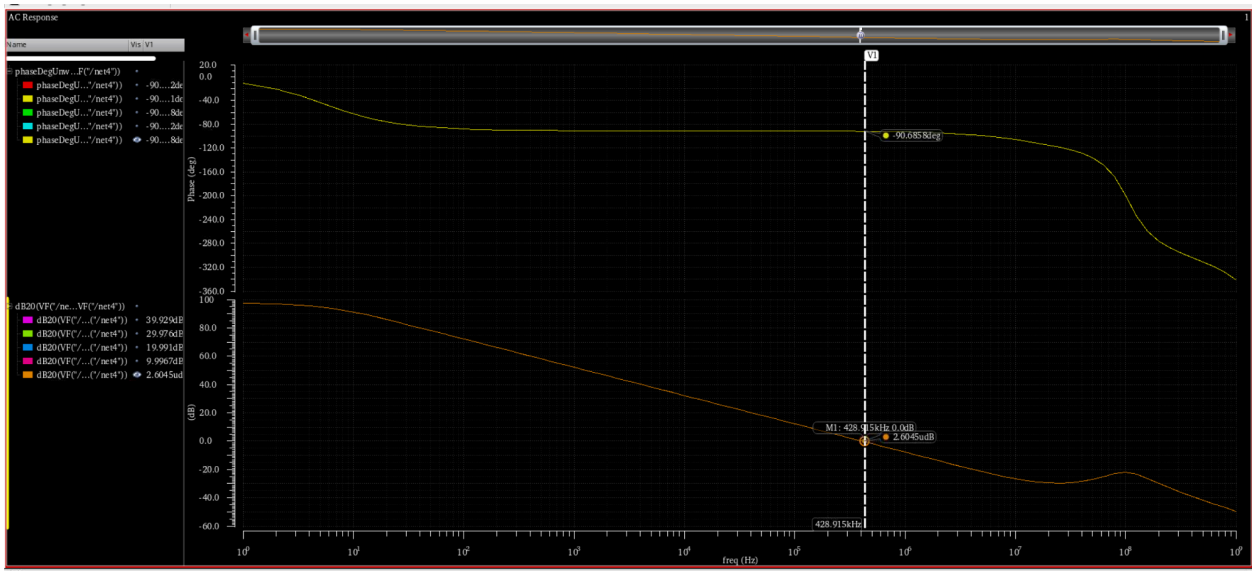
1b.




For the capacitance value of 100p F, the phase margin is approximately -180 - (-90)=-90, which is lesser than -120. Thus meeting the design specifications.



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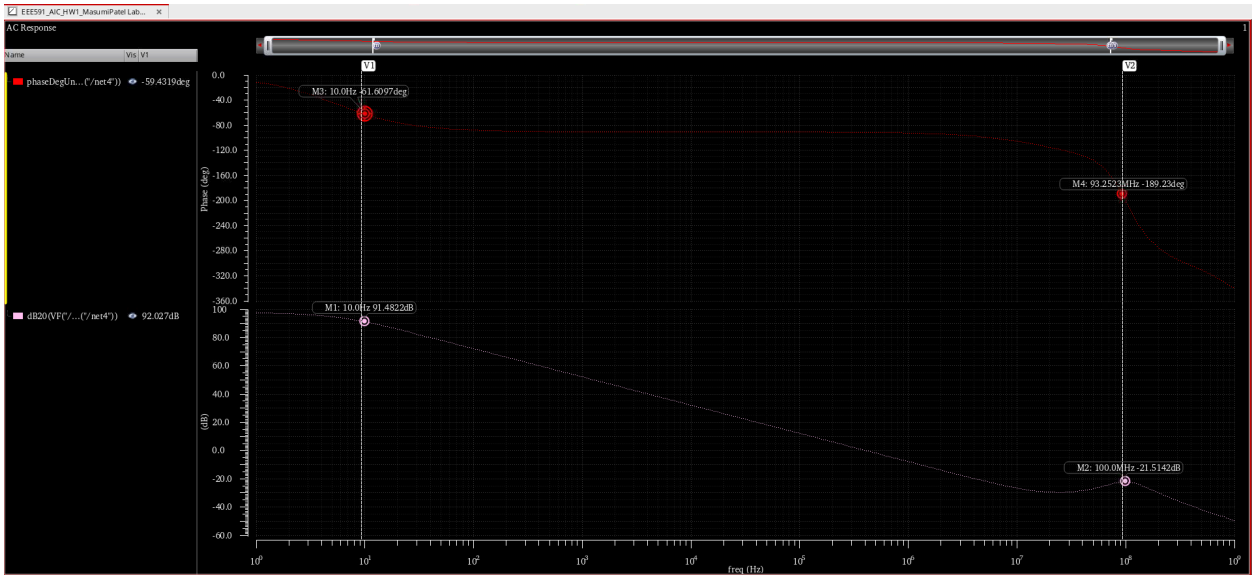
1c The two poles value approximately from the simulation is shown below.
Pole 1 is obtained at BW 10Hz and Pole 2 is obtained at BW 100MHz



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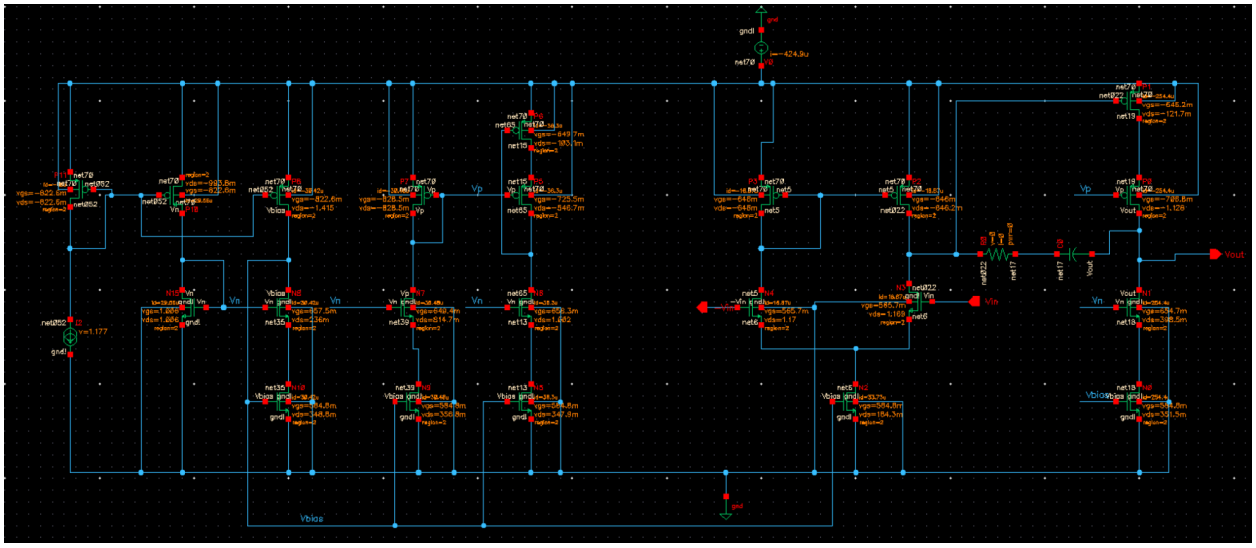
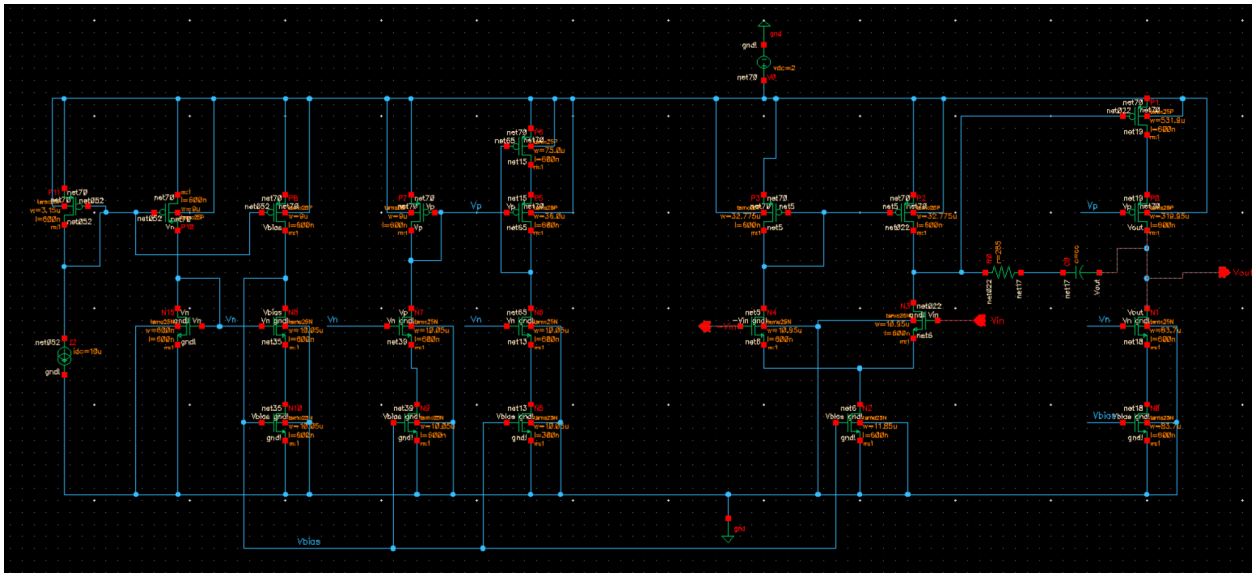
2a
DC operating points



Final device W/L ratio, resistance and capacitance value



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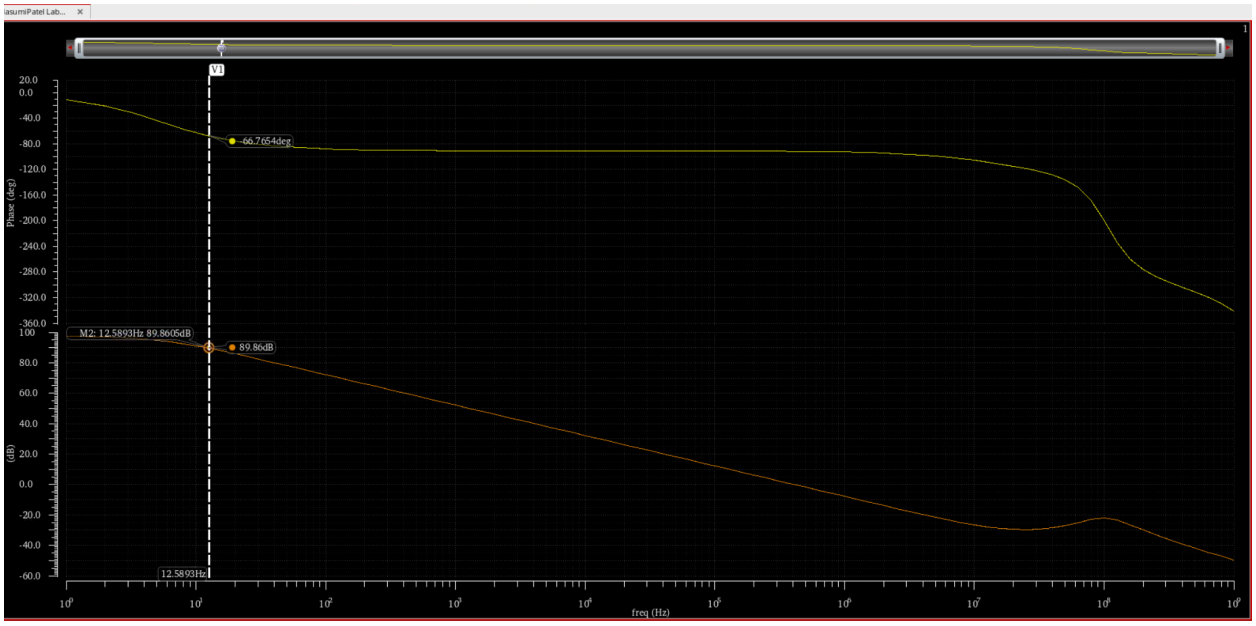
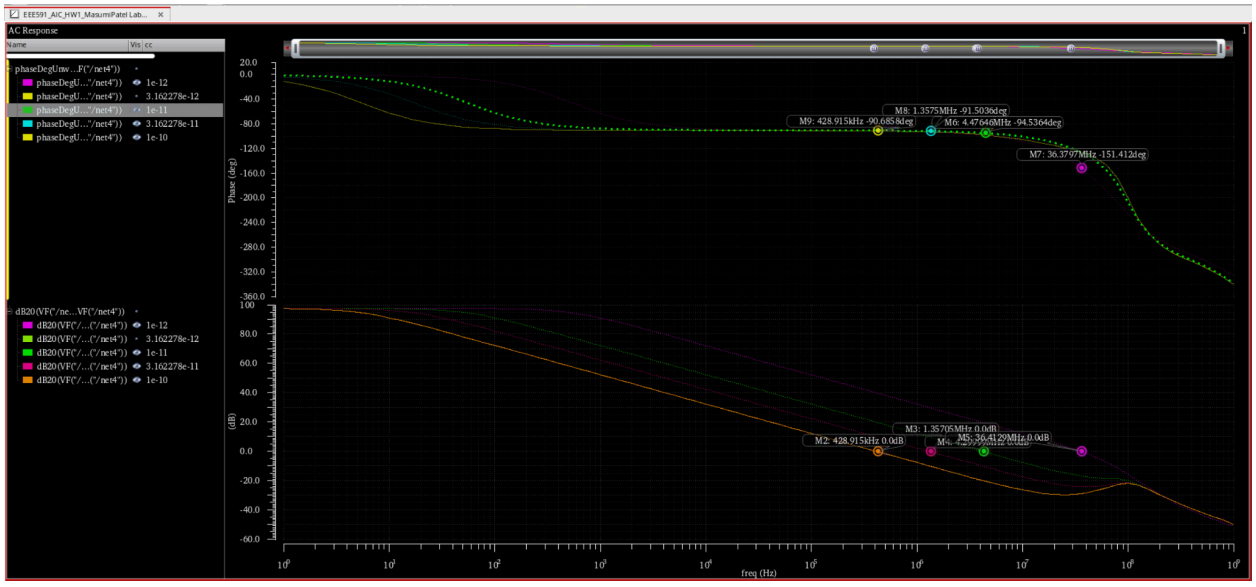
## 2b Gain vs Frequency and Phase vs Frequency




## Phase Margin for different values of capacitance Cc



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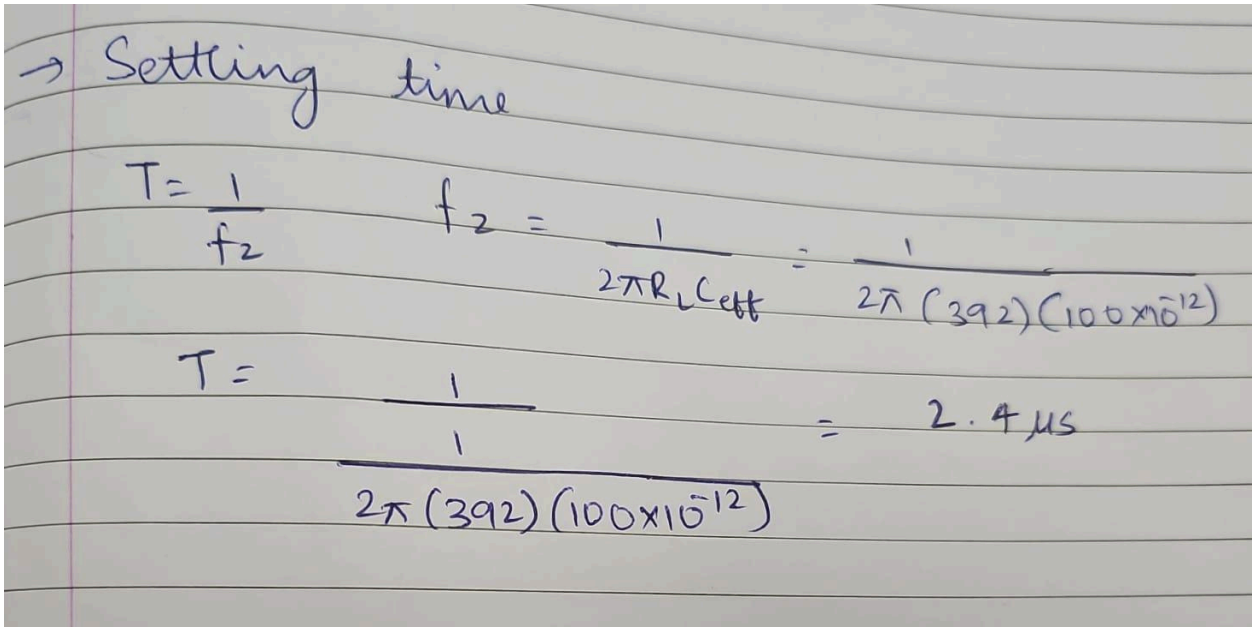
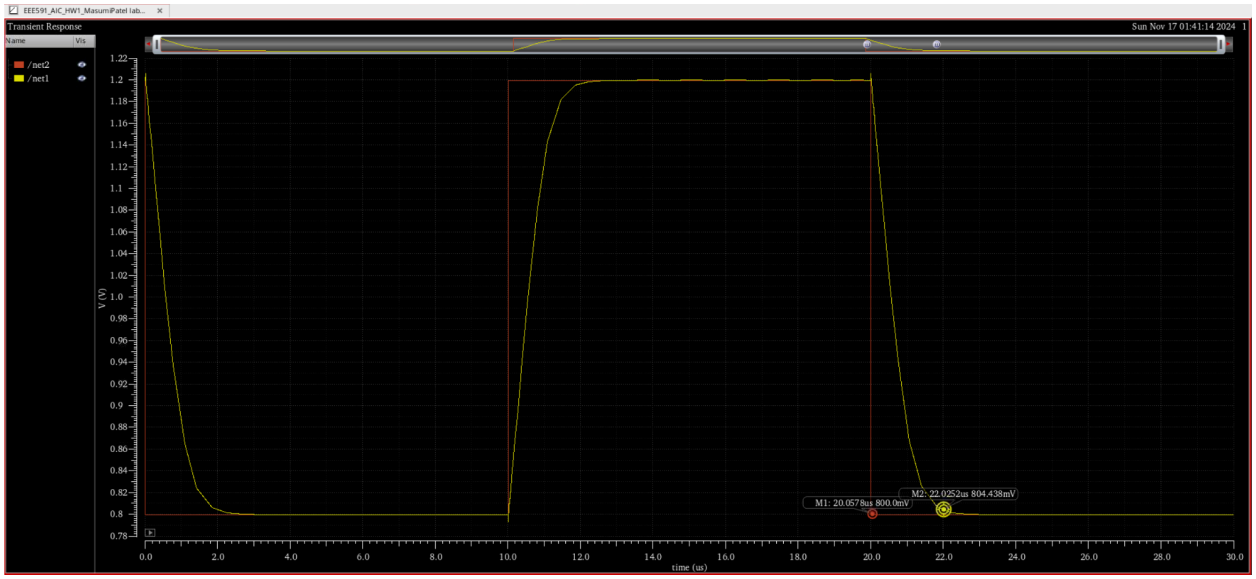
2c




The minimum settling time depends on how fast the amplifier can respond, which is determined by its unity-gain frequency. The higher the unity-gain frequency, the faster the amplifier can settle to its final value.

Settling Time of the amplifier is 1.9674 ≃ 2us



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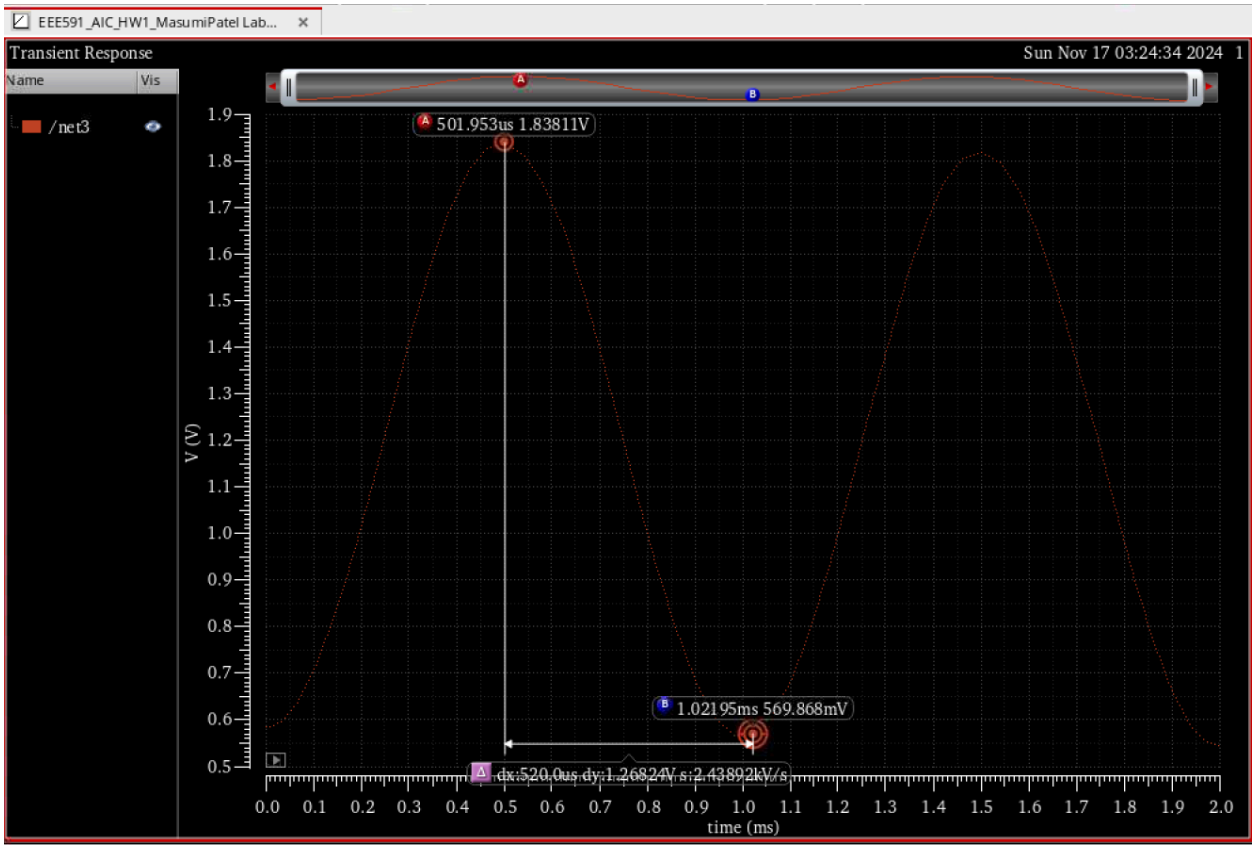
Transient output showing output swing




3a.The sources of discrepancy lie in the settling time as I calculated a settling time of 2.4us and the simulation gave me a settling time of 2us. The RL value I calculated is 392 ohm but the simulated value is 285 ohm.

b. I was able to achieve all parameters. =) My ID of 0.423mA is less than 0.5mA, my DC Gain of 89.86dB is greater than 70dB, my output swing of 1.36V is greater than 1.3V peak to peak

c.To achieve higher bandwidth, we can reduce the value of compensation capacitance (Cc) but the trade off is that our phase margin will reduce.