1.

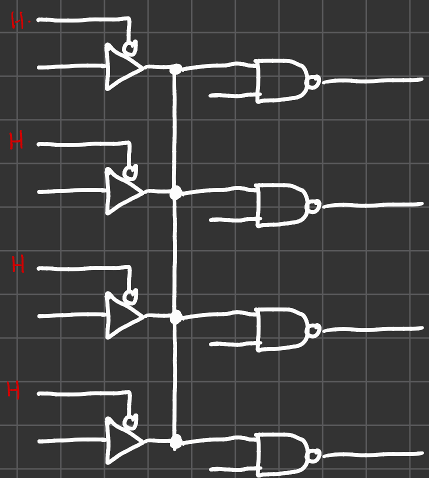
SN74LVC

V_{oh}	2.3 V
I_{oh}	-24 mA
V_{oL}	0.55 V
I_{oL}	24 mA

FPGA

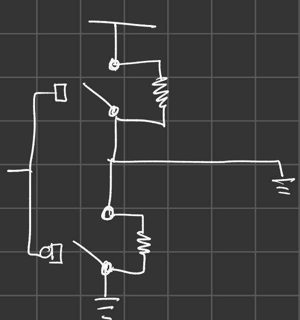
en haut = 1 V_{Ih}	2.0 V
I_{Ih}	10 µA
sous = 0 V_{IL}	0.8 V
I_{IL}	-10 µA

2.



I_{Ih} = 0,1 mA 26mA à high = 26

I_{OL} = -0,4 mA 24mA à low = 60



$26m + 20\mu(x-1) = 0.02m\,X$

$0{,}0026 = 20 \cdot 10^{-6}(x-1) + 26 \cdot 10^{-6} \cdot x$

$x = 65$

$0{,}0024 = 20 \cdot 10^{-6}(x-1) + 0{,}0004\,x$

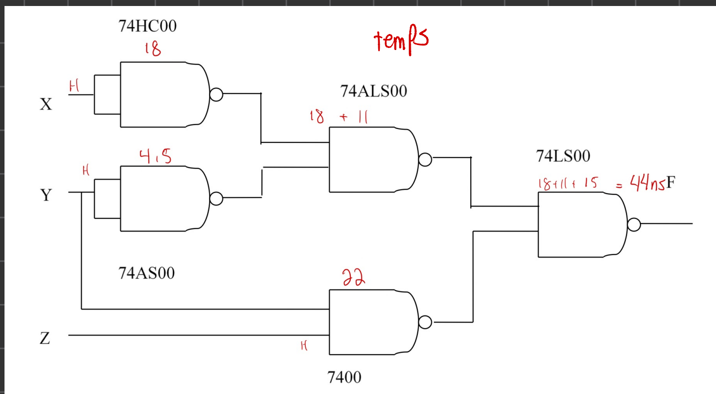
$x = 57$ → lui car c'est le pire

3. a) $\overline{(\overline{\bar{x}\bar{y}})(\overline{yz})} = F$

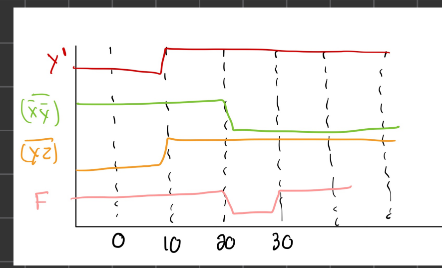
$(\bar{x}\bar{y}) + (yz) = F$ La morgan dit que le doublon de prime disparait

$\bar{x}\bar{y} + yz = F$

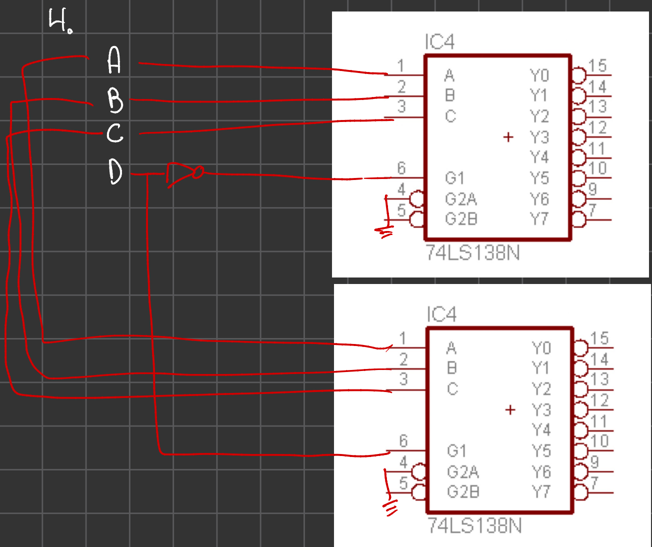
b)



c)



4.



on mets 0 à D pis ça active puce 1
1 à D pis ça active puce 2