Creating a RISC-V heterogeneous CPU architecture

Progress report

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1 Introduction

The aim of this project is to design a heterogeneous SoC using the RISC-V open source core designs. Once designed, the SoC should be implementable on an FPGA and be able to execute bare-metal C code and assembly with SMP, demonstrating that all cores in the SoC can be used at the same time.

Designing a processor is a complex challenge. They need to be power efficient to reduce the cost of running the system, as well as providing adequate processing power when required. Often one is sacrificed to improve the other: for instance, energy efficiency is often reduced due in designs of large processors containing multiple cores. Due to the increased size and complexity, more power has to be supplied to achieve the same performance as a smaller processor.

A heterogeneous CPU attempts to solve this issue by combining dissimilar core designs; often a powerful core, or p-core, and an efficient core, or e-core. When only light processing is required, the p-core can be effectively shutdown and the e-core will do all processing, resulting in less power used. For heavy processing, the p-core is then used to increase peak performance. Depending on the exact implementation, the p-core can be used either individually or in tandem with the e-core, but both result in greater performance than just the e-core.

This has been used extensively in many mobile devices. ARM released the big.LITTLE in 2011[1], a mobile heterogeneous architecture. The architecture provides the low power usage needed in mobile devices the majority of the time when idle, only running tasks like checking for new messages. It also provides the high performance that can be demanded from phones when used to browse the internet, play mobile games, etc. Most big.LITTLE designs use HMP (heterogeneous multiprocessing) where all cores are available to have processes assigned to them at all times. The alternatives to this are: clustered switching, where either the big cores or the LITTLE cores are in use, and in-kernel switching, where big and LITTLE cores are paired to form a virtual core and only one performs the tasks assigned to the virtual core at any one time.

1.1 Related work

1.1.1 A RISC-V Heterogeneous SoC for Embedded Devices

A 64-bit RISC-V host core that offloads tasks to a PMCA (Programmable Many-Core Accelerator) made from 8 32-bit RISC-V cores. Implements two types of RISC-V core in a single SoC, but one is used as an accelerator for the other as opposed to them being of equal standing.

1.1.2 Muntjac multicore RV64 processor

1.2 Objectives

The overall aim is design a heterogeneous SoC containing two types of RISC-V core that can execute bare-metal C code and assembly with SMP. Objectives have been labelled according to the MoSCoW method to indicate their importance and expected completion.

1. Design a heterogeneous RISC-V SoC containing 2 dissimilar cores, each capable of executing at least the RV64 instruction set (Must).

2. Execute instructions on both cores when implemented in an SoC on an FPGA (Must).

3. Measure the performance of the SoC for comparison against single-core designs. (Must)

4. Run Linux on the SoC and connect to it via SSH (Could).

5. Allow processes to execute on both cores inside of Linux (Could).

6. Intelligently select which core the process will run on, depending on factors such as process priority and resource usage (Won't).

2 Background

Your literature review goes here. **?**] discusses the advantages of functional programming by exploring *e.g.* lists, trees, and noughts and crosses in a functional programming language.

3 Progress

Summarise the progress you have made so far. You can cross-reference other sections (Section 2).

4 Project management

Include a timetable (in 2 week chunks) for the remainder of the academic year, up until the submission deadline.

References

[1] A. Ltd. big.little processing. `https://web.archive.org/web/20121022055646/http://www.arm.com/products/processors/technologies/bigLITTLEprocessing.php`, 2011.