

Introduction to VLSI – Final project

Implementation stage

Matan Amit Cohen

Madina Saidova

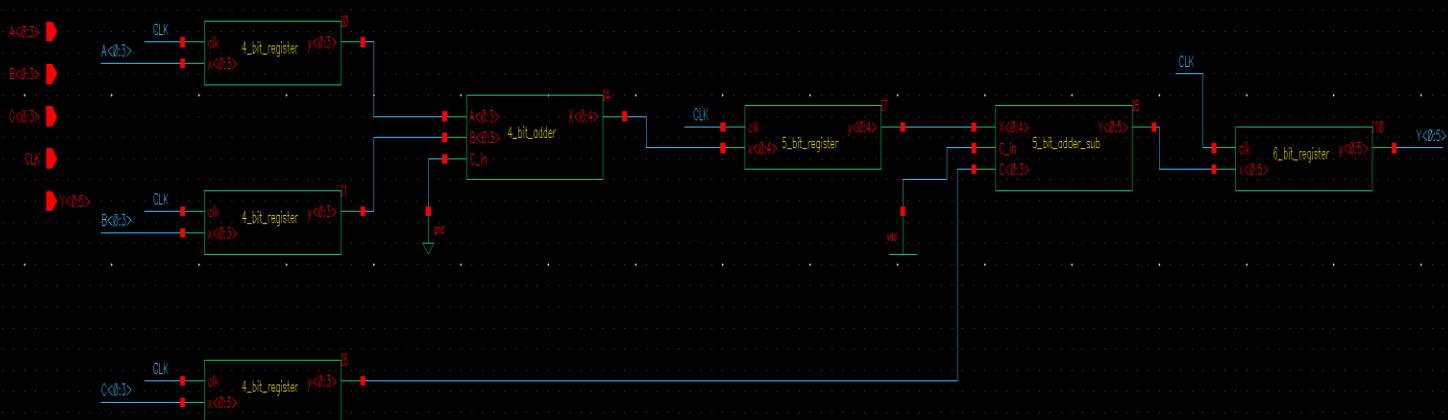
Bshara Rhall

Lior Daniel

ALU Implementation

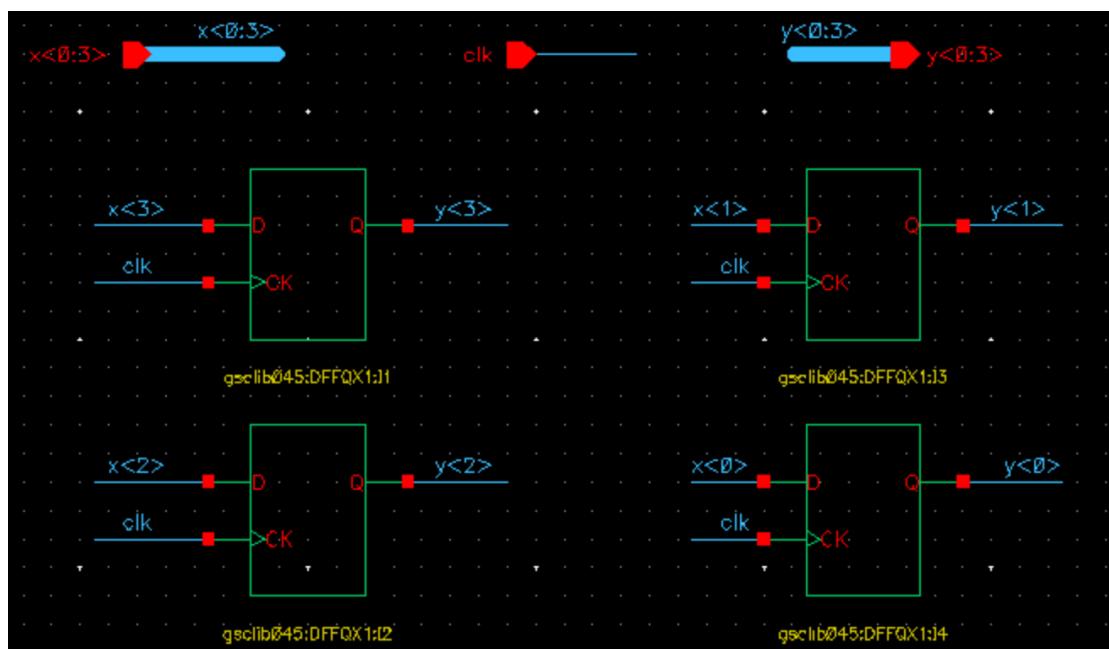
For all the components in the project, a schematic was implemented, and for the **4_bit_adder**, a layout was designed according to the planning details in Part A. Screenshots of these, along with the successful DRC and LVS runs, are attached. The simulations can be found at the end.

Below is the overall system schematic :

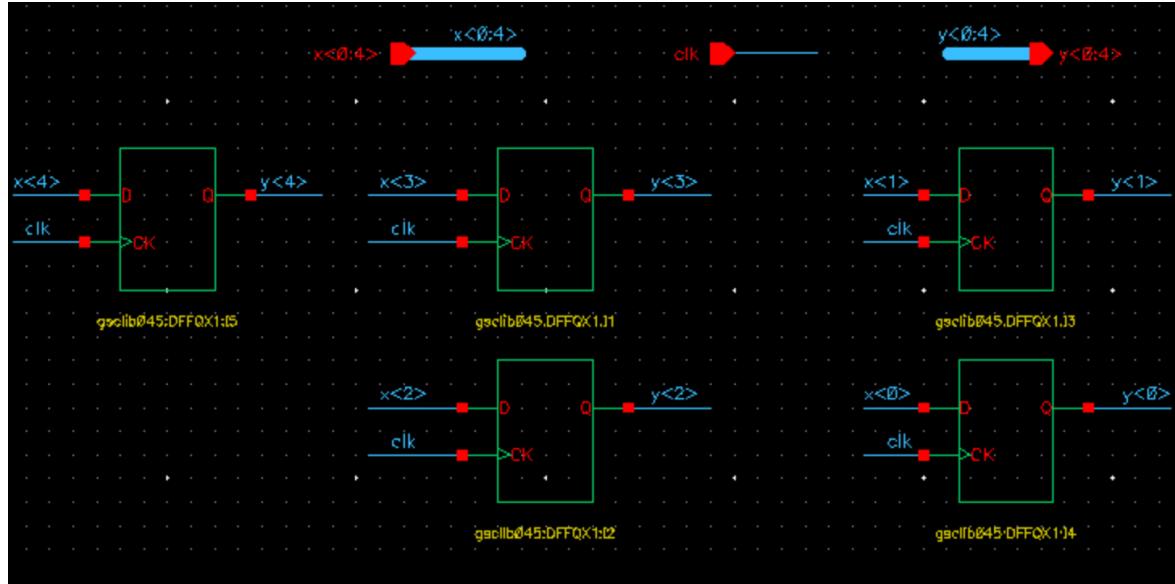


Below are all the system components' schematics:

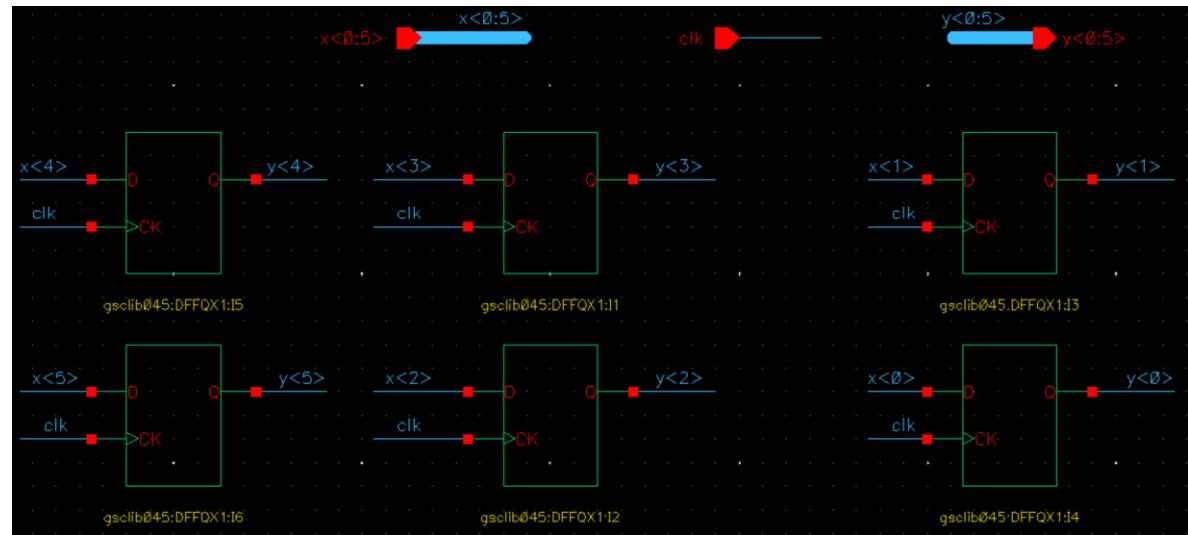
- **4_bit_register**



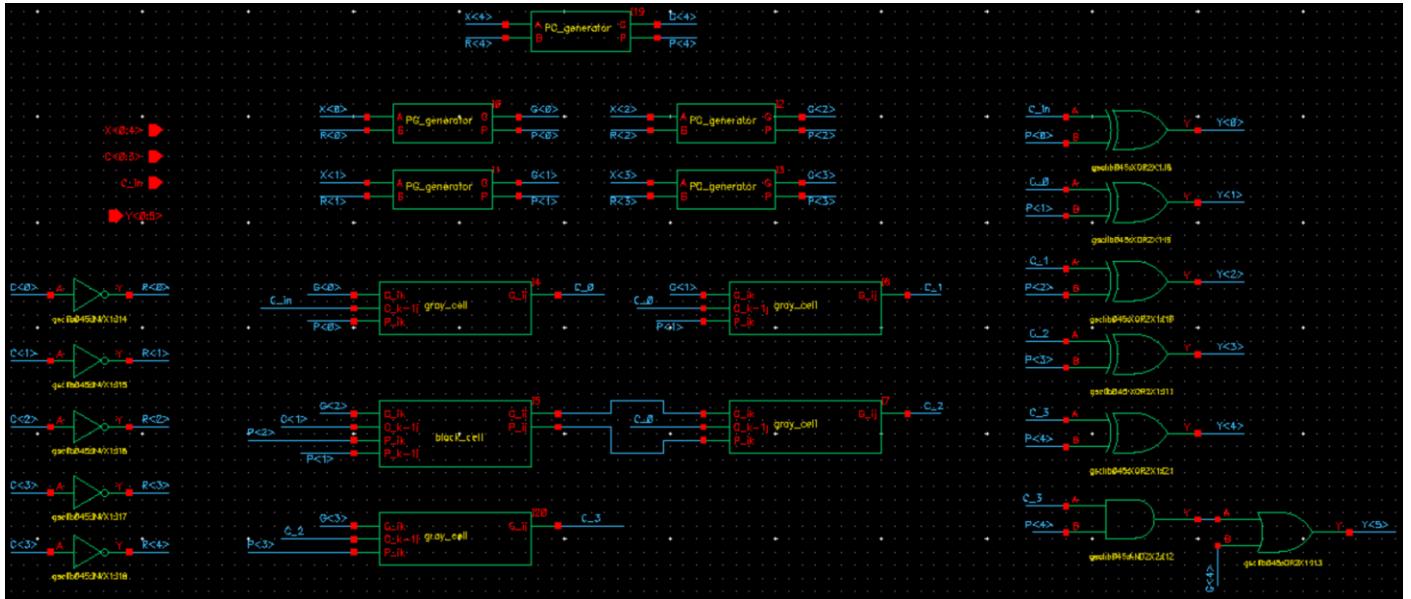
- **5_bit_register**



- **6_bit_register**

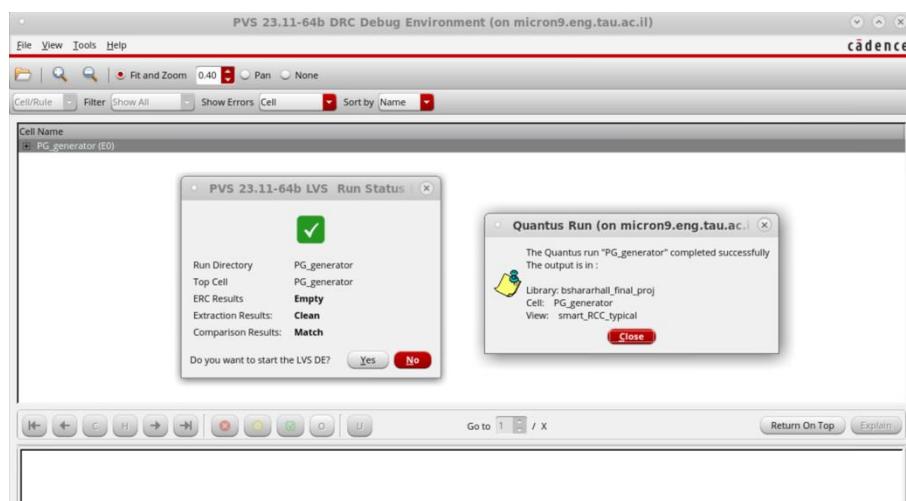
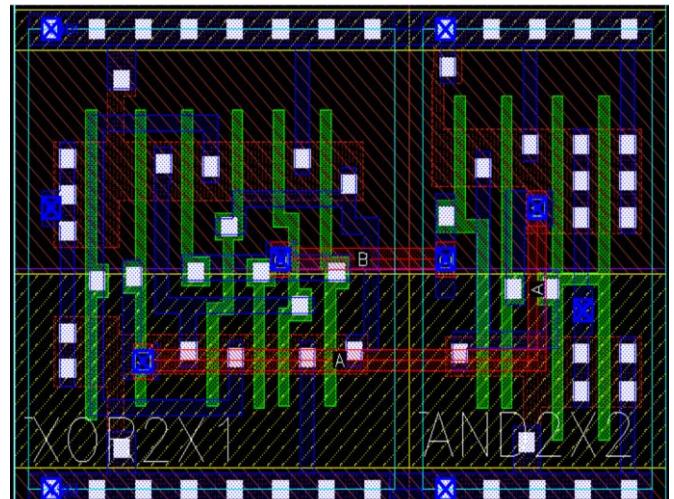
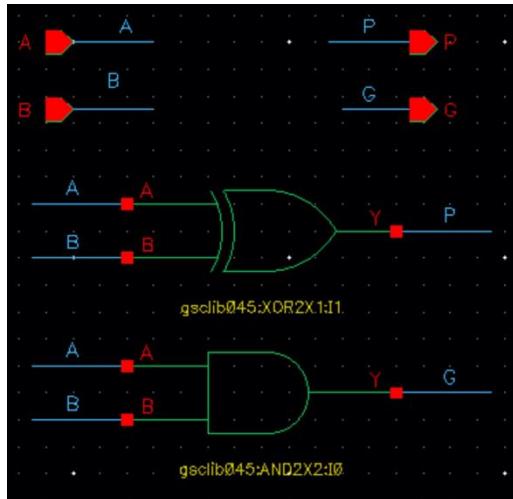


- **5_bit_adder_sub**

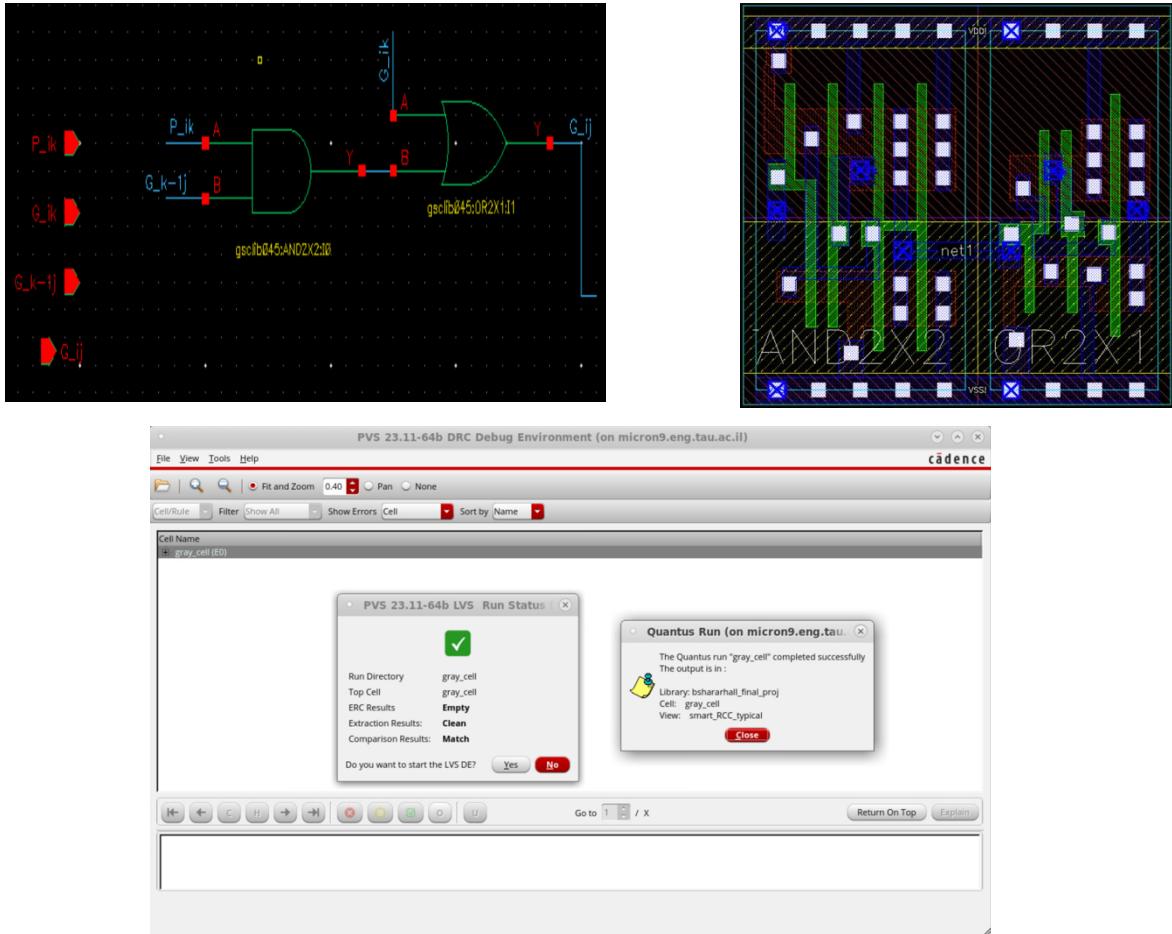


For the 4_bit_adder, we designed the layout and successfully passed the DRC, LVS, and QRS tests, as shown below.

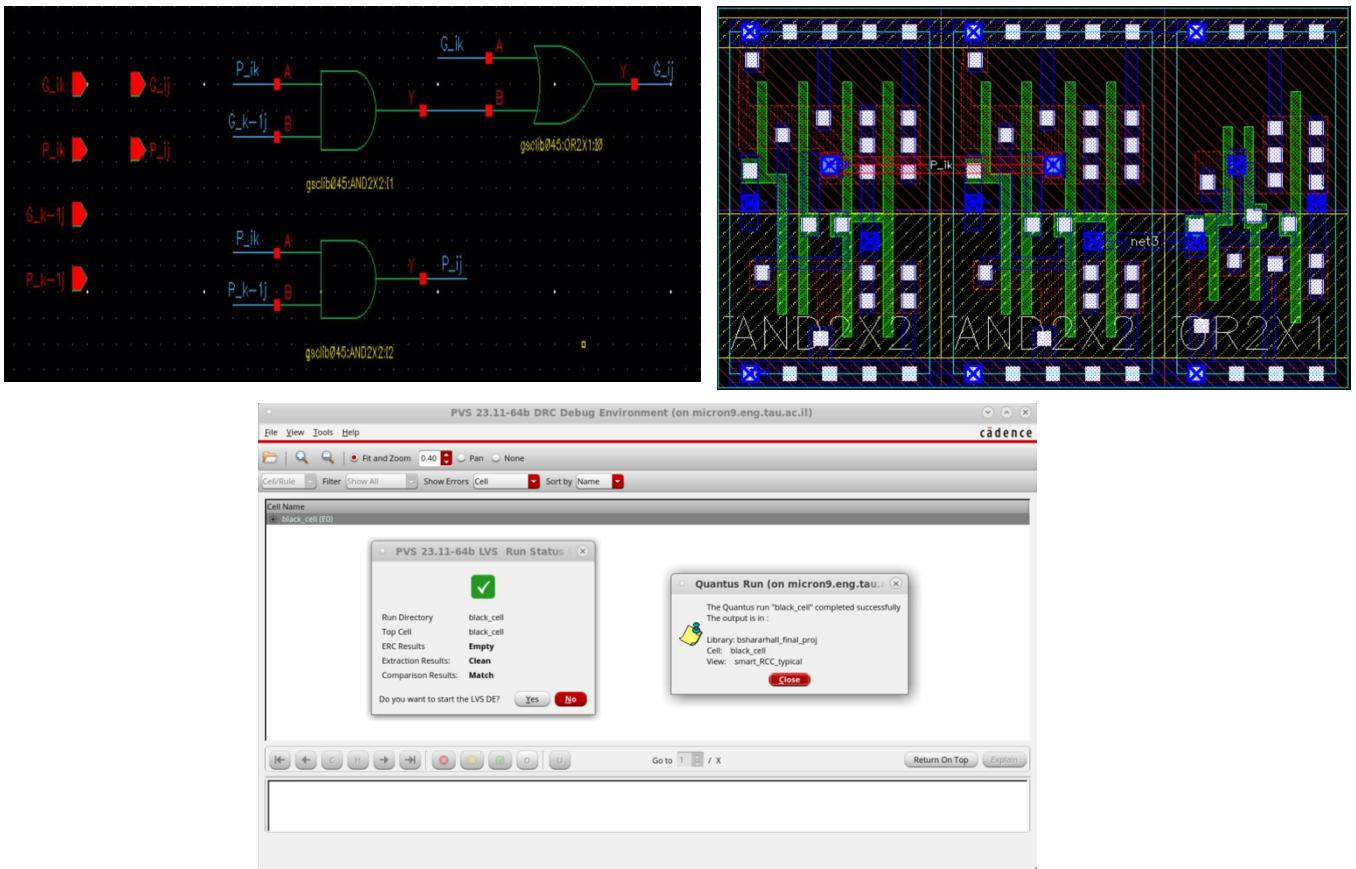
- **PG_generator**



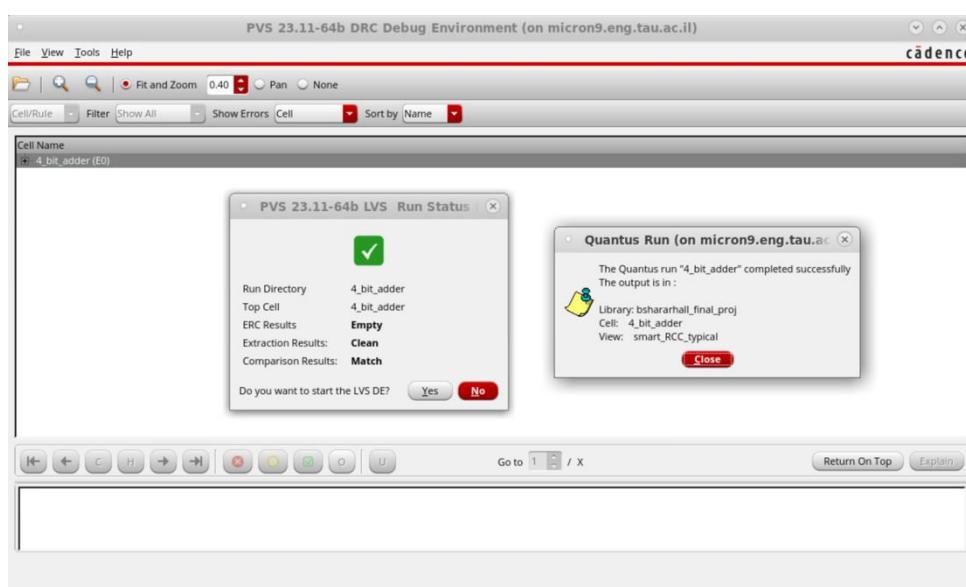
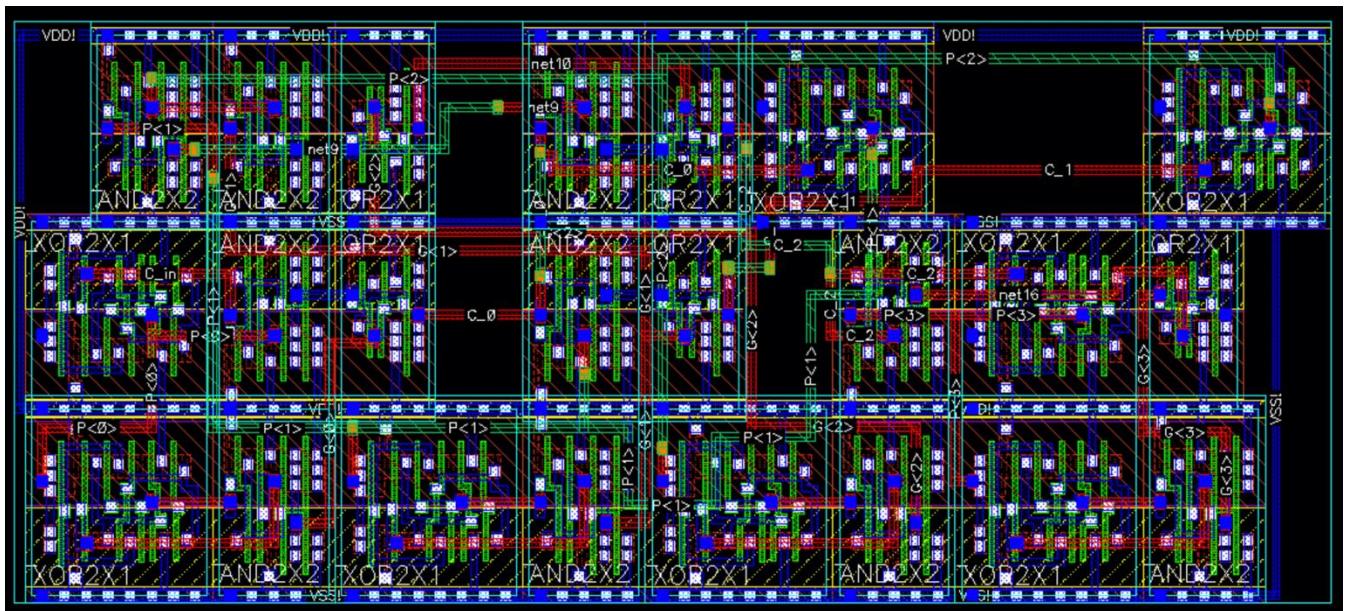
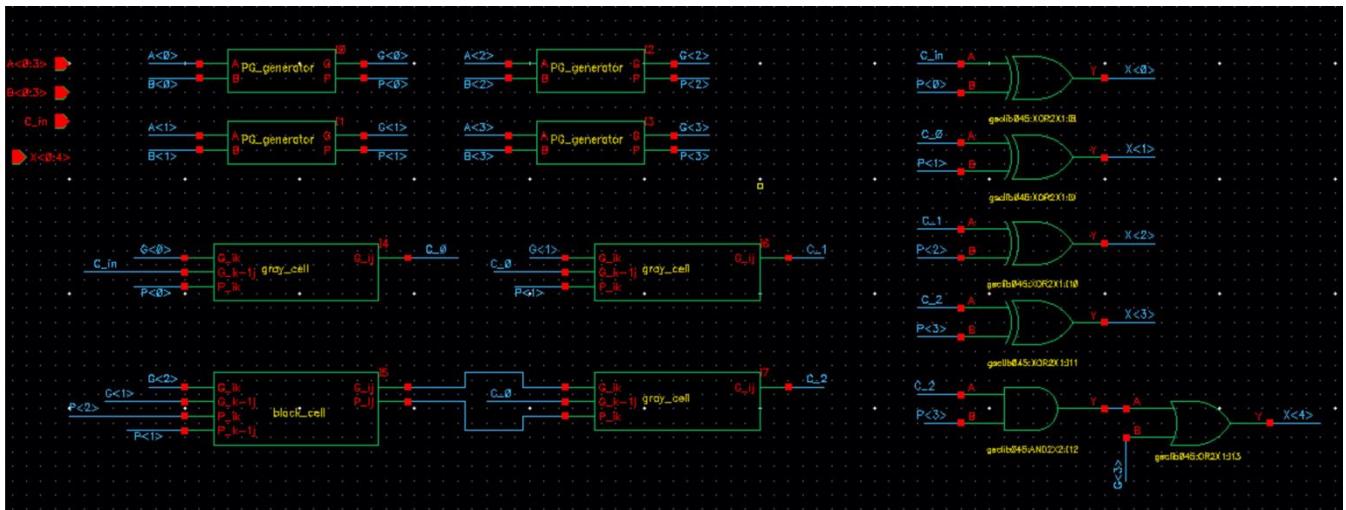
- **Gray_cell**



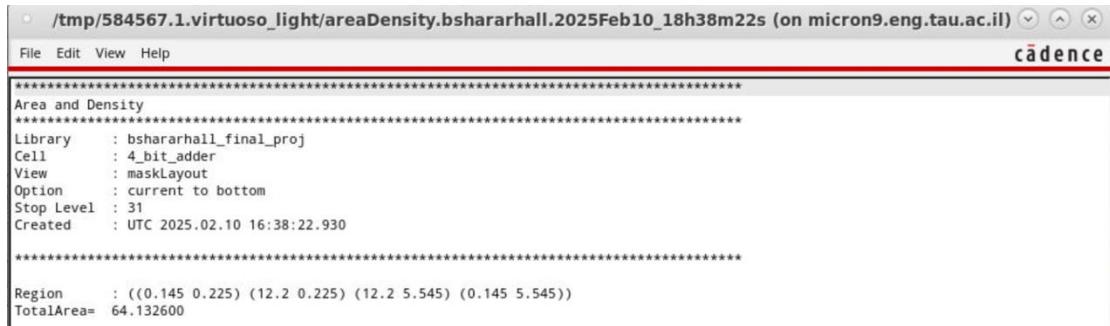
- **Black_cell**



- 4_bit_adder



In the planning stage, we estimated the total area of the 4_bit_adder to be $56.088[\mu\text{m}^2]$. After designing the layout, the total area obtained was $64.1326[\mu\text{m}^2]$, as shown in the measurement below. Thus, we have met the requirement of 150% of the estimated total area.



```

/tmp/584567.1.virtuoso_light/areaDensity.bshararhall.2025Feb10_18h38m22s (on micron9.eng.tau.ac.il) ◻ □ ×
File Edit View Help
*****
***** Area and Density *****
*****
Library : bshararhall_final_proj
Cell   : 4_bit_adder
View    : maskLayout
Option  : current to bottom
Stop Level : 31
Created : UTC 2025.02.10 16:38:22.930
*****
Region  : ((0.145 0.225) (12.2 0.225) (12.2 5.545) (0.145 5.545))
TotalArea= 64.132600

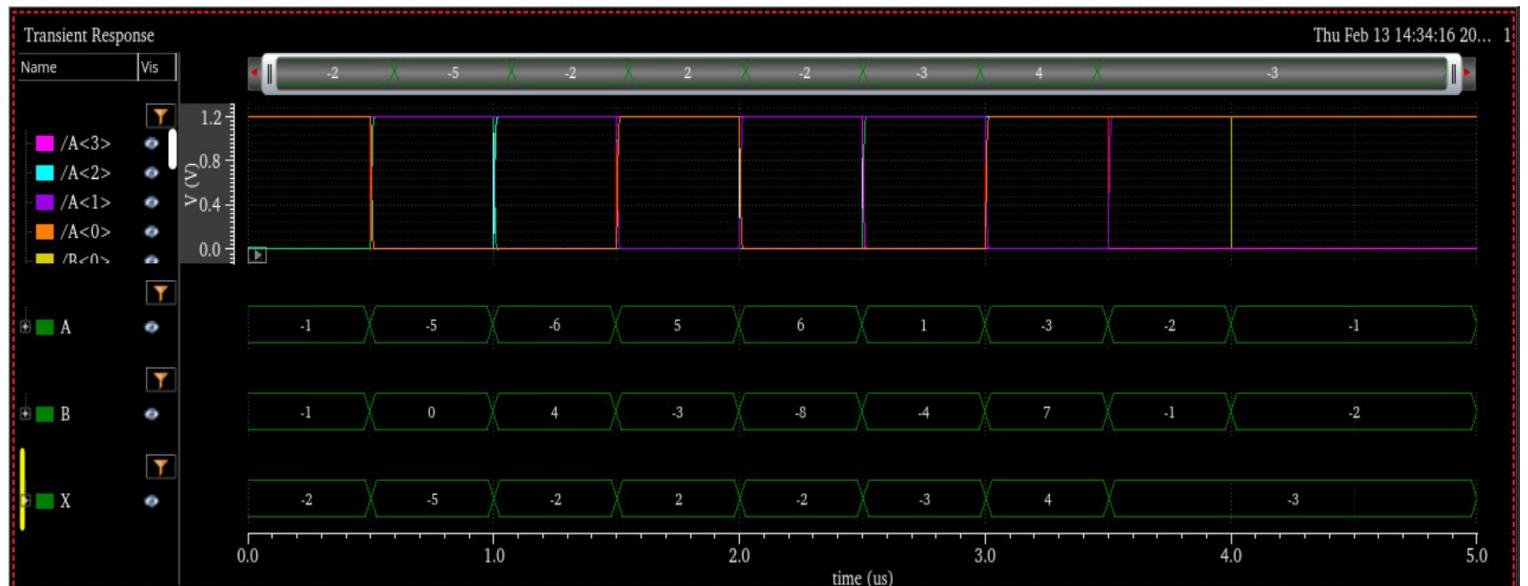
```

The additional area is necessary for wiring, routing, and power separation to prevent electrical interference and optimize functionality. While minimizing extra space is possible, certain design rules (DRC, LVS) must be followed to ensure proper spacing and prevent electromagnetic issues. Reducing the total area enhances production efficiency, increases chip yield per wafer, and improves power consumption and performance.

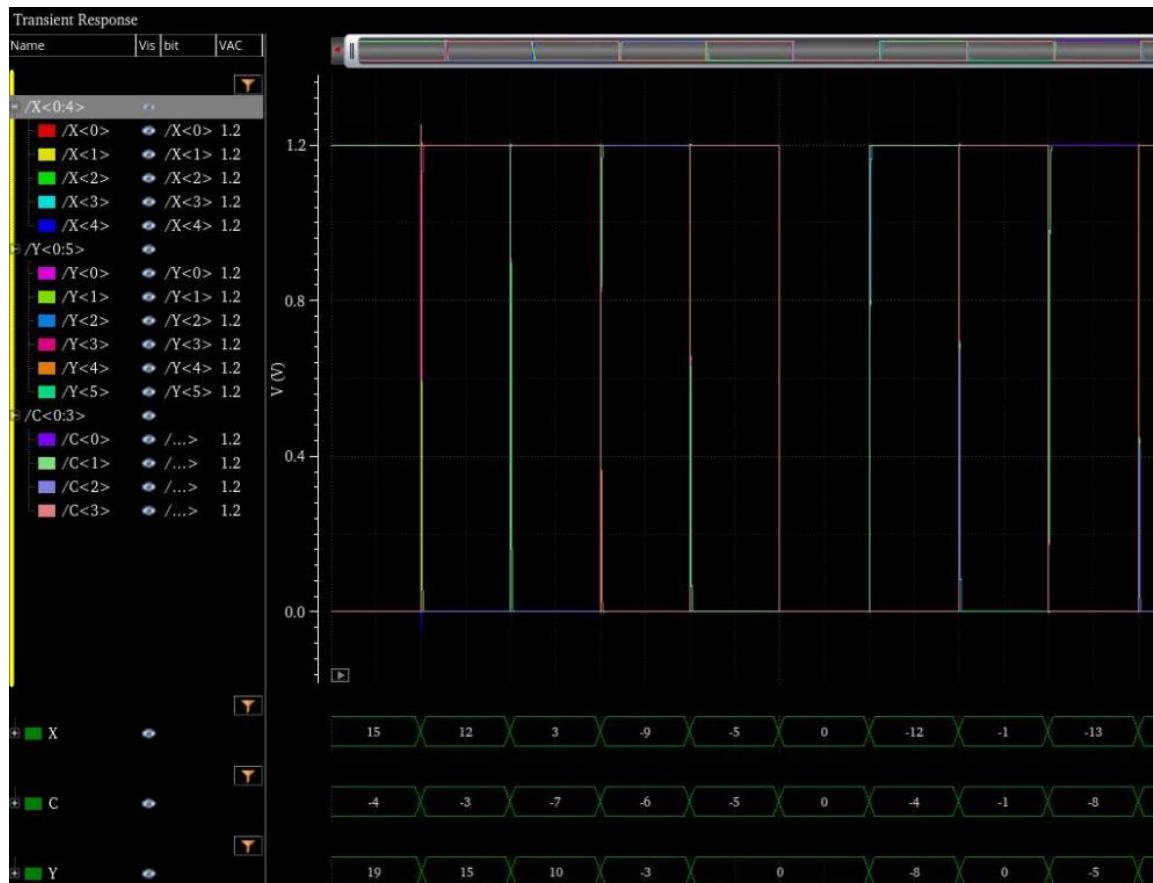
Simulation Results

We have simulated the functionality of both the adder and the subtractor to ensure they function properly.

Adder's simulation results:

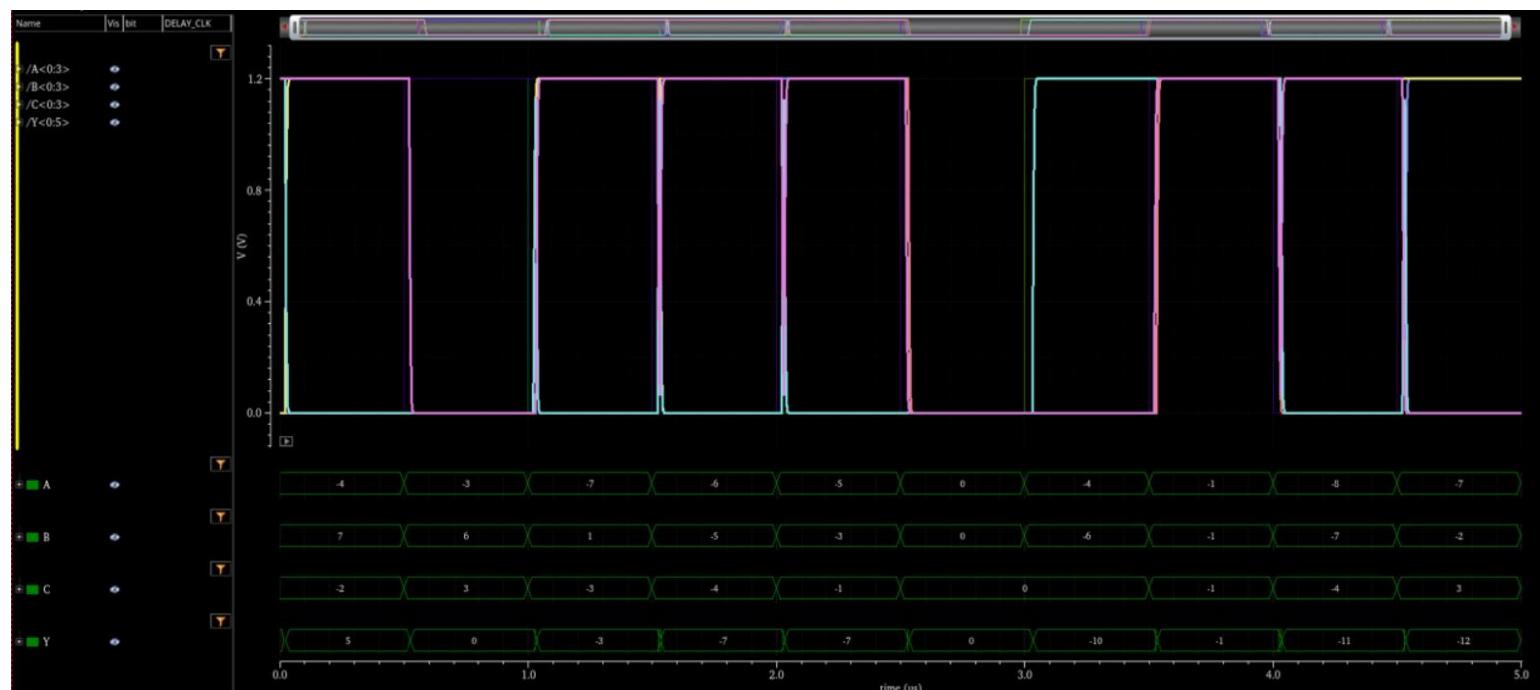


Subtractor's simulation results:



It's seen that both the adder and the subtractor fulfill their expected functionality.

The entire unit's simulation results:



Calculation of the clock's max frequency

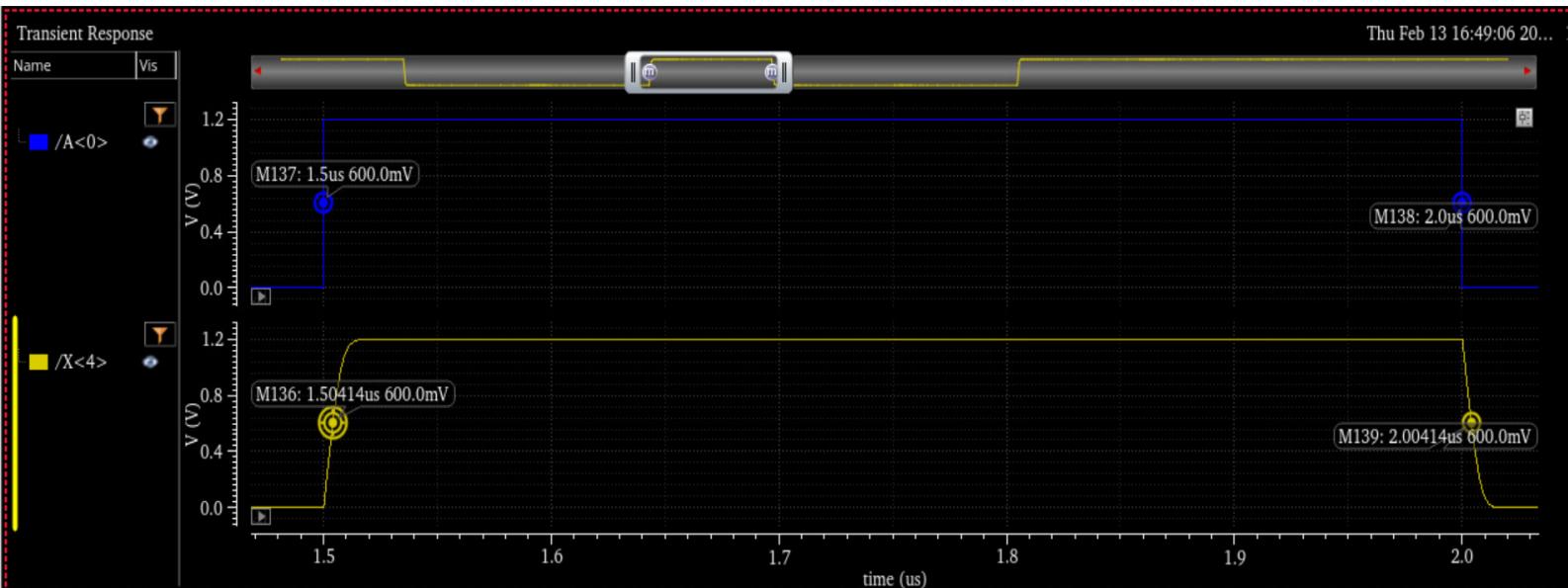
Now, we'd like to find our critical path's delay on our way to ensure our clock is operating withing the limitations of the clock cycle period and frequency.

Finding the delay of the critical path (VDD=1.2V)

We have simulated both the adder and the subtractor to find who has the higher delay, as they are the logic blocks that connect our synchronous components in the circuit.

We've calculated the t_{PLH} and t_{PHL} of the adder and the subtractor via simulations.

For the adder:



It's visible from the simulation that:

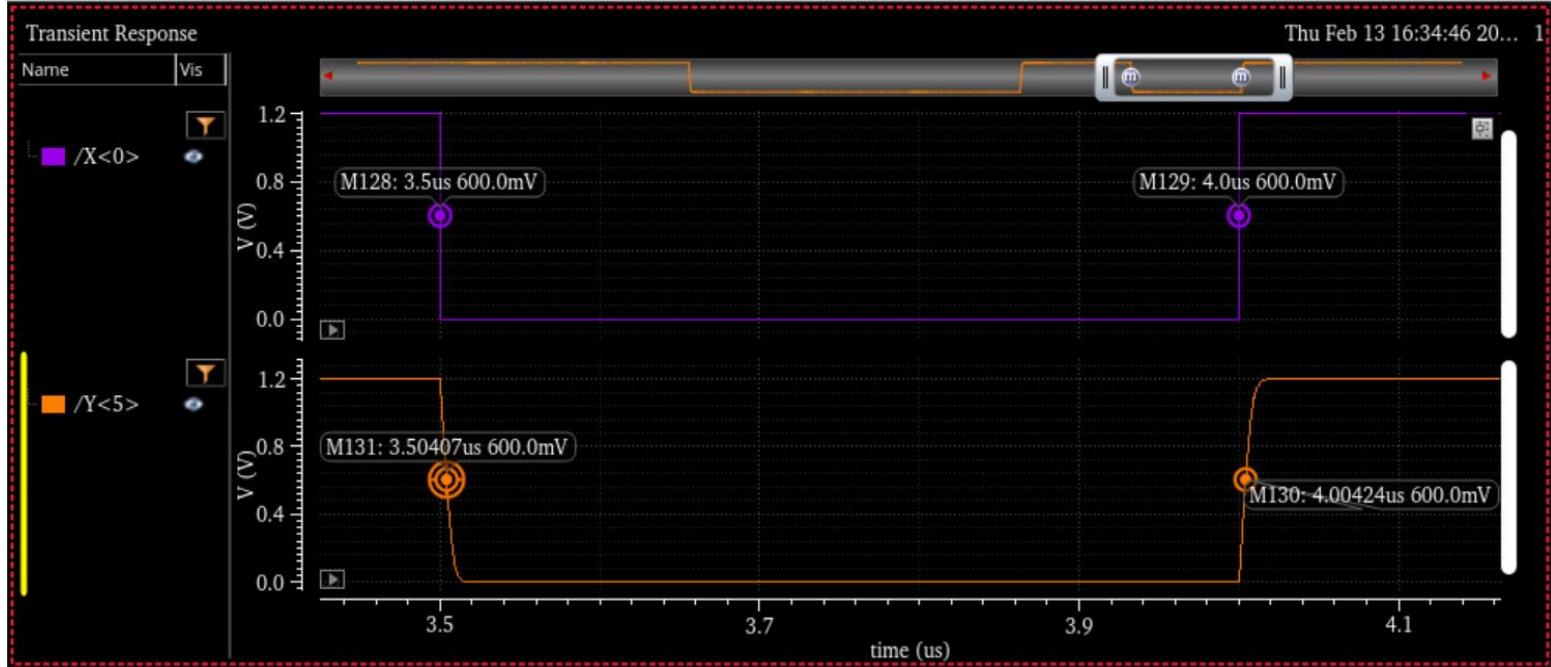
$$t_{PLH} = 4.14 \text{ [ns]}$$

$$t_{PHL} = 4.14 \text{ [ns]}$$

Hence:

$$T_{crit-adder} = 4.14 \text{ [ns]}$$

As for the subtractor:



From the simulation:

$$t_{PLH} = 4.24 \text{ [ns]}$$

$$t_{PHL} = 4.07 \text{ [ns]}$$

Hence the critical time would be the higher delay:

$$T_{crit-subtractor} = 4.24 \text{ [ns]}$$

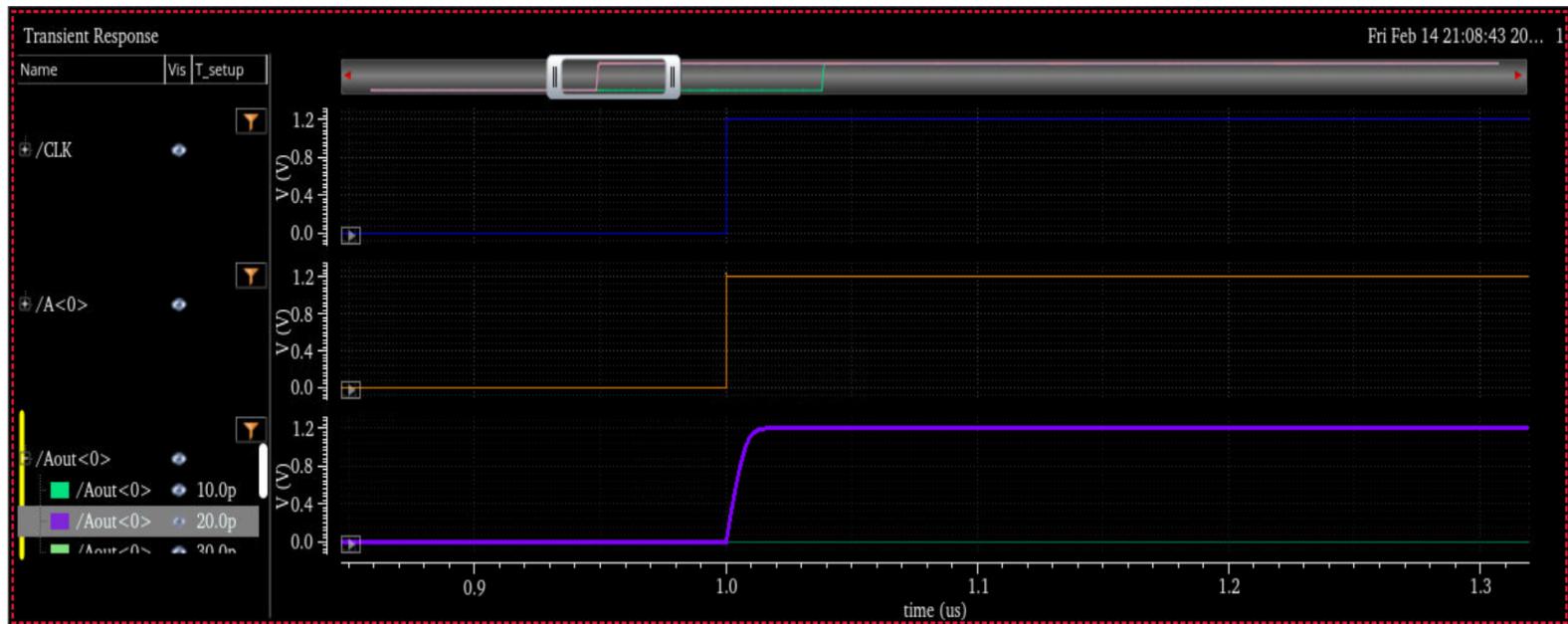
As we expected, the critical path of the subtractor has a longer delay, and thus it will be the critical path of our entire circuit.

Finding t_{setup}

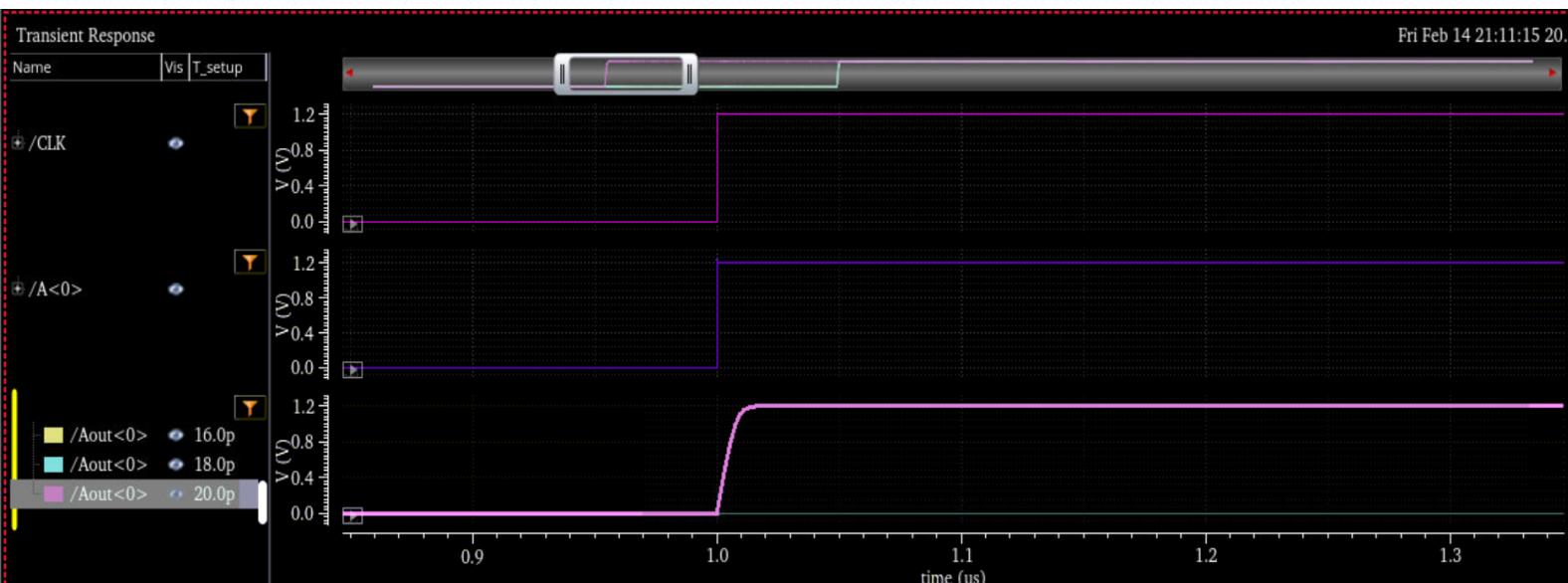
In order to calculate the setup time we'll measure different values for the setup time as we expect to see our desired value at the output each time. We'll define our bit to rise to '1' after 1 [us], and our clock to rise after 1[us]+T_setup, which we will sweep over.

We'll examine our output for each value of T_setup, and once we find the lowest value of T_setup that our output receives its expected value, we'll progress to a lower resolution until we find our final setup time.

First we'll sweep for $10ps < t_{setup} < 50ps$, with each step of 10ps:



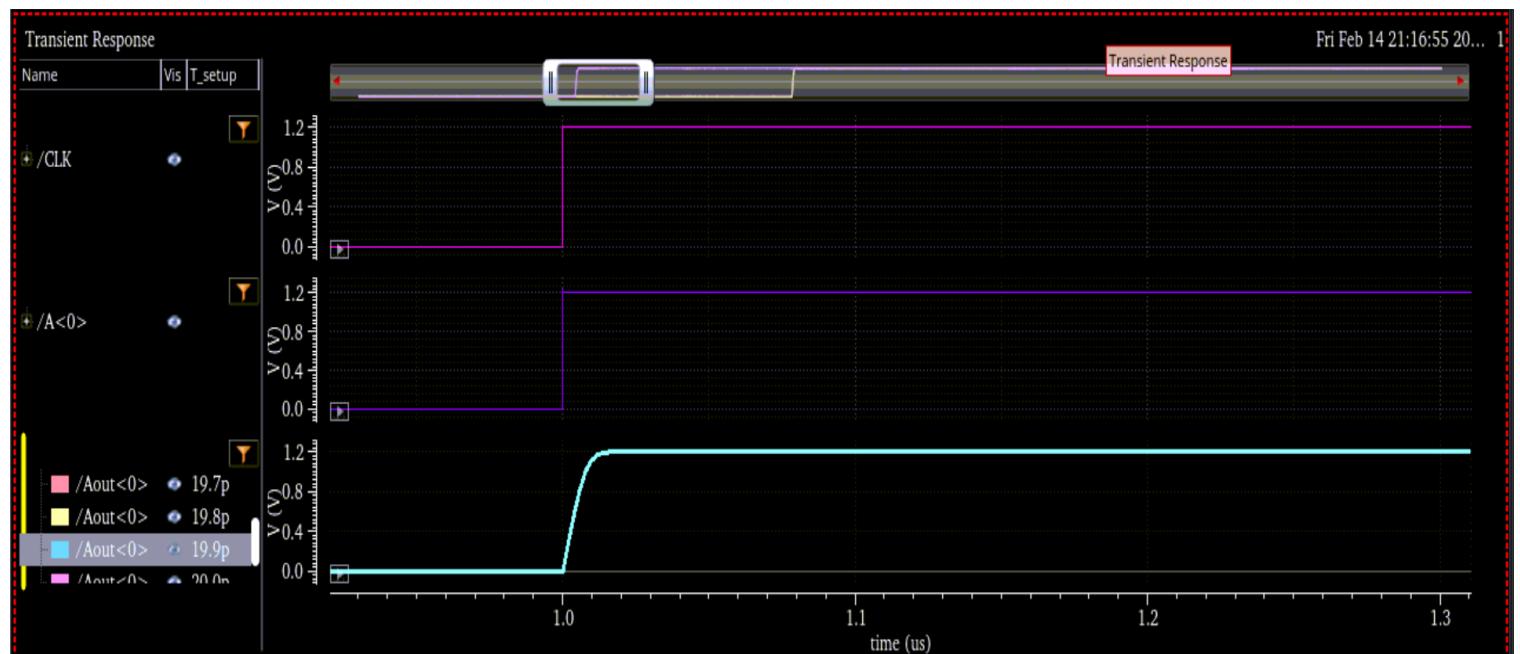
We've got the expected value for a setup time of 20ps, so we're moving on to sweep over $10ps < t_{setup} < 20ps$, with each step of 2ps:



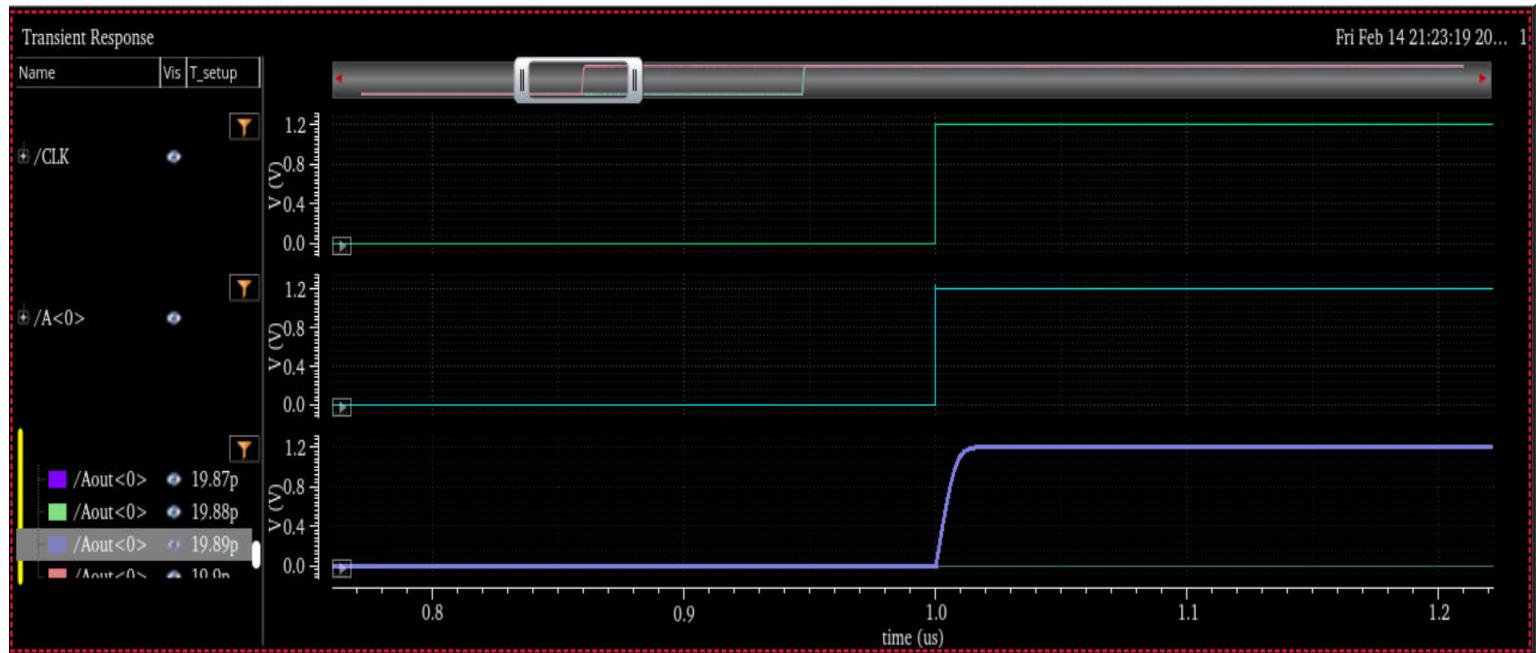
Similarly, our next step will be sweeping over $18ps < t_{setup} < 20ps$, with each step of 0.5ps:



For the next stage, we'll sweep over $19.5ps < t_{setup} < 20ps$ with each step of 0.1ps:



As for the result we've got, we'll do a final sweep over $19.8\text{ps} < t_{\text{setup}} < 19.9\text{ps}$ with steps of size 0.01ps, to obtain our final result:

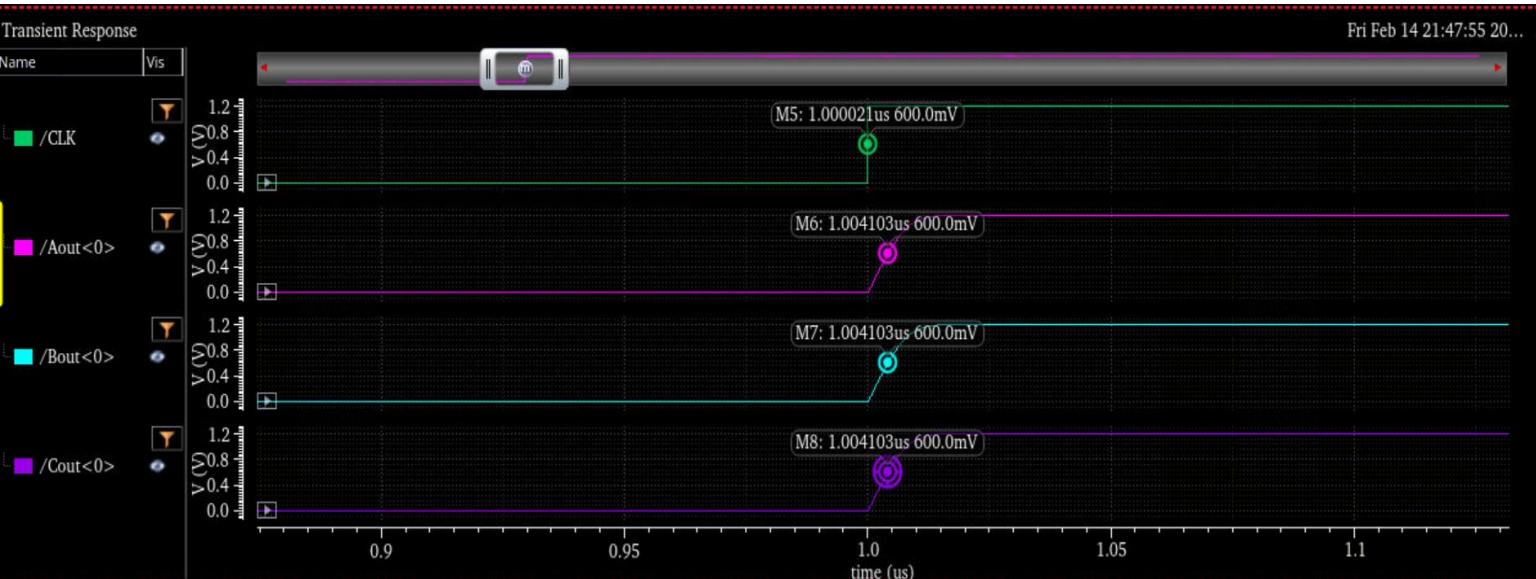


And it's seen from the simulation that the final result is $t_{\text{setup}} = 19.89 \text{ [ps]}$.

TCQ delay (Clock to Q)

We'll want to calculate the TCQ for our design, as it's the final value we need to obtain the appropriate clock frequency.

We'll simulate and observe at the delay of all the registers (3,4, and 5-bit) and choose the maximal delay to be our TCQ for the circuit:



As expected, the delay of all the registers is the same, as they are all constructed of D-FFs connected in parallel. Thus our TCQ would be:

$$t_{CQ} = 4.082 \text{ [ns]}$$

Now, we can calculate our maximal clock frequency by calculating the minimal clock period:

$$T_{clock-min} > t_{setup} + t_{CQ} + t_{logic-crit} = 19.89[\text{ps}] + 4.082[\text{ns}] + 4.24[\text{ns}] = 8.341[\text{ns}]$$

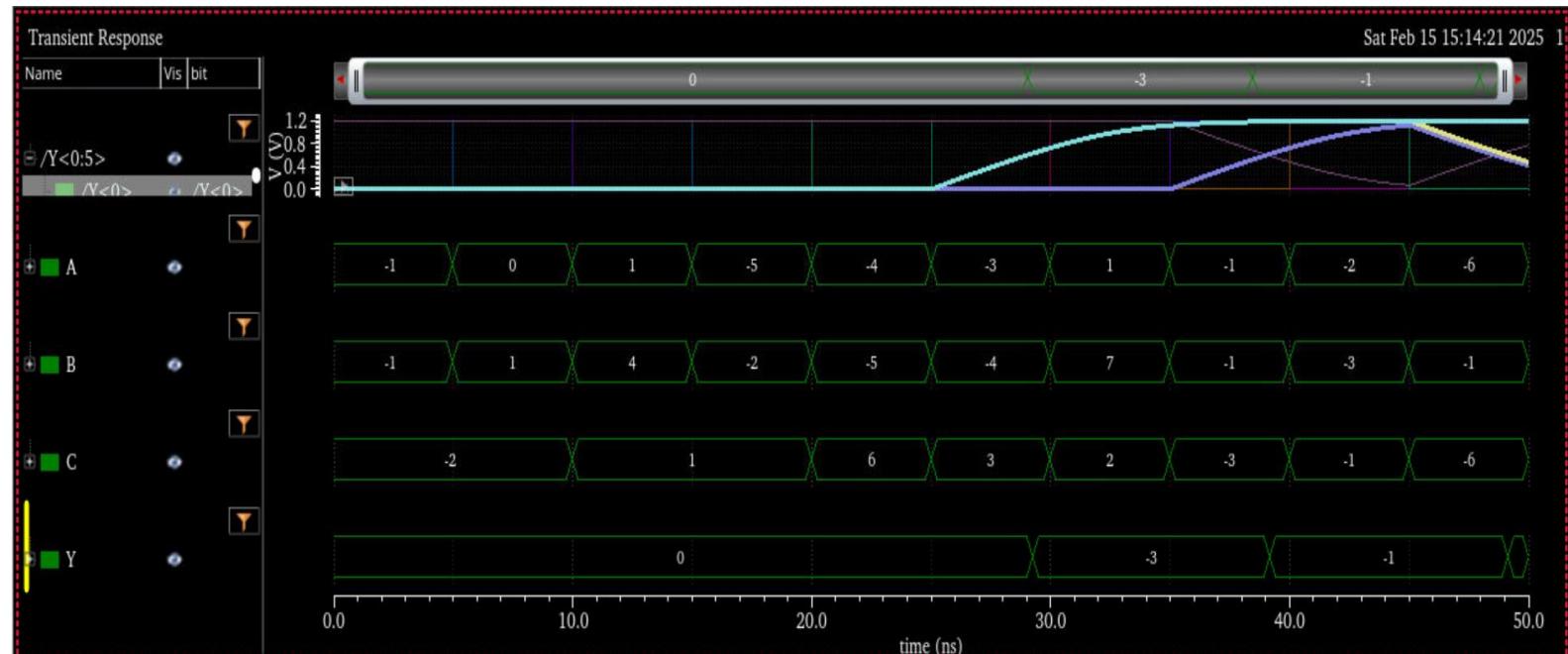
$$f_{max} = \frac{1}{T_{min}} = 0.11987 \text{ GHz}$$

Pass/Fail Test

We have shown that the circuit passes and works appropriately for a clock cycle that is within the range that we have found.

We will now lower our clock cycle period (raise clock frequency) significantly to be below our low boundary for 1.2V, and show via a simulation that the circuit does not operate as intended with this clock cycle

For a clock cycle period that is outside of the range:



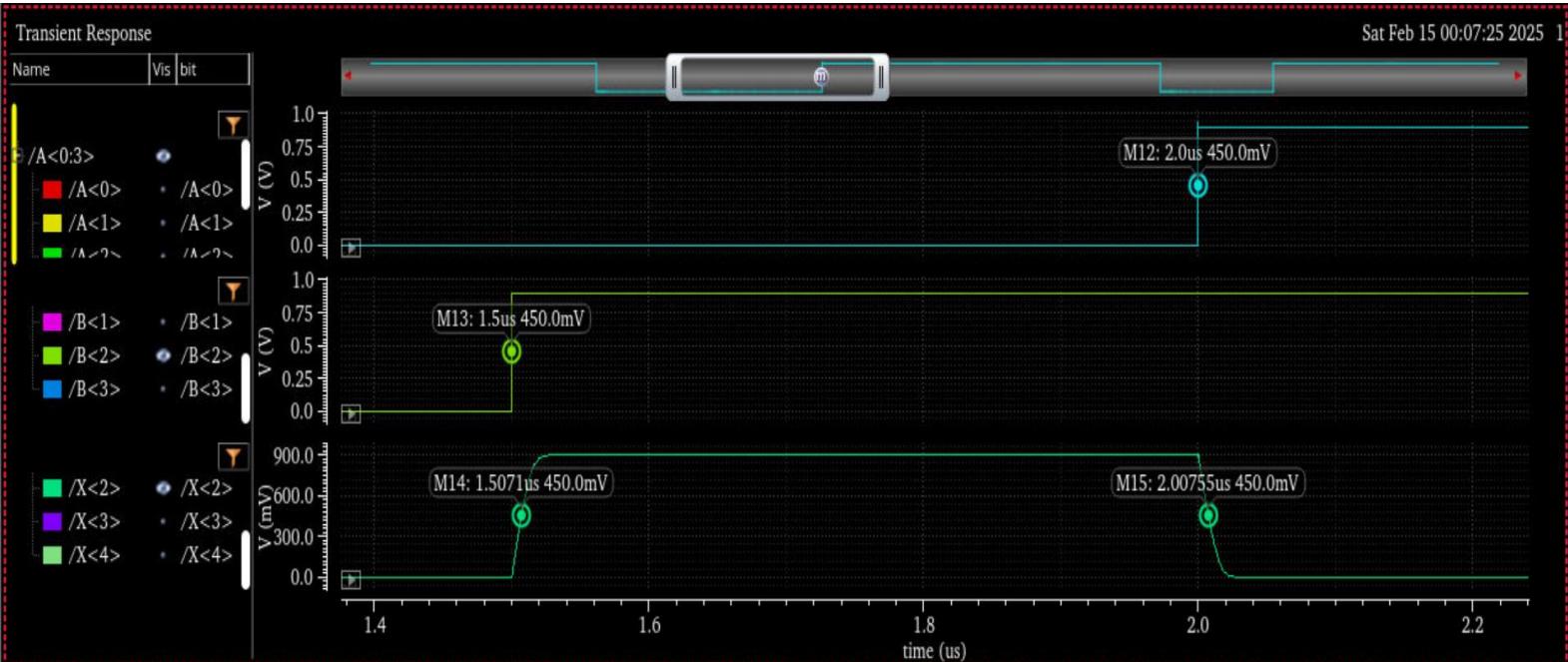
It's seen from the simulation that the circuit does not operate as intended since it's operating in a clock frequency that's higher than the maximal that we've found.

Finding the delay of the critical path (VDD=0.9V)

Similar to the process we've done just now, we'd like to go over for a supply voltage of 0.9V.

The results for t_{PLH} and t_{PHL} of the adder and the subtractor:

For the adder:



$$t_{PLH} = 7.1 \text{ [ns]}$$

$$t_{PHL} = 7.55 \text{ [ns]}$$

Hence the critical delay would be the higher delay:

$$T_{crit-adder} = 7.55 \text{ [ns]}$$

For the subtractor:



$$t_{PLH} = 7.22 \text{ [ns]}$$

$$t_{PHL} = 7.58 \text{ [ns]}$$

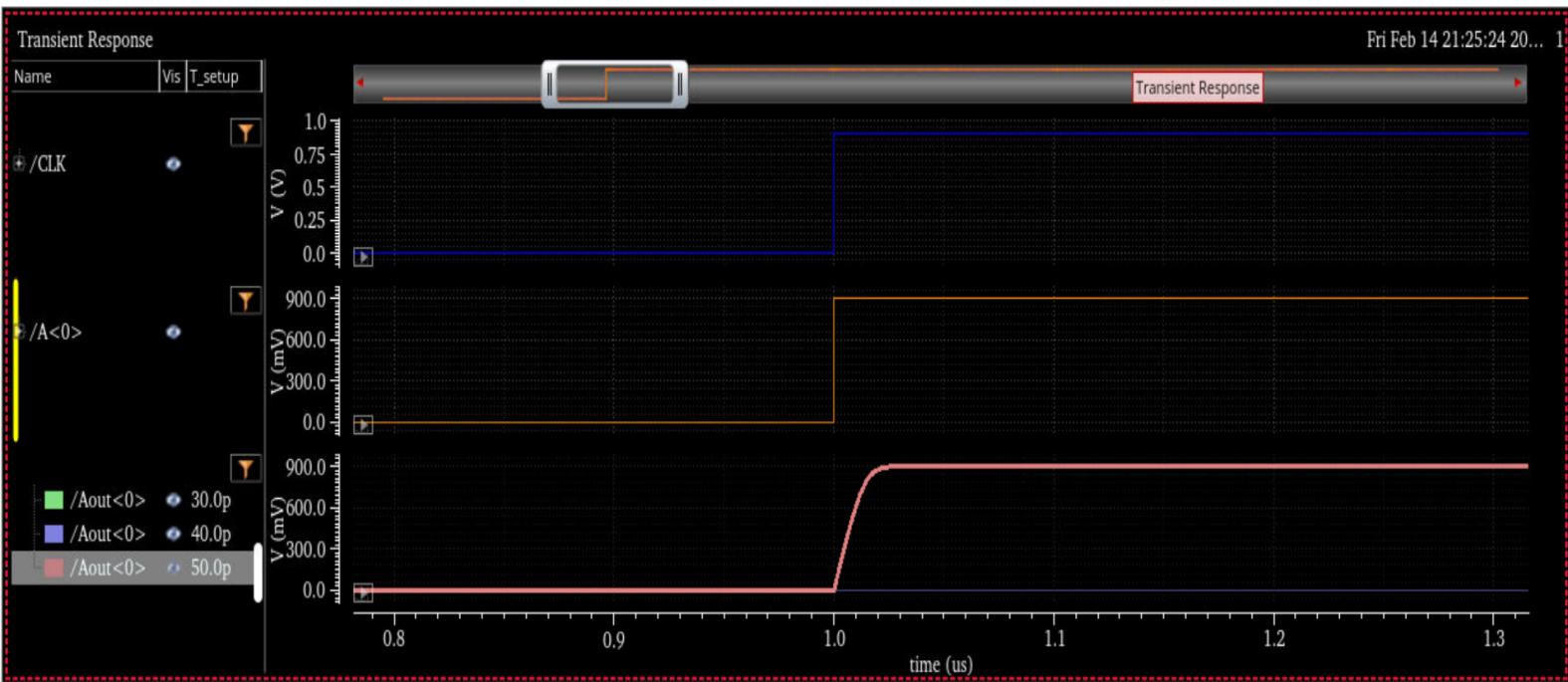
And so the critical delay would be the higher delay:

$$T_{crit-subtractor} = 7.58 \text{ [ns]}$$

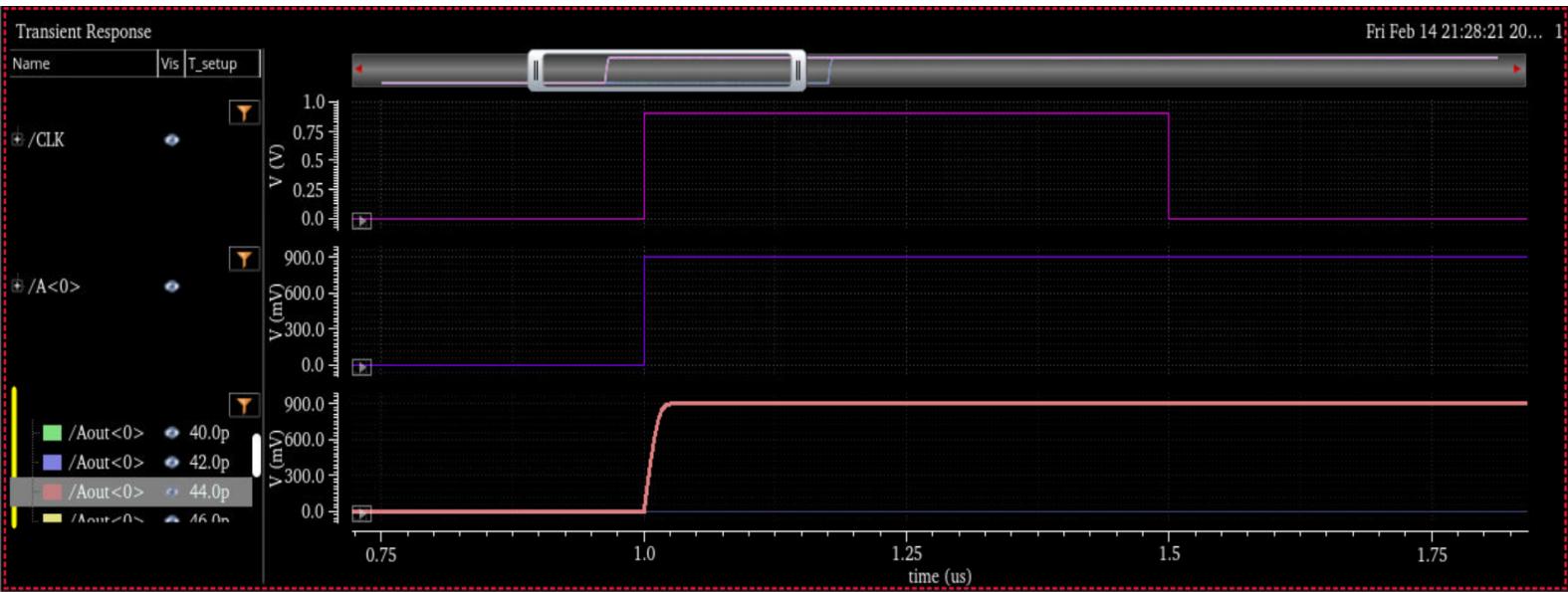
Once again, as expected, the critical path of the subtractor has the longer delay, and will be considered our critical path for the circuit.

Finding t_{setup}

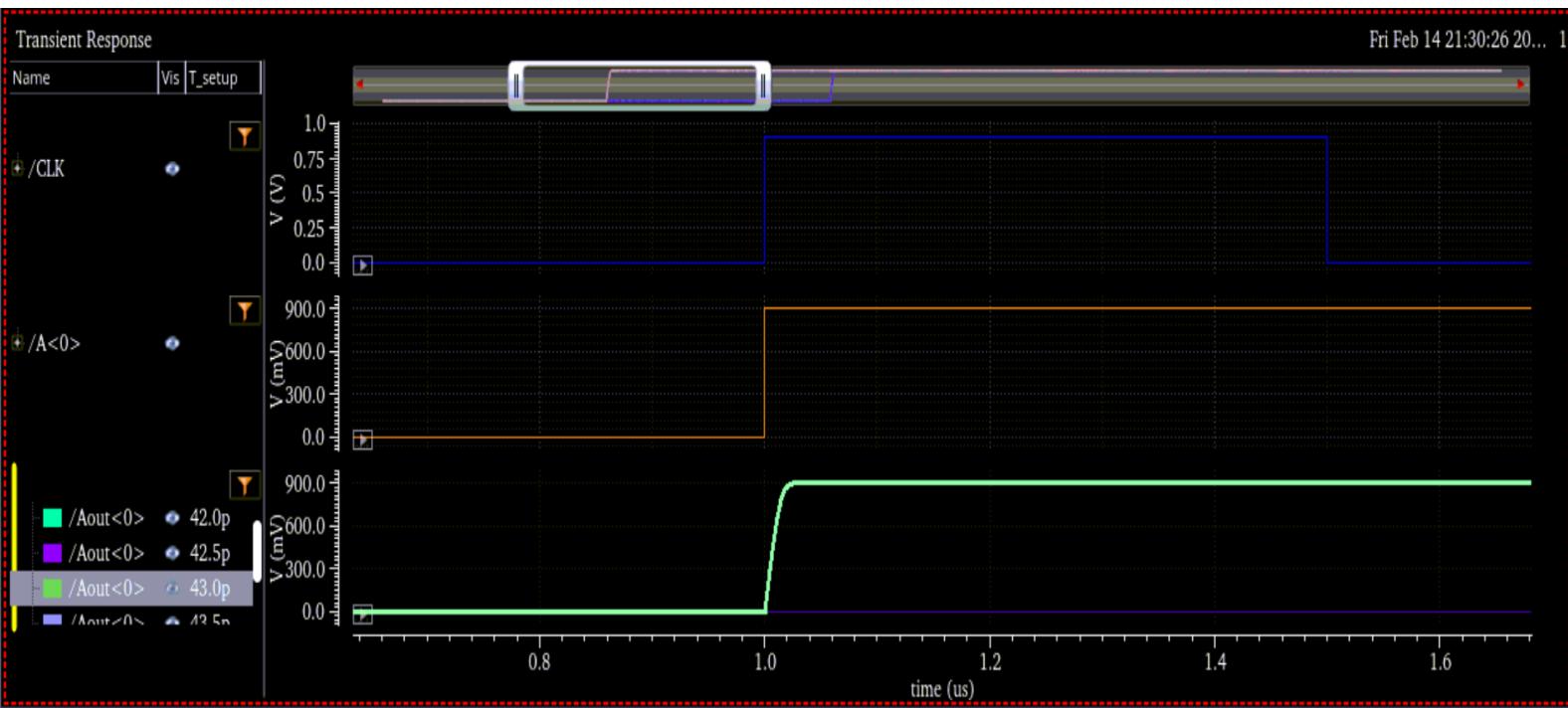
As we did before, we'll start by sweeping over $10ps < t_{setup} < 50ps$ with steps of 10ps:



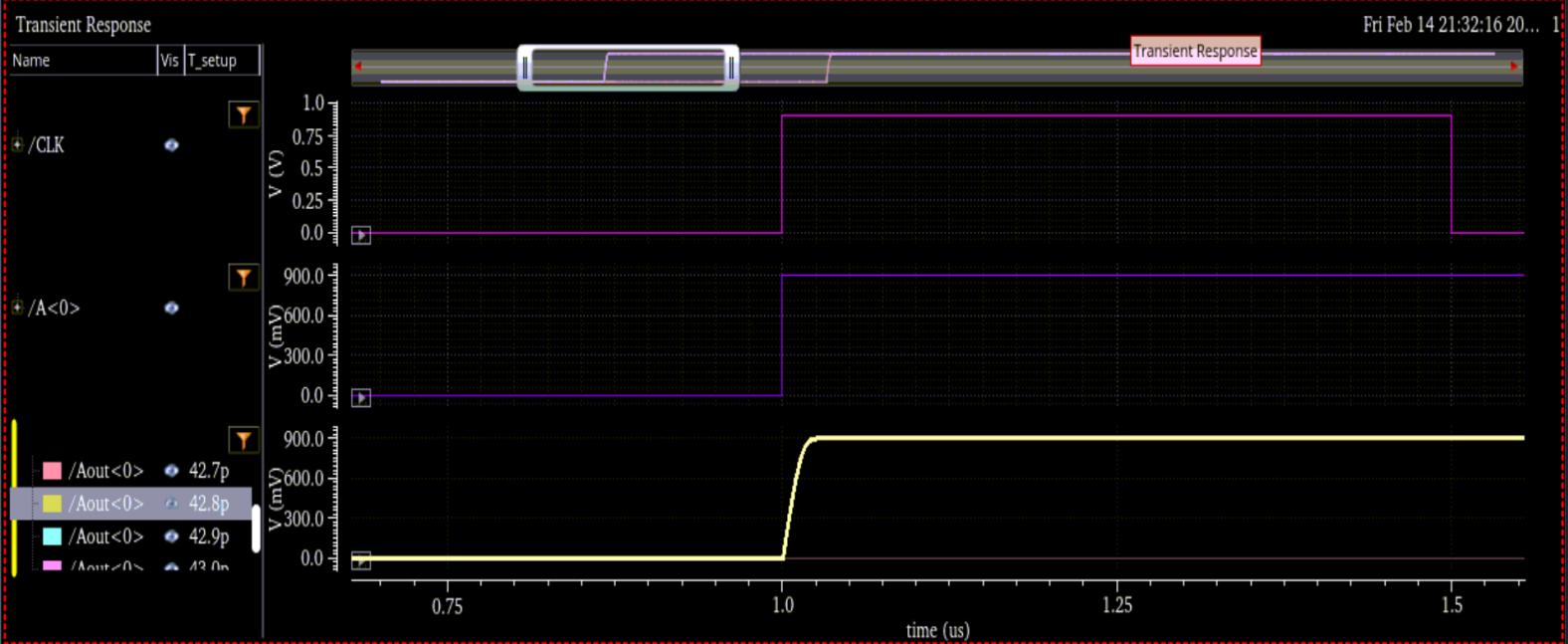
Our next step, if so, will be sweeping over $40ps < t_{setup} < 50ps$ with steps of 2ps:



For the next step, we'll sweep over $42ps < t_{setup} < 44ps$ with steps of $0.5ps$:



Now, we'll proceed to sweep over $42.5ps < t_{setup} < 43ps$ with steps of $0.1ps$:



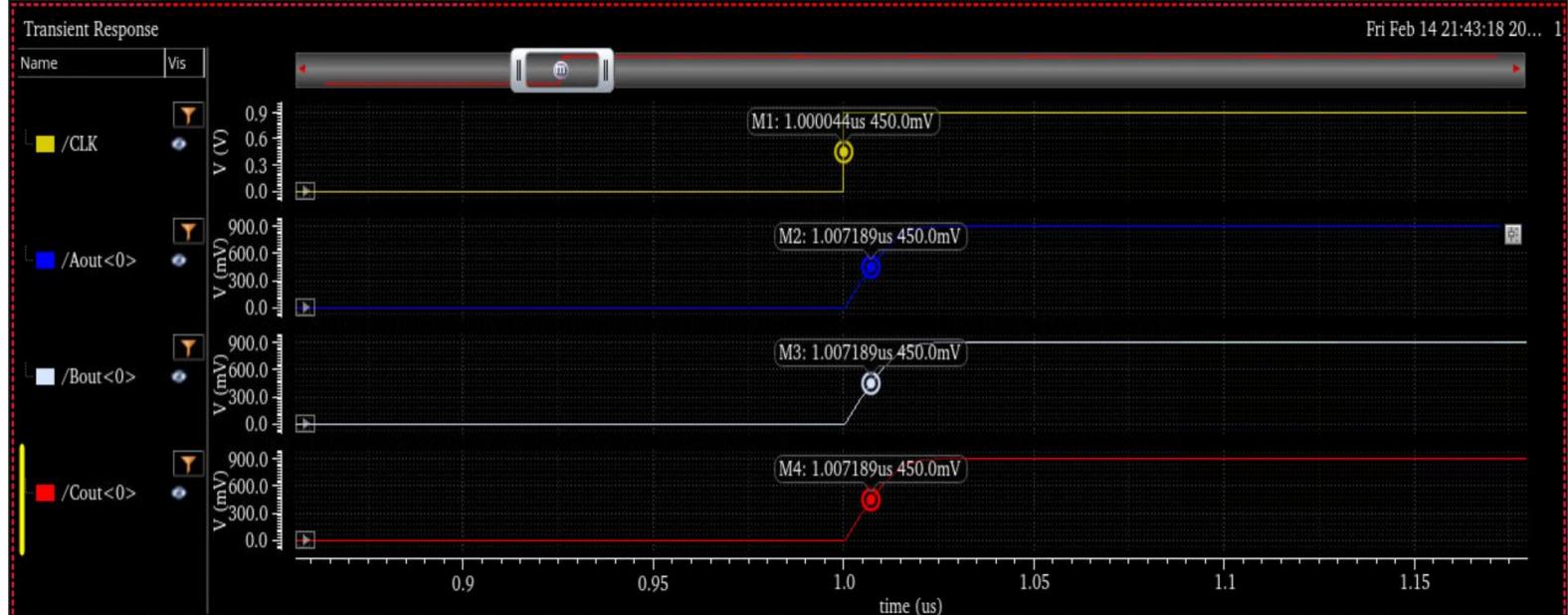
To obtain our final result, we'll sweep over $42.7\text{ps} < t_{\text{setup}} < 42.8\text{ps}$ with steps of 0.01ps :



As seen in the simulation, our final result is $t_{\text{setup}} = 42.8 \text{ [ps]}$.

TCQ delay (Clock to Q)

We'll once again want to calculate our TCQ for the circuit, so we'll do it in a similar way—we will measure the delay of all of our registers, and choose the maximal delay of the three to be our TCQ:



Once again, as expected, the delays of all the registers are exactly the same, and our TCQ of the circuit will be $t_{CQ} = 7.145 [ns]$.

Therefore, our minimal clock period would be:

$$T_{Clock-min} > t_{setup} + t_{CQ} + t_{logic-crit} = 42.8[ps] + 7.145[ns] + 7.58[ns] = 14.767[ns]$$

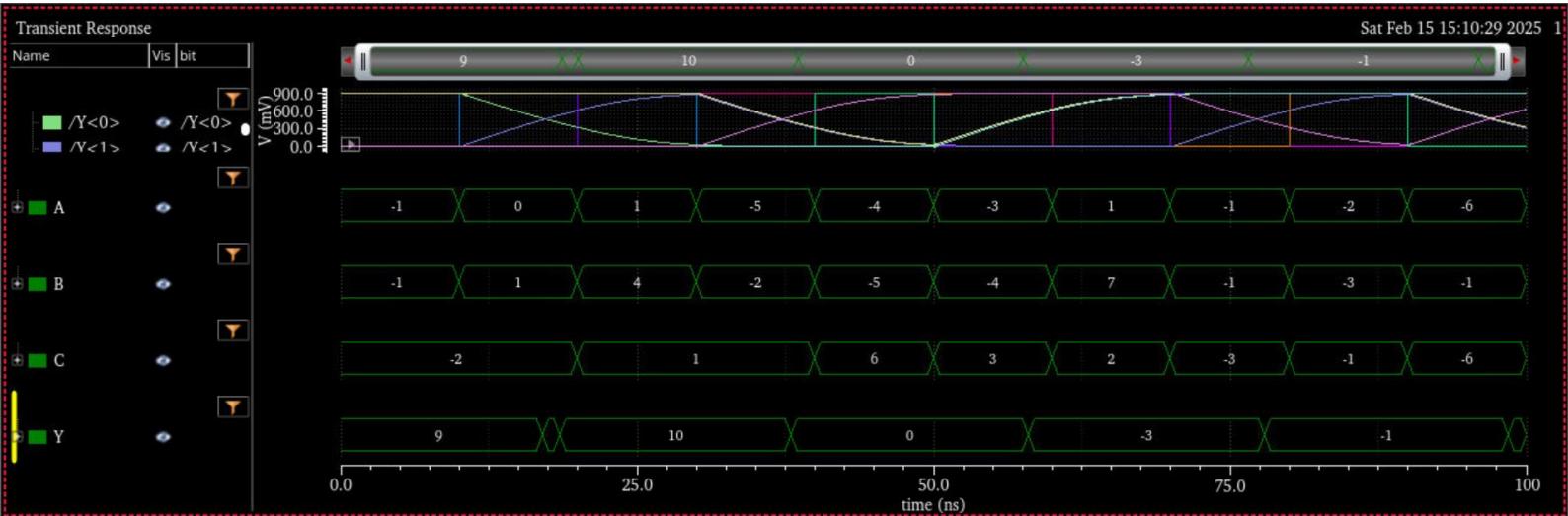
$$f_{max} = \frac{1}{T_{min}} = 0.06771 \text{ GHz}$$

Pass/Fail Test

We have shown that the circuit passes and works appropriately for a clock cycle that is within the range that we have found. Working with a significantly long clock cycle (We used a relatively long clock cycle period when simulating) period answers for both criteria for the clock cycle period boundary, for both supply voltages, and passes for both of them (0.9V and 1.2V).

We will now once again lower our clock cycle period significantly to be below our low boundary for 0.9V, and show via a simulation that the circuit does not operate as intended with this clock cycle

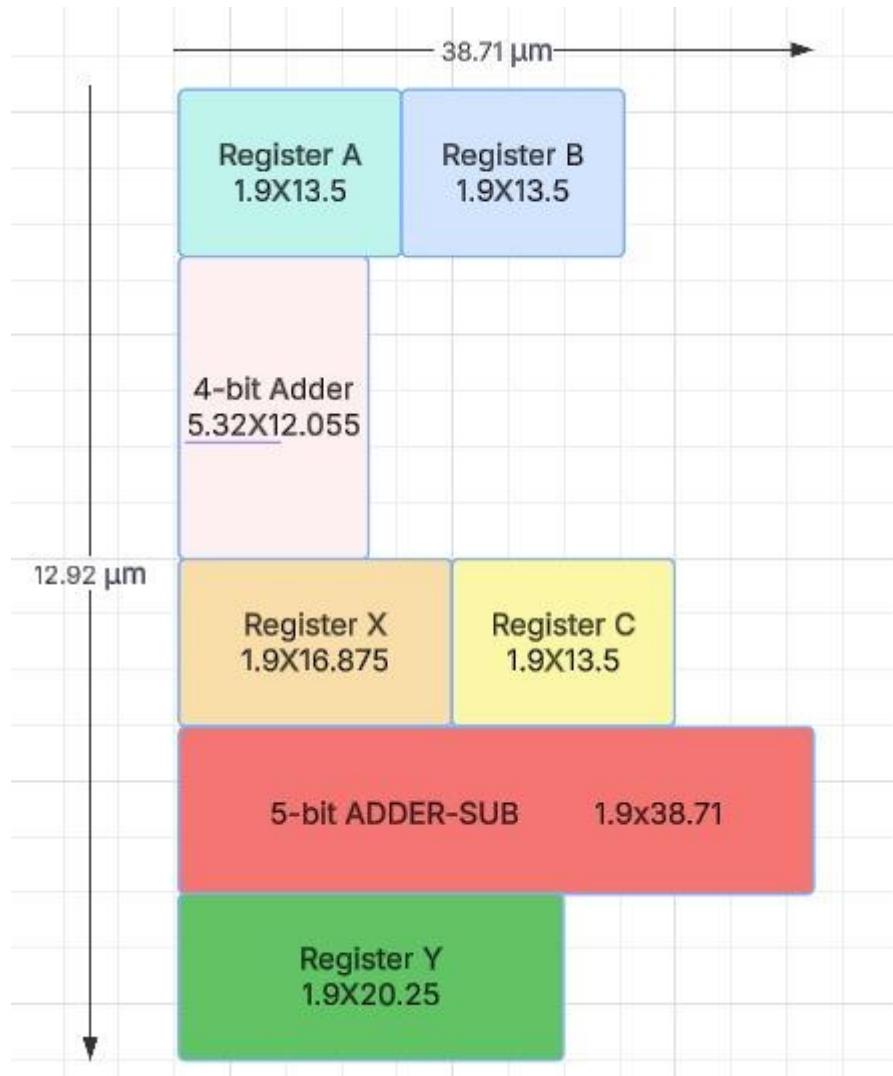
Outside of the range:



We can observe mild glitches and stutters in the output as a result of a clock cycle period which is lower than the minimum that we have found. Thus, we conclude that the circuit fails when operating with clock cycle periods outside of our range.

A detailed floorplan of our final circuit

Below is a detailed floorplan of our circuit. We used the sizes of the 4-bit adder which we have designed the layout of, and used the sizes of the rest of the components from our planning stage (since we didn't design a layout for them):



The overall area of our circuit (according to this sized floorplan) will be:

$$12.92 \text{ } [\mu\text{m}] * 38.71 \text{ } [\mu\text{m}] = 500.13 \text{ } [\mu\text{m}^2]$$

The total area for our circuit turned out to be larger than what we estimated in the planning stage. This could happen due to considerations that weren't made during the planning stage and impacted while designing the layout, such as extra space that had to be left to pass the DRC test and actual space that could be used for the metal wires, the active layers and the poly lines. We can assure that the more layouts we'd build for the components of the circuit-the more these aspects would be expressed and the more they will expand our circuit's total area.

