

שאלה פת
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Computer Organization - Quiz 3

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- Please write your ID number on top of the first page.
- The assignment consists of **one** question with **three** subsections.
- Write the solutions in the space provided below the relevant section. If you need extra space, please use the back of the page.
- Please make sure your answers are clear and readable.

Question

Consider the following sequence of instructions in MIPS assembly language:

| Label | Instruction | Comment |
|--------|-------------------------|---|
| | lw \$t0, 0(\$s0) | # load word from memory into \$t0 |
| | add \$t1, \$t0, \$s1 | # add \$t0 and \$s1, store result in \$t1 |
| | sw \$t1, 4(\$s0) | # store word in memory |
| | beq \$t1, \$zero, Label | # branch to Label if \$t1 is equal to 0 |
| | add \$t2, \$t1, \$t3 | # add \$t1 and \$t3, store result in \$t2 |
| | sw \$t2, 8(\$s0) | # store word in memory |
| Label: | | |
| | ... | # other instructions |

Based on the code above, answer the questions given below.

| clk cycle | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|-------------|-----|----|----|----|-----|----|-----|-----|-----|-----|-----|----|
| Instruction | lw | IF | ID | EX | MEM | WB | | | | | | |
| | add | | IF | ID | EX | EX | MEM | WB | | | | |
| | sw | | | IF | ID | ID | EX | MEM | WB | | | |
| | beq | | | | IF | IF | ID | EX | MEM | WB | | |
| | add | | | | | | IF | ID | EX | MEM | WB | |
| | sw | | | | | | | IF | ID | EX | MEM | WB |

1. Identify and describe any data hazards that occur in this sequence of instructions.

• first add - we don't have ft_0 on file
• first sw - we don't have the value we need to store
• beg - ft_1 don't hold yet the value.
• second sw - ft_2 is written on the previous instruction.

2. Identify and describe any control hazards that occur in this sequence of instructions.

• beg - we don't know if we need to jump to label and we're already fetching the next instruction.

3. Suggest **one** technique that could be used to minimize the impact of one of the hazards that you identified in the previous sections on the performance of the MIPS pipeline processor.

• forwarding - on the most of the data hazards were described, forwarding prevents the need to stall (exception is first data hazard)