Lecture1

CORTEX M3/M4 OPERATION | MODES | RIGESTER

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Processor mode:

- **Thread mode:** Used to execute application software. The processor enters Thread mode when it comes out of reset.
- **Handler mode:** The processor returns to Thread mode when it has finished all exception processing.

The privilege levels for software execution:

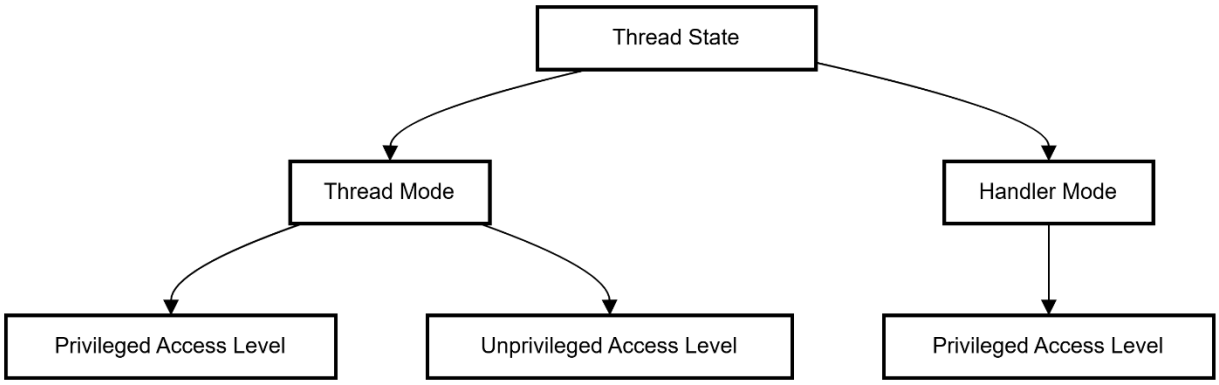
- **Unprivileged:**
  - The software has limited access to the MSR and MRS instructions, and cannot use the CPS instruction
  - The software cannot access the system timer, NVIC, or system control block
  - The software might have restricted access to memory or peripherals.

  “Unprivileged software executes at the unprivileged level”

- **Privileged:**
  - The software can use all the instructions and has access to all resources. Privileged software executes at the privileged level.

“In Thread mode, the CONTROL register controls whether software execution is privileged or unprivileged, In Handler mode, software execution is always privileged.”

Diagram:

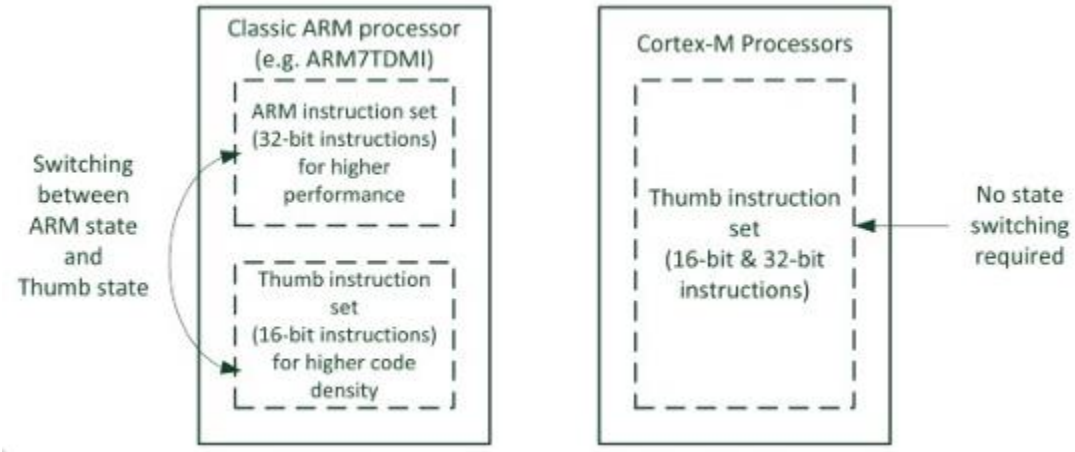


The Difference Between Thumb/ARM/Thumb2:

- **Thumb:**
  - Thumb instructions Set architecture Having Fixed Length 16 Bits.
  - Low performance But Small in Size
  - Used in Cortex M0.

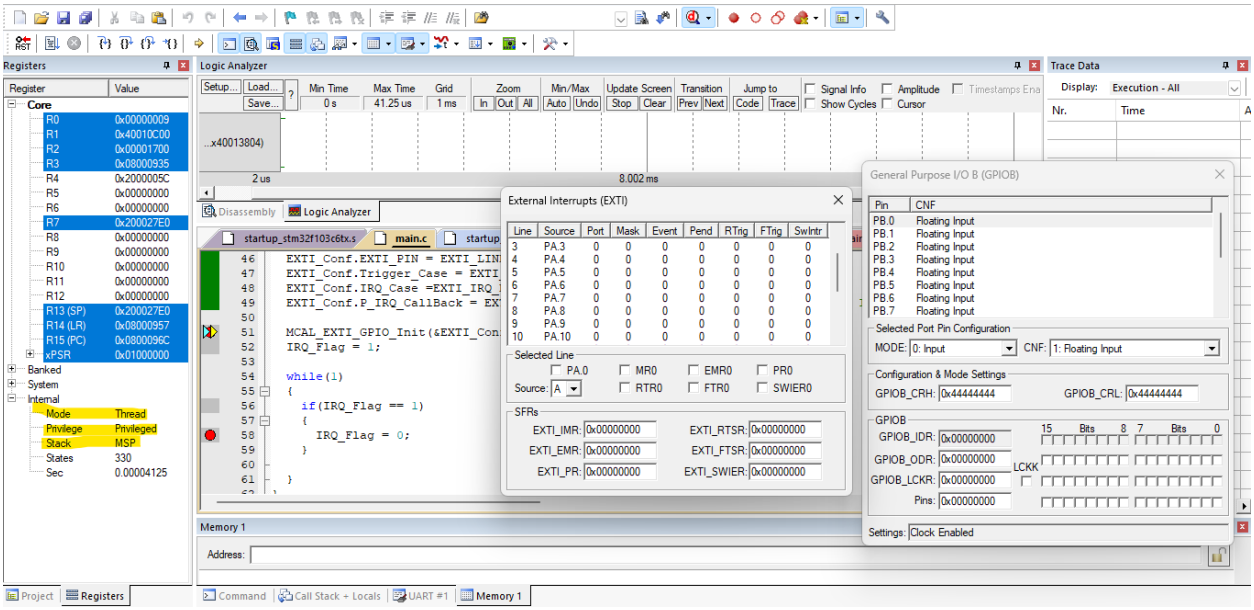
- **ARM:**
  - ARM instructions Set architecture Having Fixed Length 32 Bits.
  - High performance But Big in Size
  - Used in Cortex M1/M2

- **Thumb2:**
  - Thumb2 instructions Set architecture Having Fixed Length 16 & 32 Bits.
  - Best in performance and in size
  - Used in Cortex M3/M4



Output in Keil Micro Vision:

- In Main the operation mode is thread and privileged



- In ISR the operation mode is Handler and privileged