

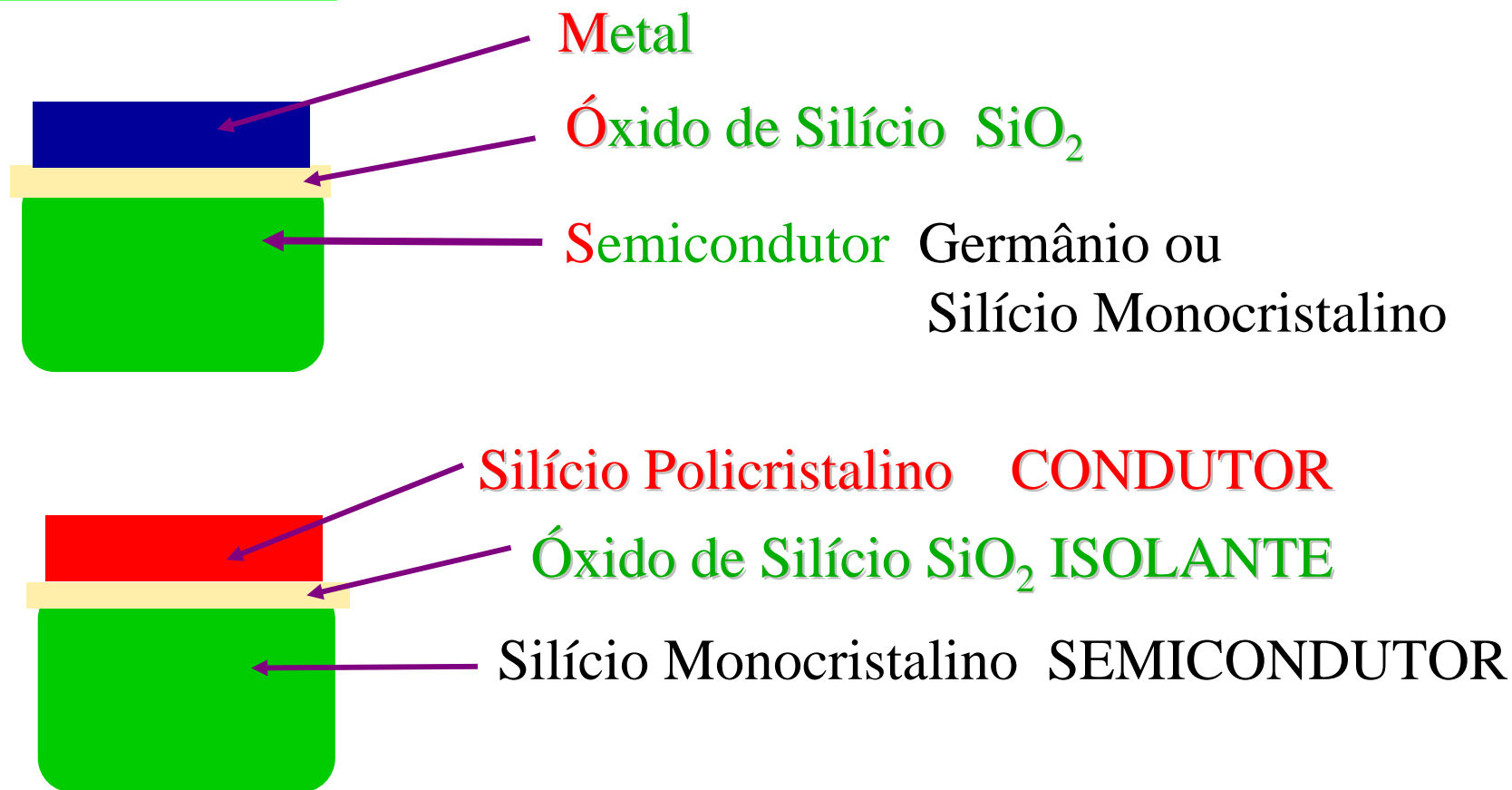
INF01 118

# Técnicas Digitais para Computação

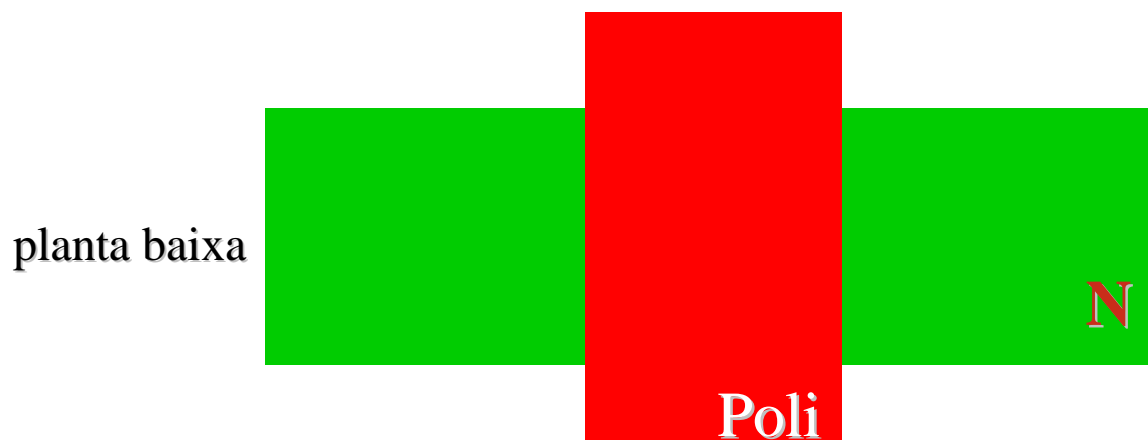
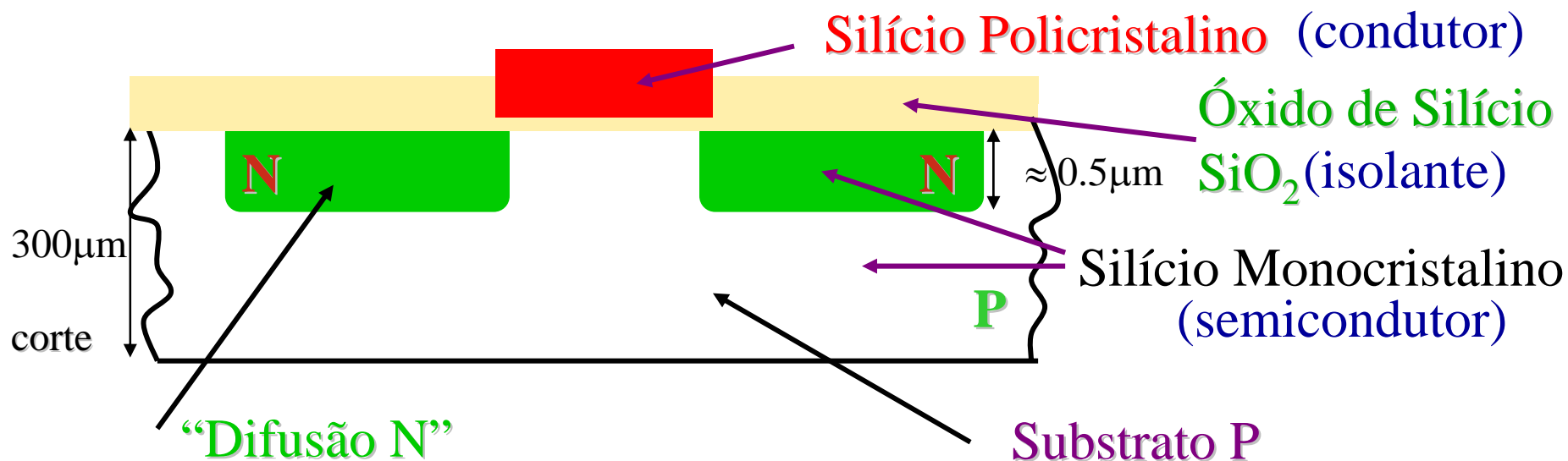
Transistor MOS  
Portas CMOS  
Portas Complexas

# Transistor MOS

## Estruturas MOS



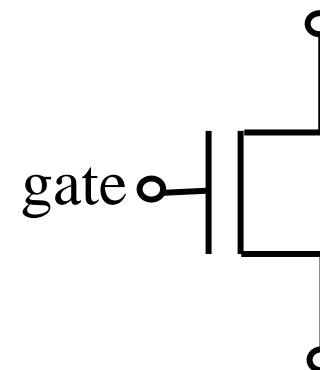
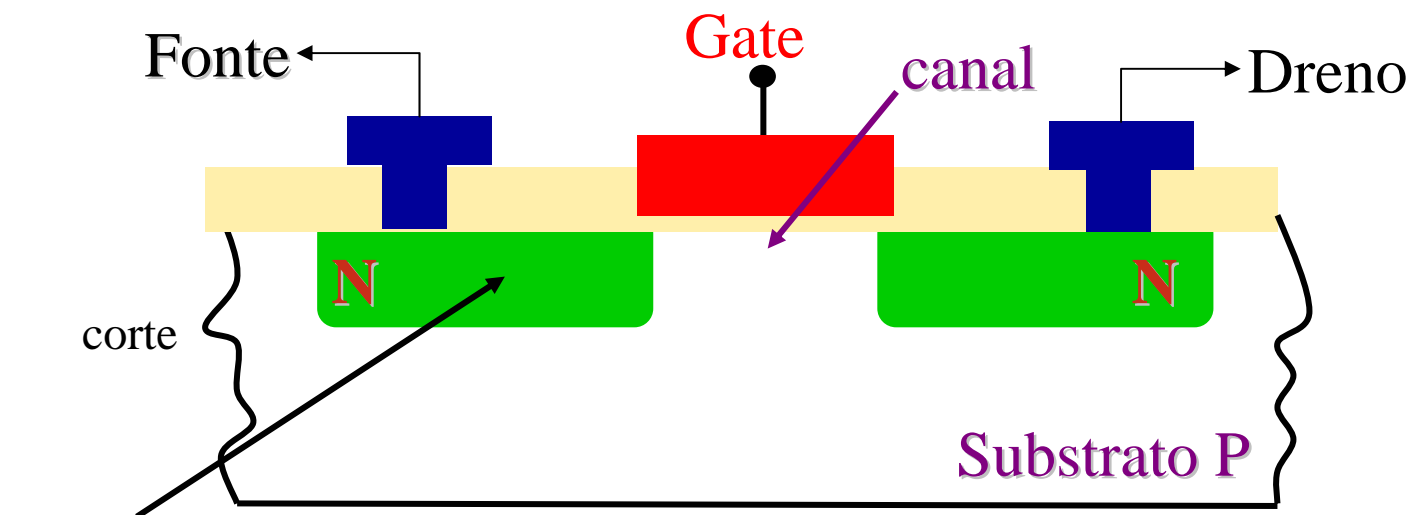
# Transistor MOS



**2 Tipos:**

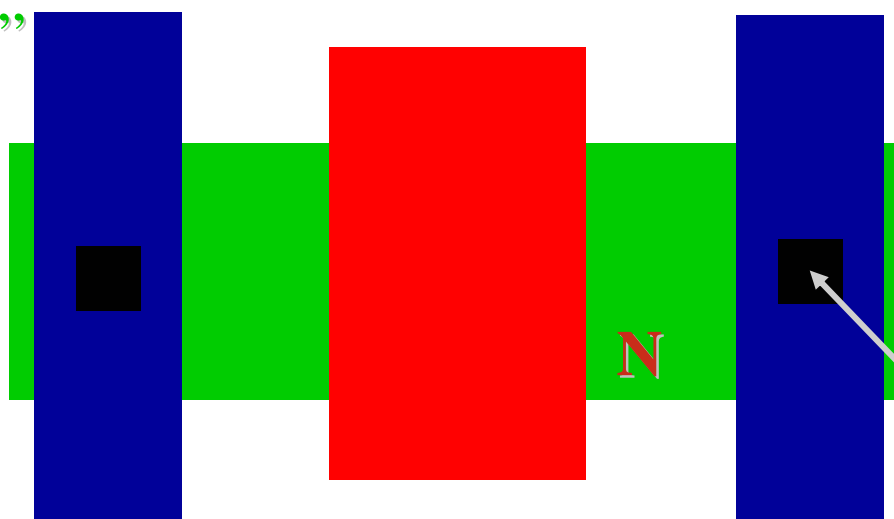
- **PMOS**
- **NMOS**

# Transistor NMOS



“Difusão N”

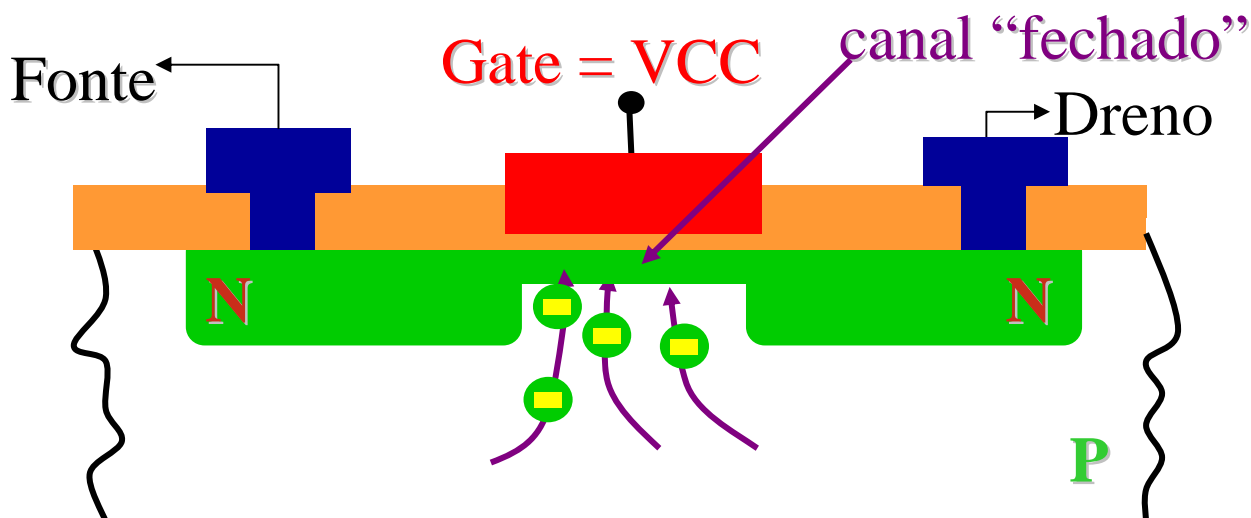
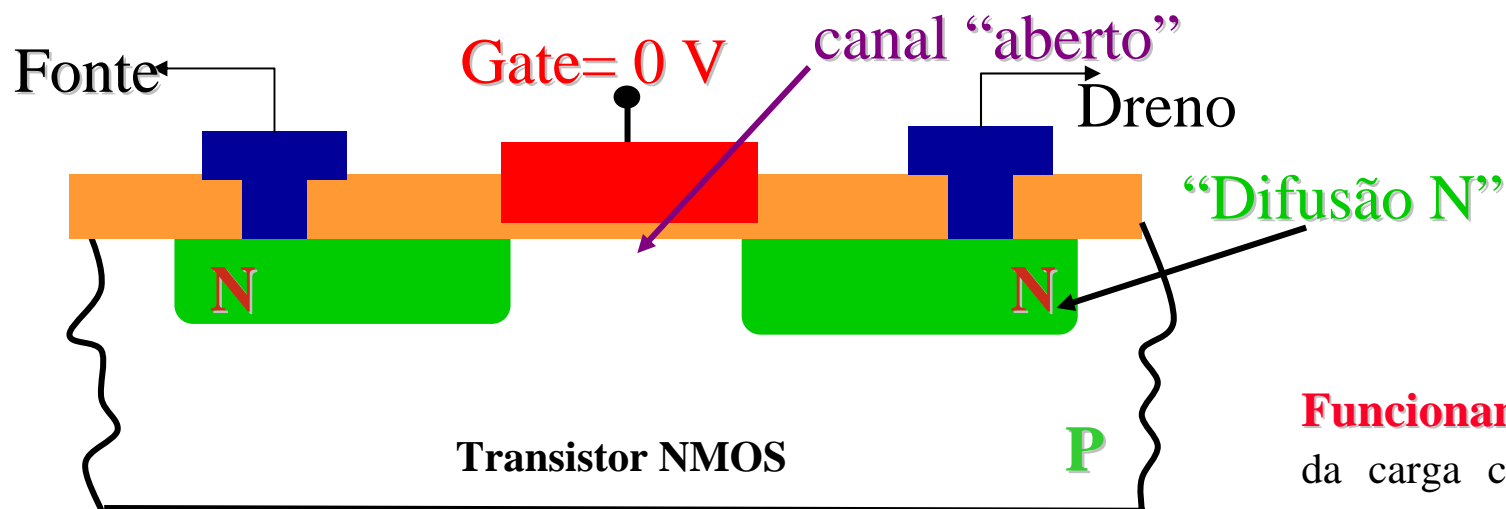
planta baixa



Contato

S - *source*, fonte  
D - *drain*, dreno  
G - *gate*, grade

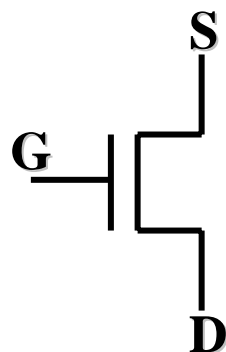
# Transistor NMOS



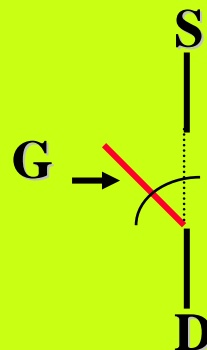
**Funcionamento:** através da carga colocada no gate (G), cargas de sentido oposto são atraídas para a interface com o óxido, formando o canal do transistor. Se estas cargas forem do mesmo tipo que as cargas presentes nas regiões de fonte (S) e dreno (D), haverá passagem de corrente ( $I$ ) entre essas regiões através do canal do transistor.

## Transistor NMOS

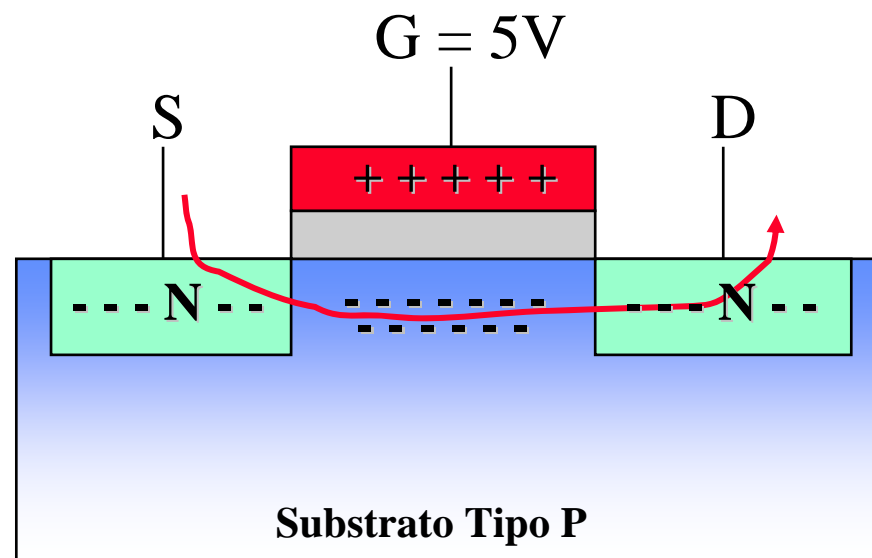
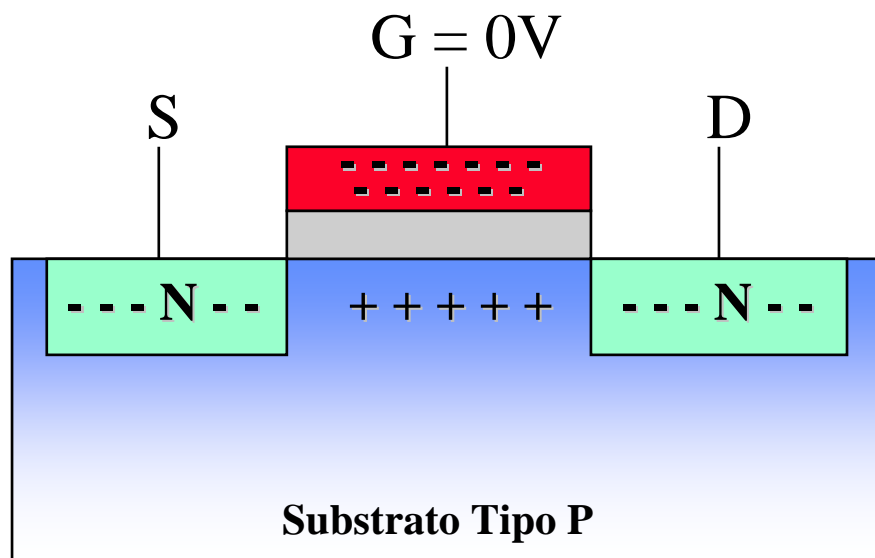
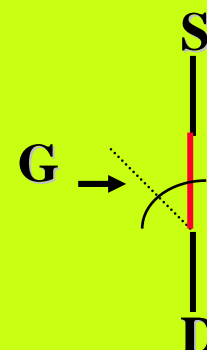
Símbolo:



Se  $G = 0V$  ('0')  
Chave aberta (off)

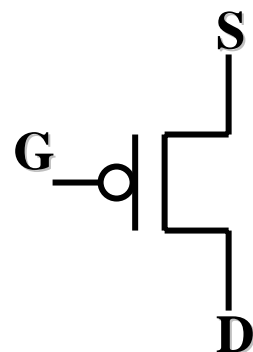


Se  $G = 5V$  ('1')  
Chave fechada (on)

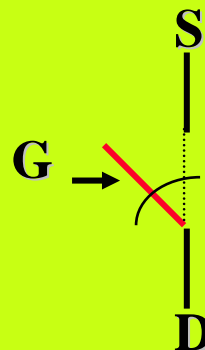


## Transistor PMOS

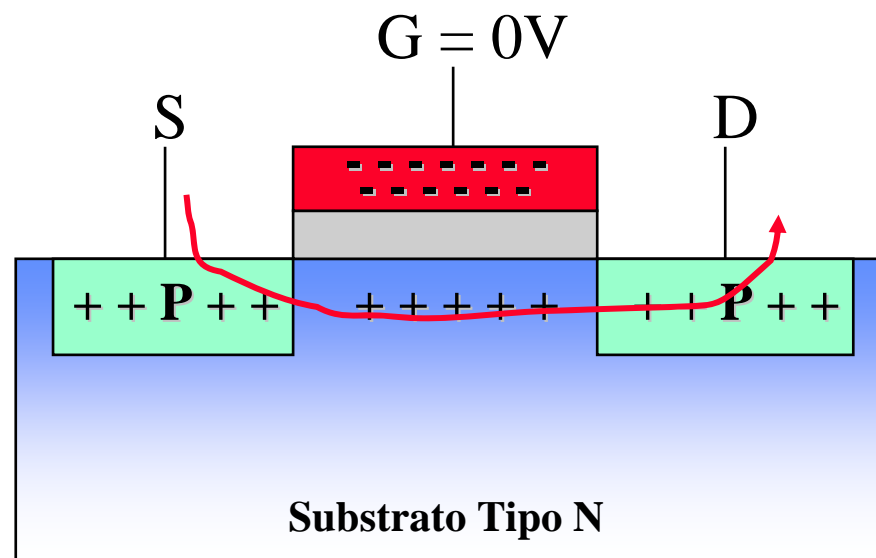
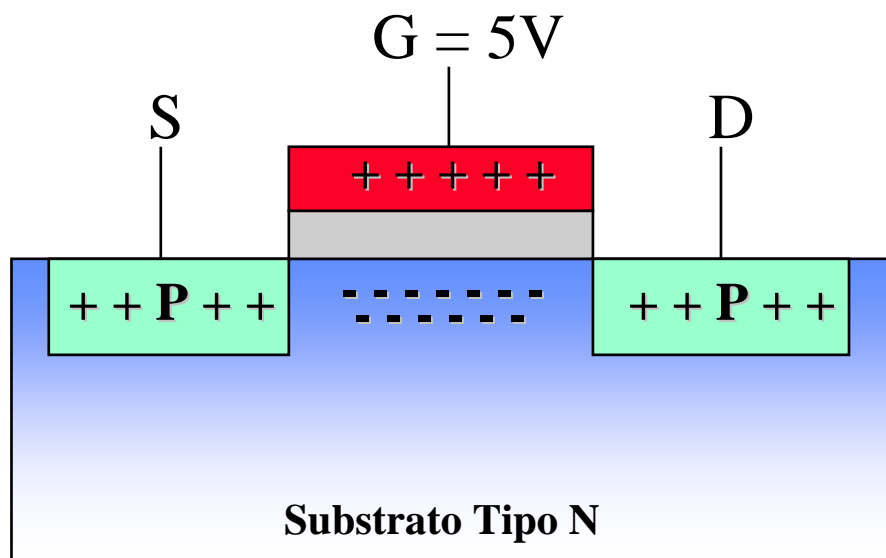
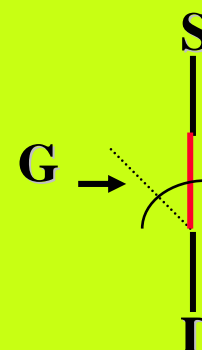
Símbolo:



Se  $G = 5V$  ('1')  
Chave aberta (off)



Se  $G = 0V$  ('0')  
Chave fechada (on)

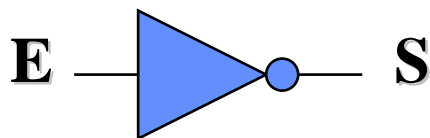


## Portas Lógicas básicas

## Portas XOR/XNOR

**INV**

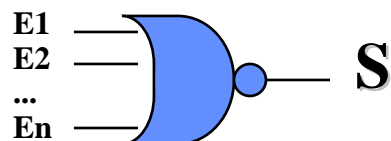
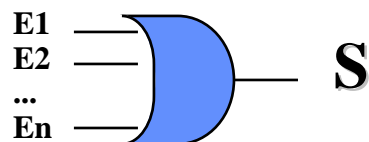
$$E = \bar{S}$$



**OR**

**(NOR)**

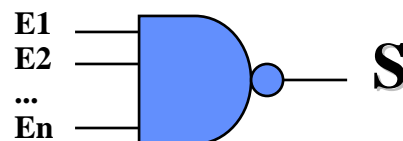
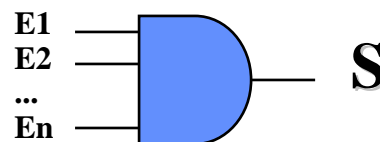
$$S = E1 + E2$$



**AND**

**(NAND)**

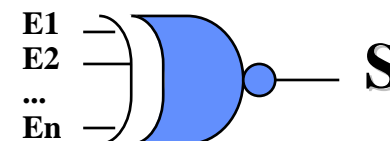
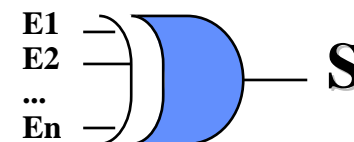
$$S = E1 \bullet E2$$



**XOR**

**(XNOR)**

$$S = E1 \oplus E2$$



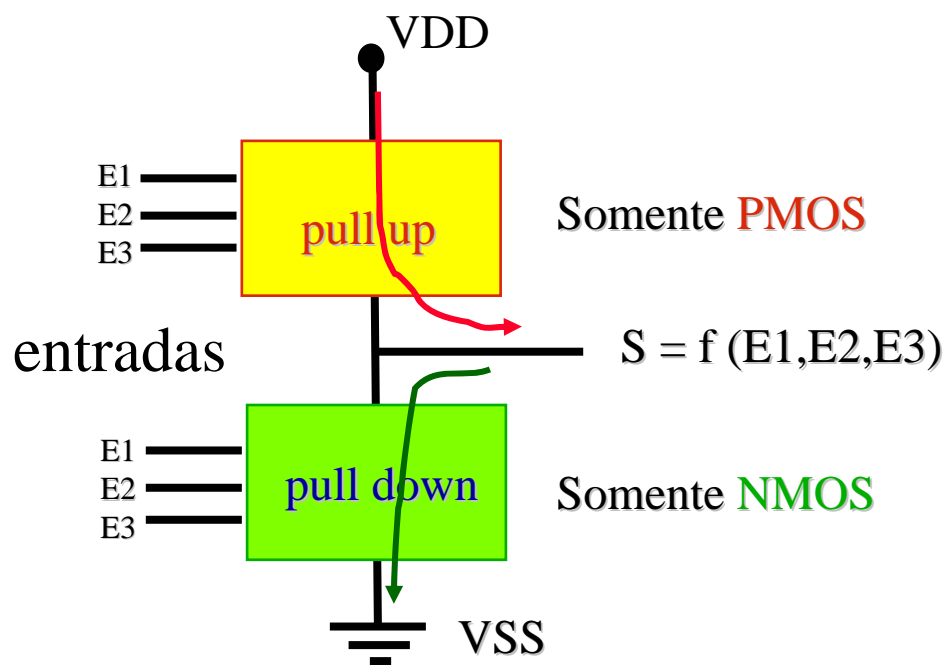
E	INV
0	1
1	0

E1	E2	AND	NAND	OR	NOR	XOR	XNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

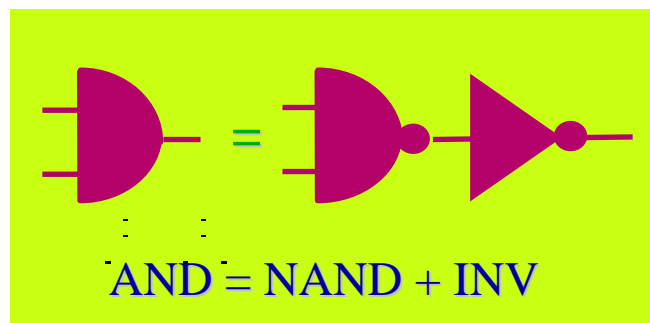


# Portas Lógicas

## Circuitos CMOS Estáticos



De Morgan:  $\overline{A + B} = \overline{A} \cdot \overline{B}$

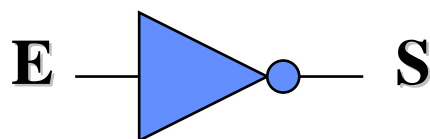


- A lógica PMOS permite conectar o sinal de saída a Vcc (5V), '1' lógico.
- A lógica NMOS permite conectar o sinal de saída a Gnd (0V), '0' lógico.
- Sempre um dos caminhos, para Vcc ou Gnd, estão fechados para a saída, conectando a mesma a 5V ou 0V.

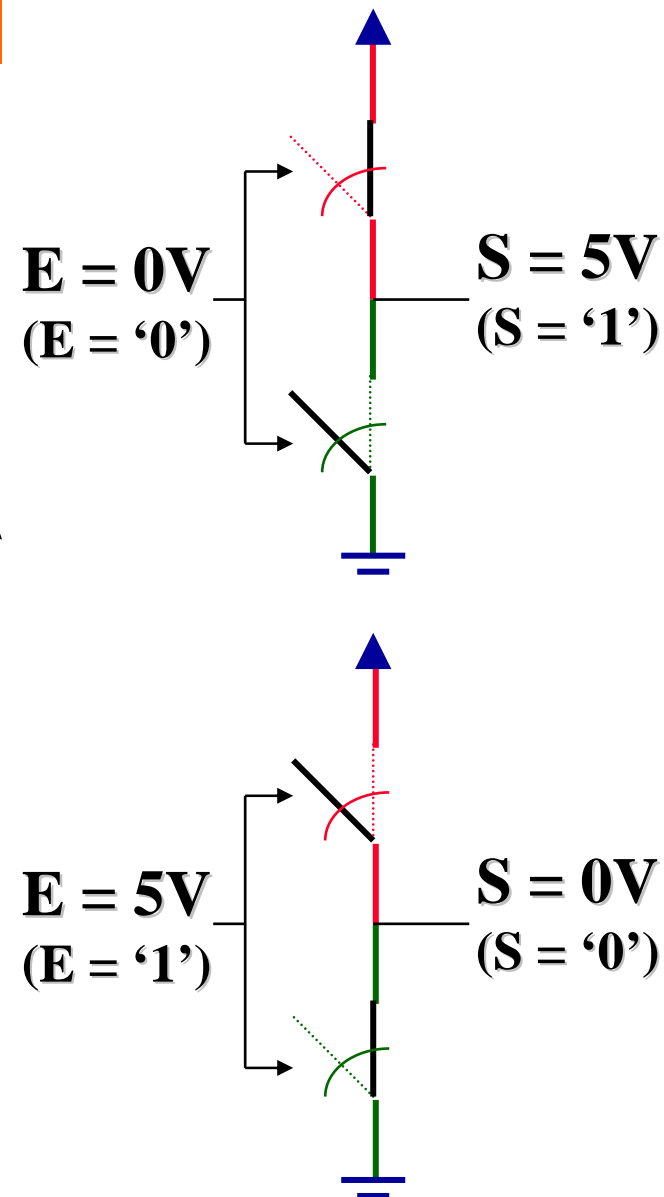
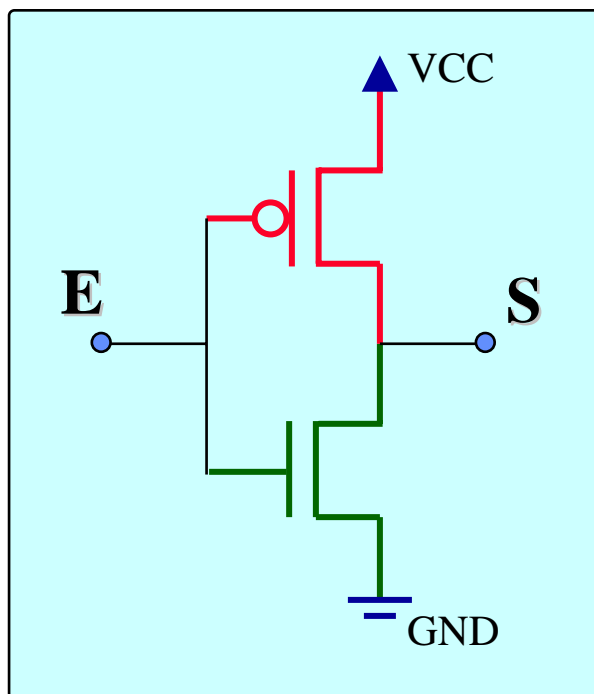
As redes PUP (pull up) e PDN (pull down) são duais nas suas topologias.

# Portas Lógicas

## INVERSOR CMOS



E	S
0	1
1	0



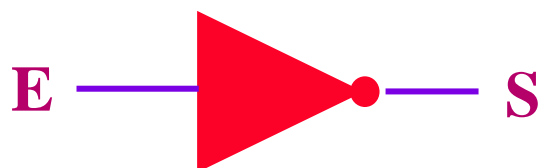
# Portas Lógicas

## INVERSOR CMOS

- Equação:

$$S = \overline{E}$$

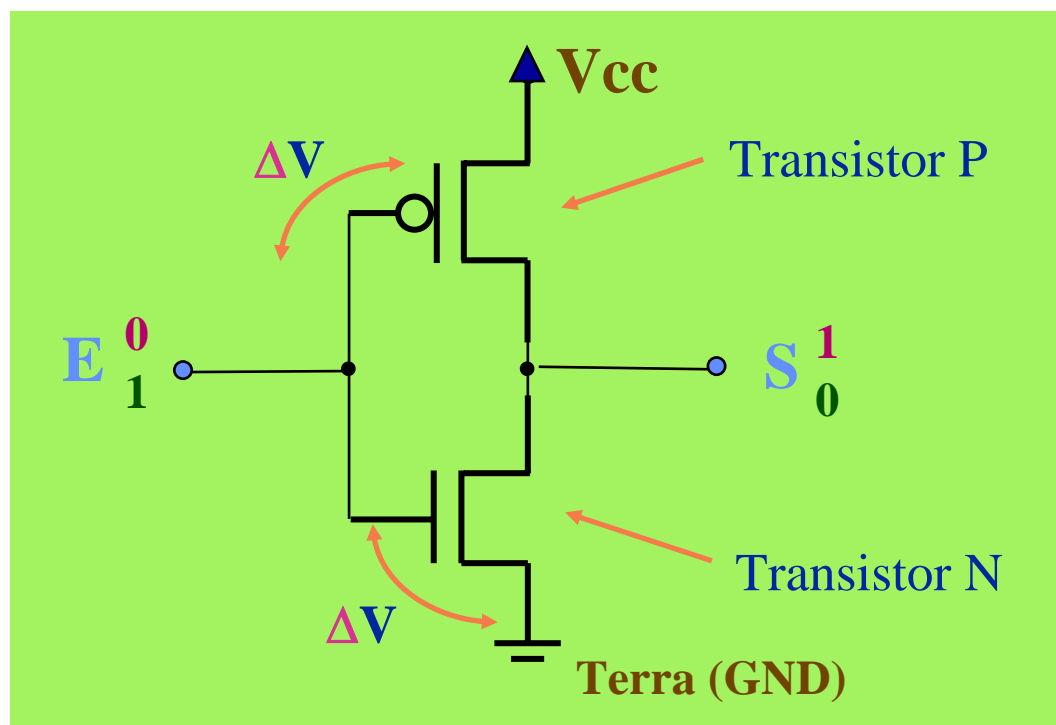
- Esquema Lógico:



- Tabela Verdade:

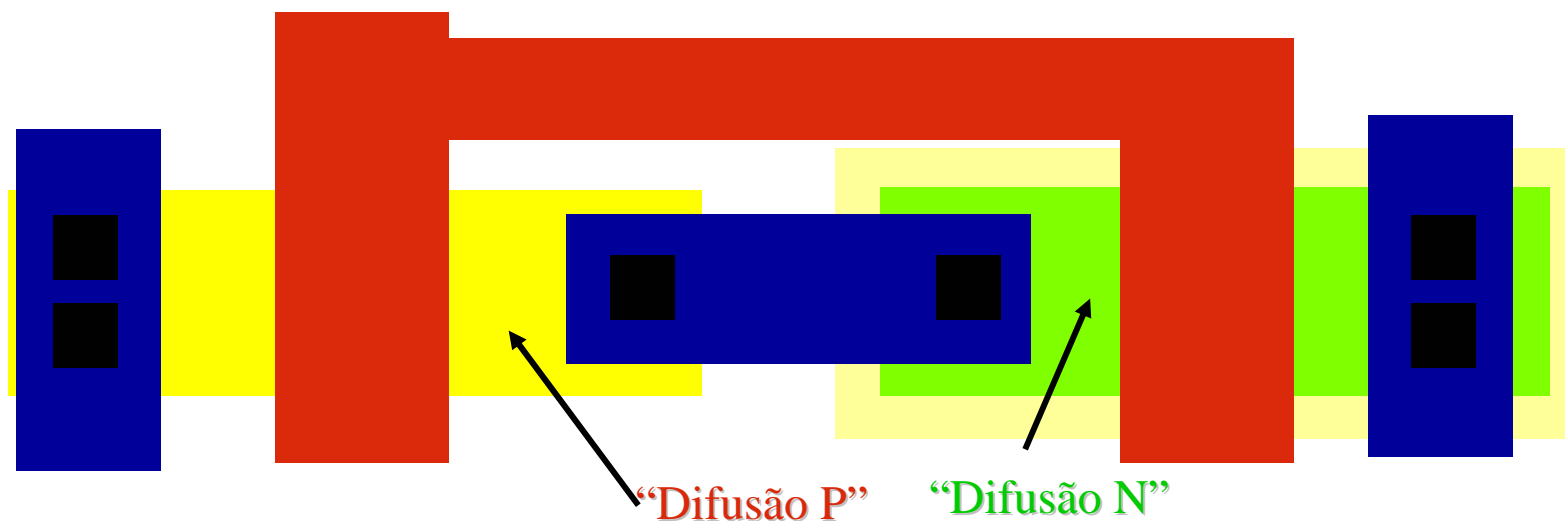
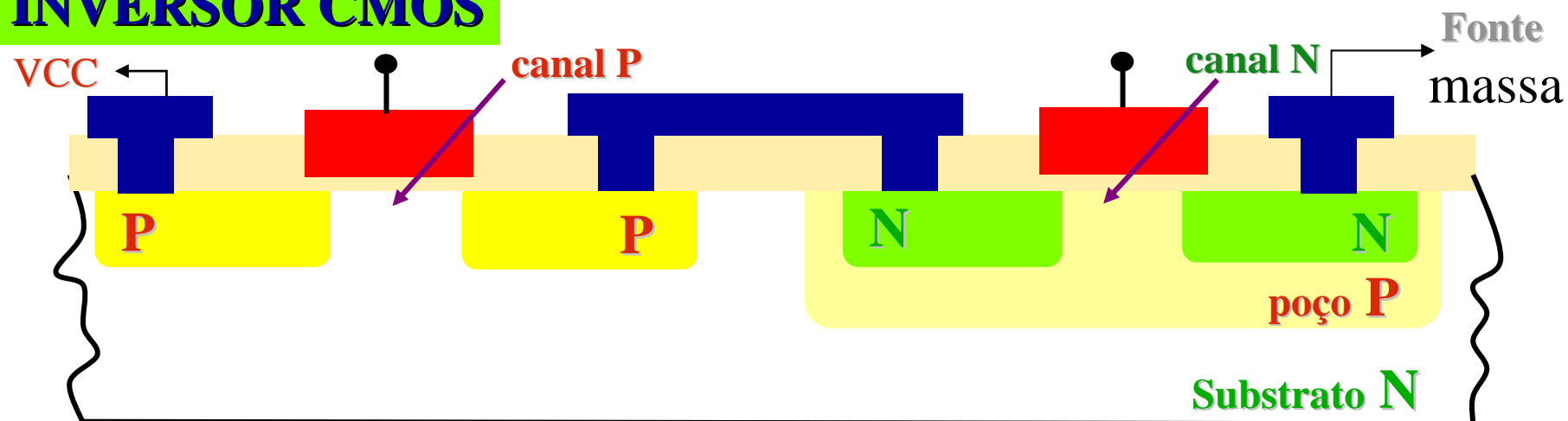
E	S
0	1
1	0

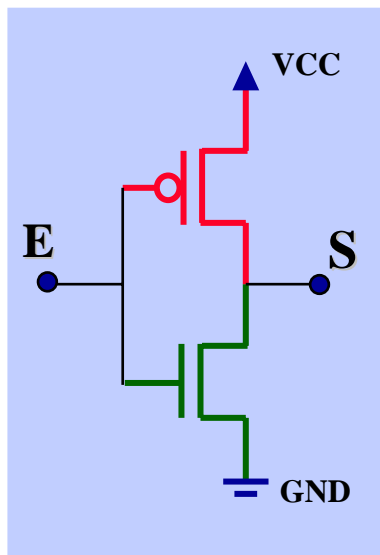
- Esquema Elétrico CMOS



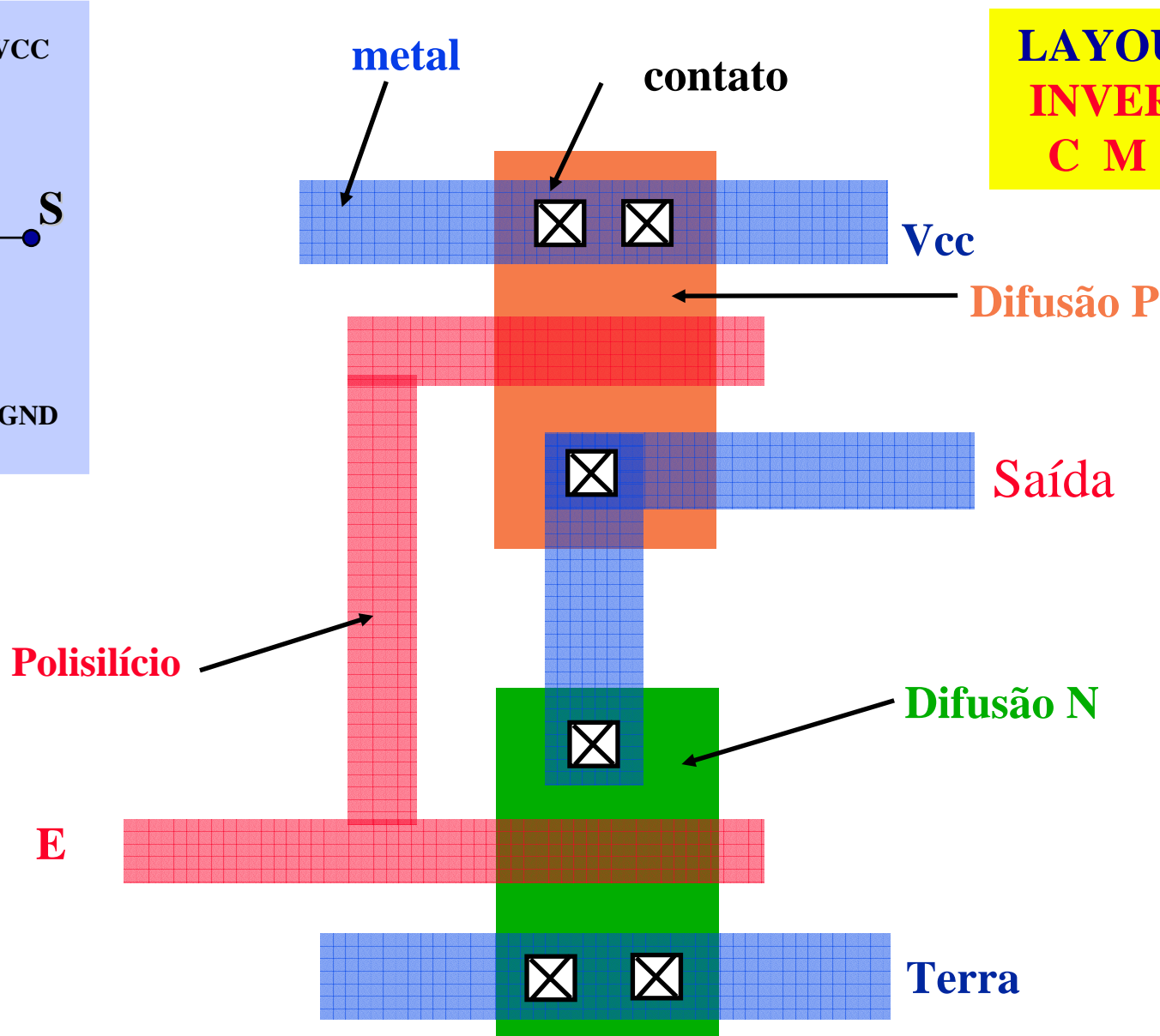
# Portas Lógicas

## INVERSOR CMOS





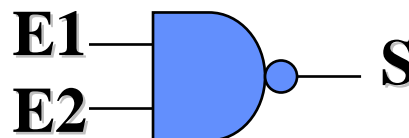
$$S = \overline{E}$$



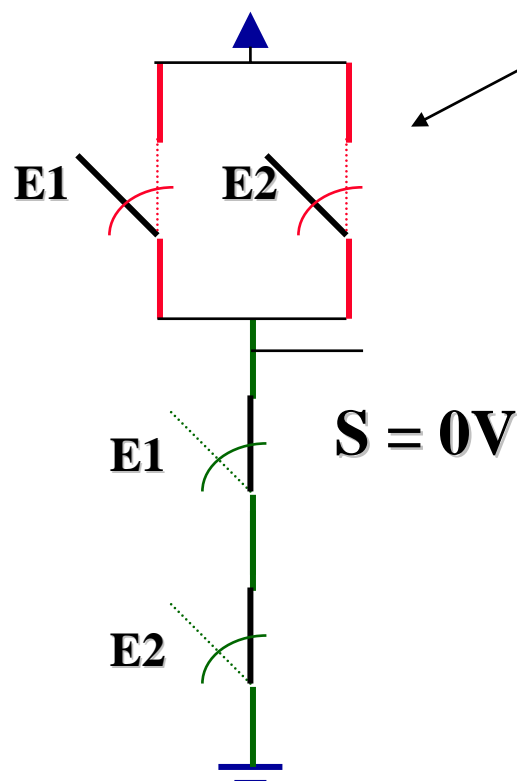
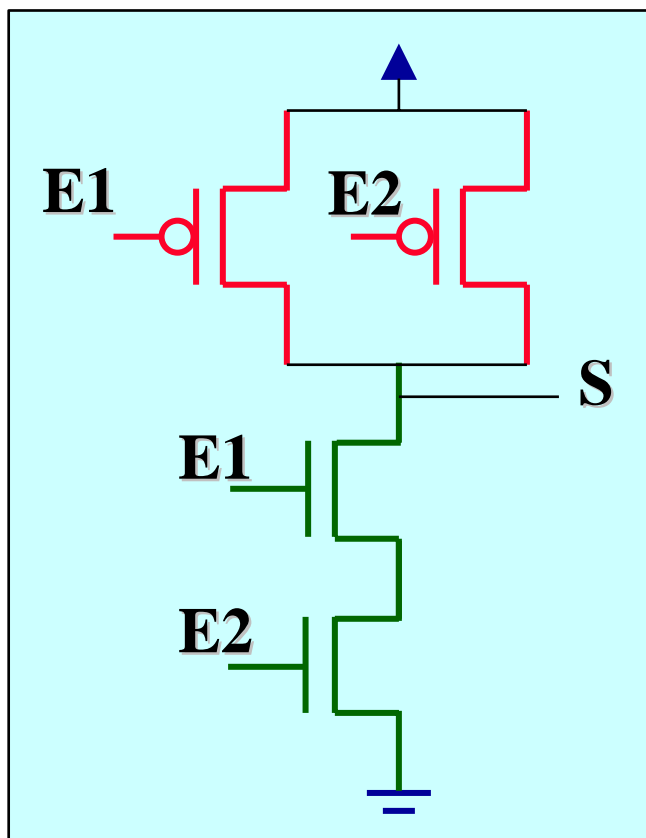
**LAYOUT DO  
INVERSOR  
C M O S**

# Portas Lógicas

## Porta NAND CMOS



E1	E2	S
0	0	1
0	1	1
1	0	1
1	1	0



*Dica:* A SAÍDA É 0 SOMENTE QUANDO TODAS AS ENTRADAS FOREM 1, CASO CONTRÁRIO HAVERÁ 1 NA SAÍDA. CONTRÁRIO DA PORTA 'AND'.

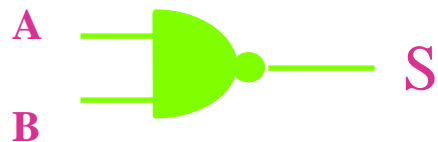
# Portas Lógicas

## Porta NAND CMOS

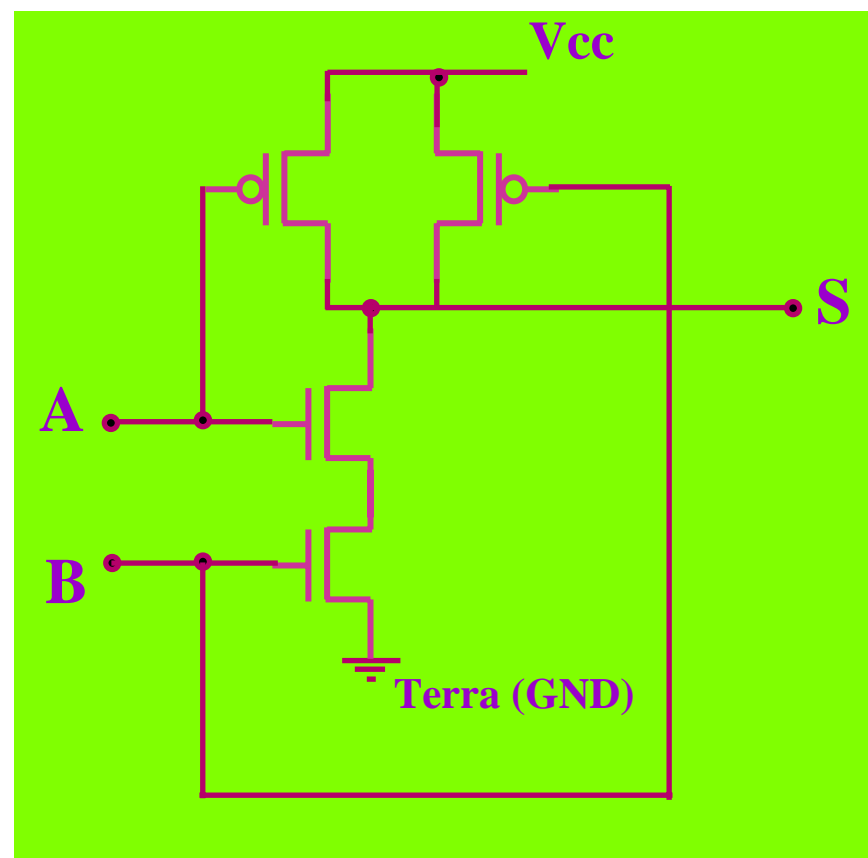
- Equação Lógica:

$$S = \overline{A \cdot B}$$

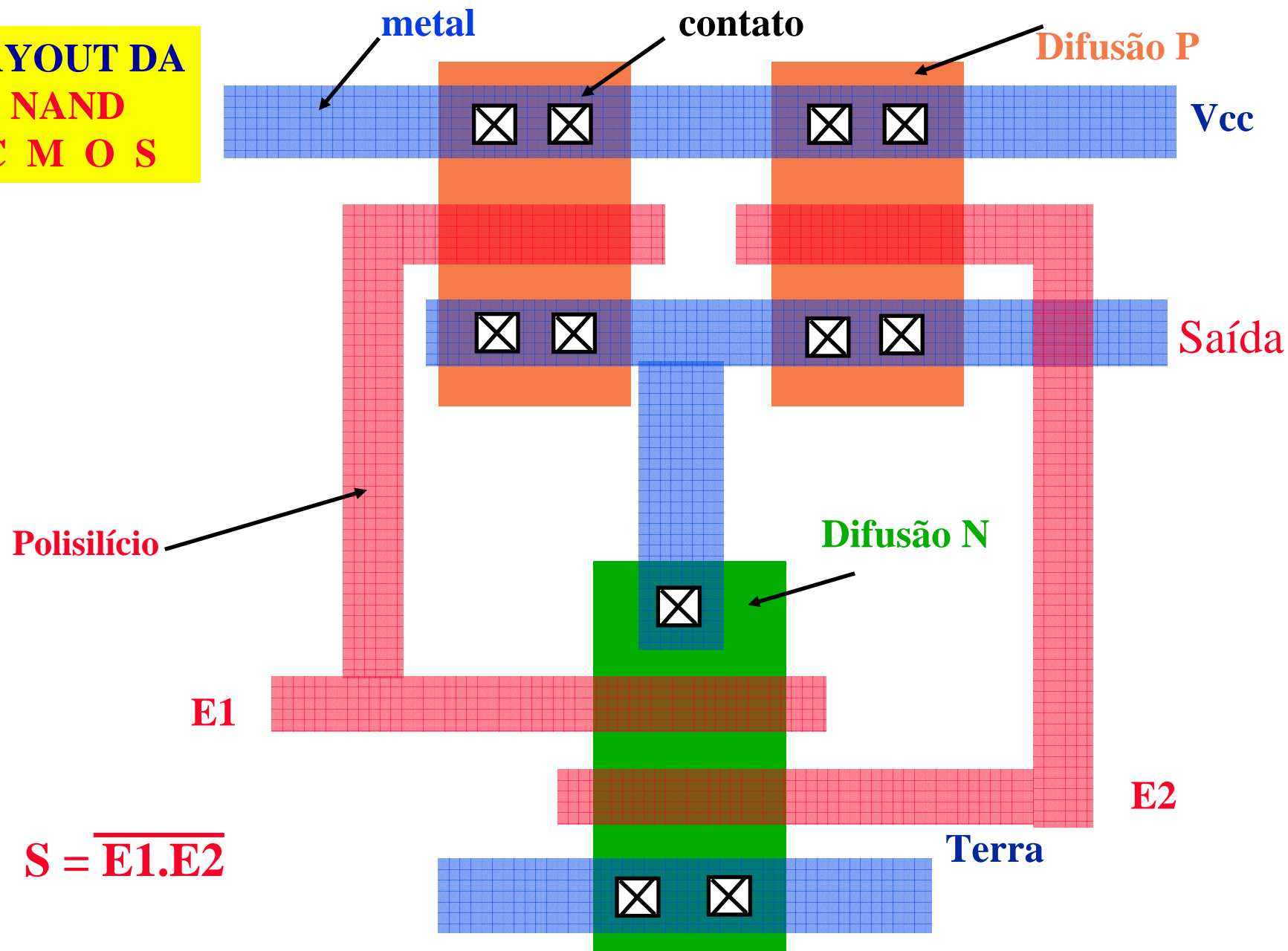
- Esquema Lógico :



- Esquema Elétrico:



## LAYOUT DA NAND CMOS

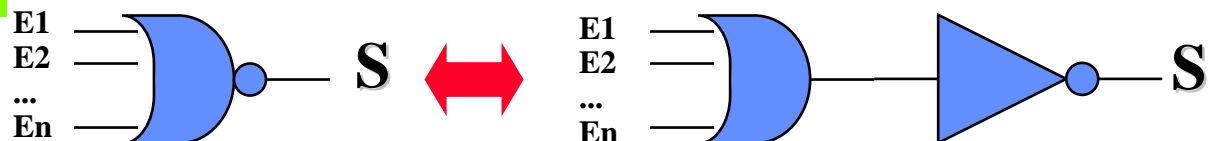




# Portas Lógicas

## Porta NOR CMOS

Símbolo:



Equação Booleana:  $S = \overline{E1 + E2}$   
 $S = \overline{E1 + E2 + \dots + En}$

Tabela Verdade:

E1	E2	S
0	0	1
0	1	0
1	0	0
1	1	0

E1	E2	...	En	S
0	0		0	1
0	1		0	0
1	0		0	0
1	1	...	1	0

*Dica:* A SAÍDA É 1 SOMENTE QUANDO TODAS AS ENTRADAS FOREM 0, CASO CONTRÁRIO HAVERÁ 0 NA SAÍDA. OU SEJA, 1 EM UMA DAS ENTRADAS JÁ GARANTE 0 NA SAÍDA. CONTRÁRIO DA PORTA OR.

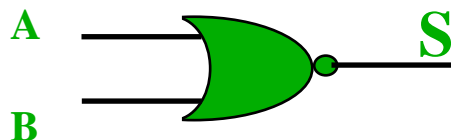
# Portas Lógicas

## Porta NOR CMOS

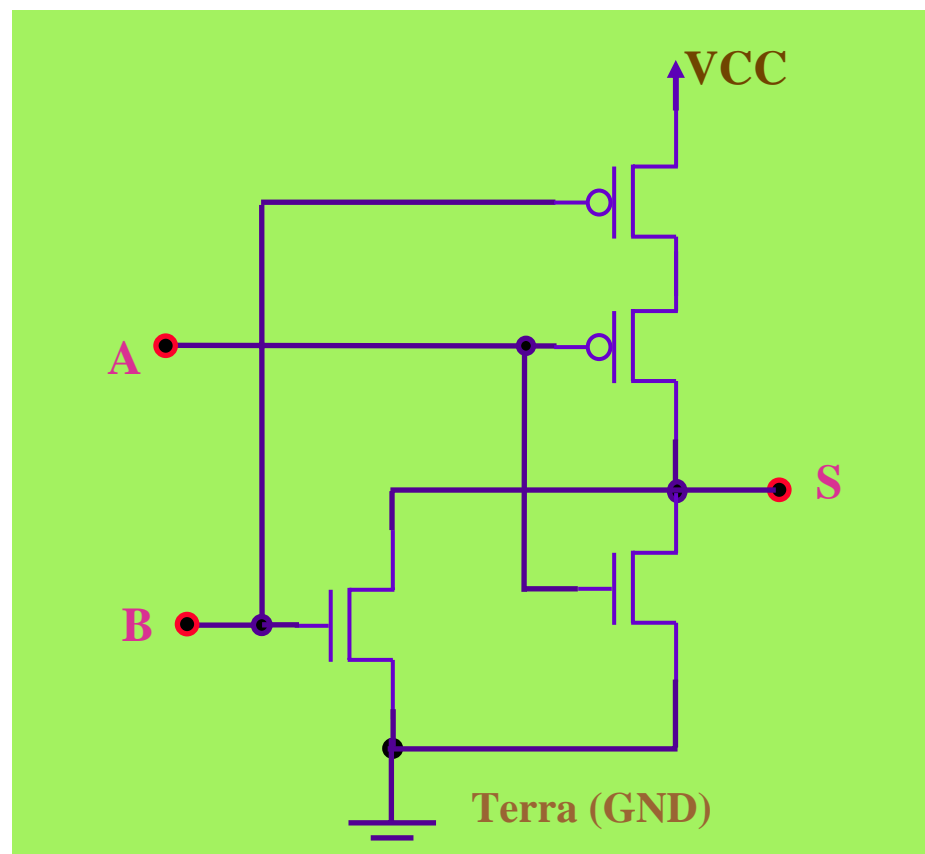
- Equação:

$$S = \overline{A + B}$$

- Esquema Lógico:

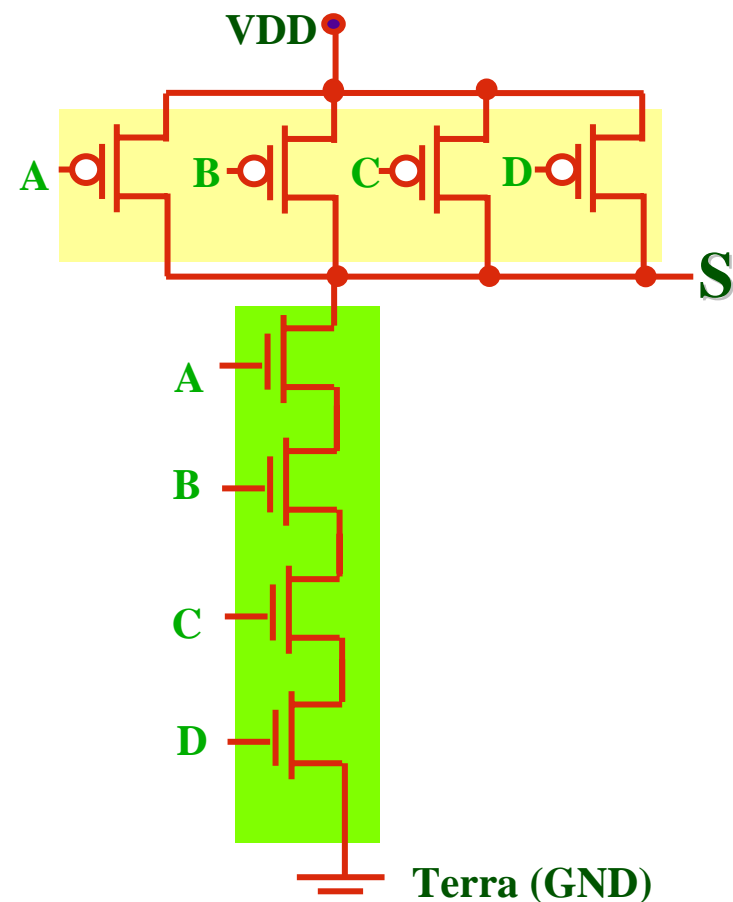
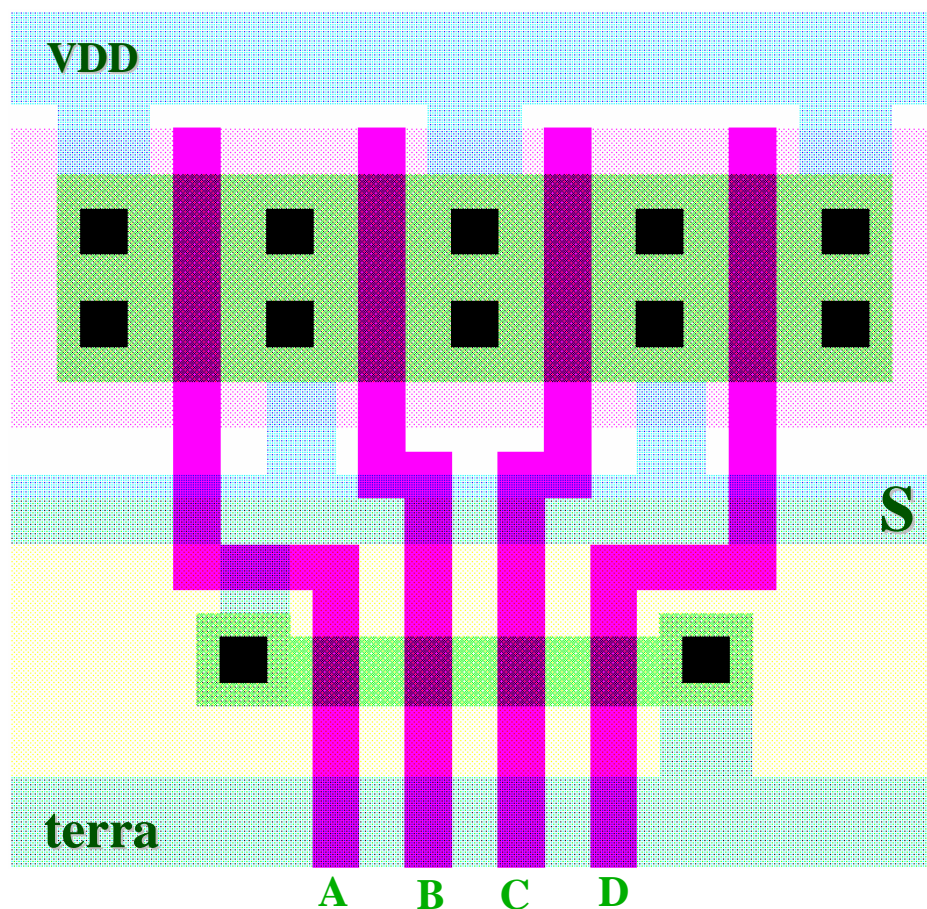
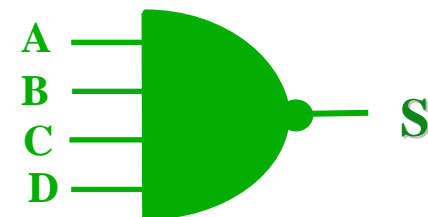


- Esquema Elétrico CMOS

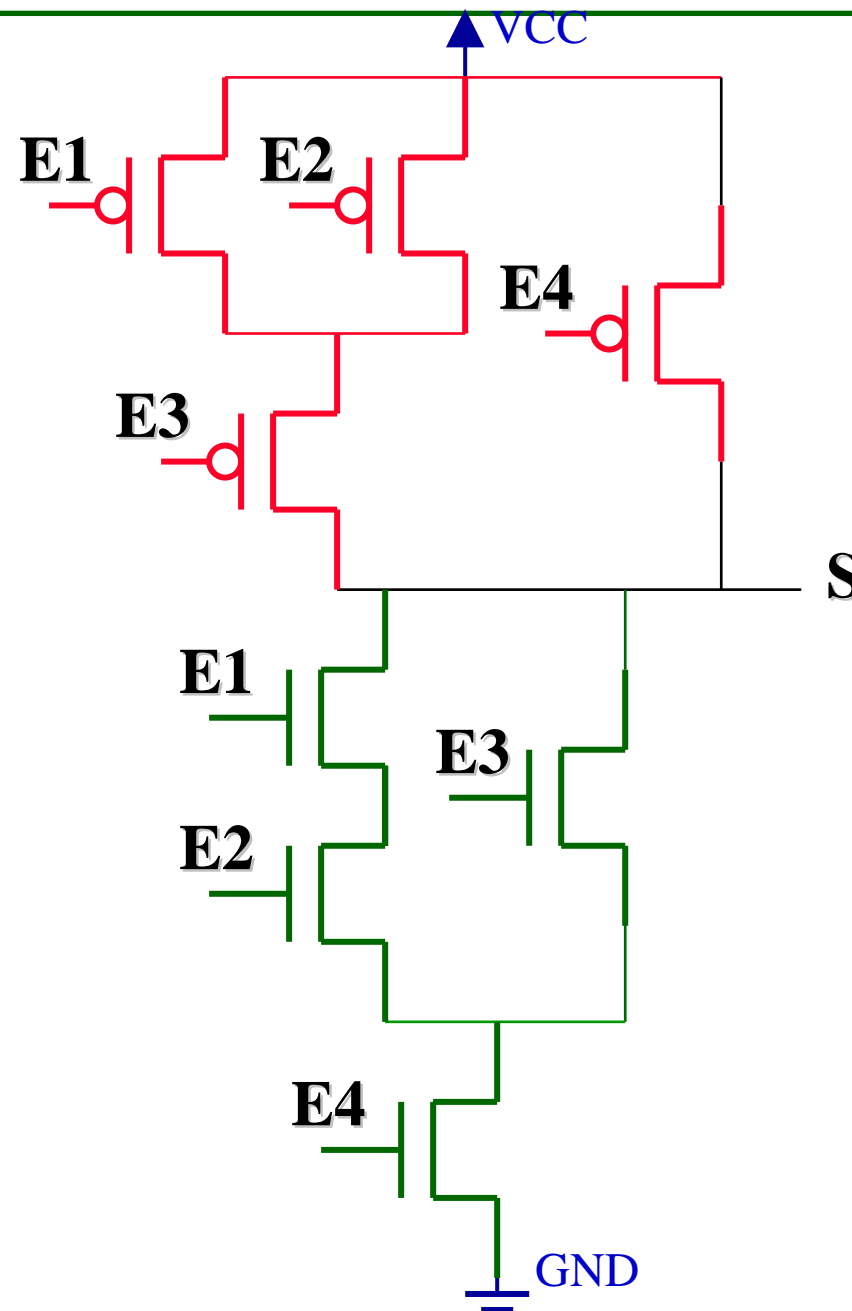
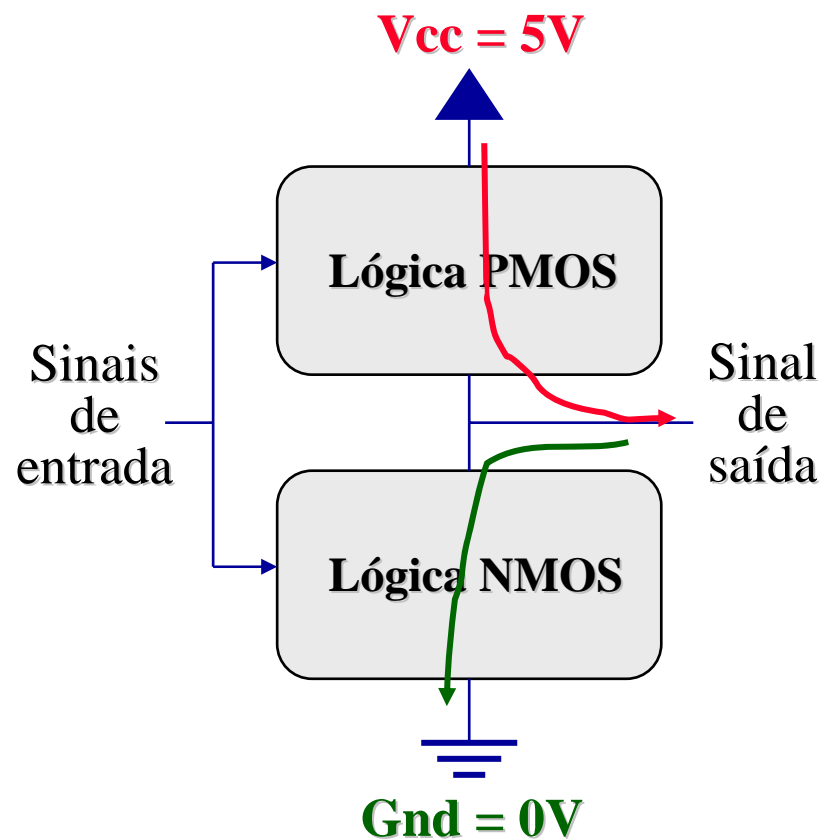


# Portas Lógicas

## Porta NAND CMOS



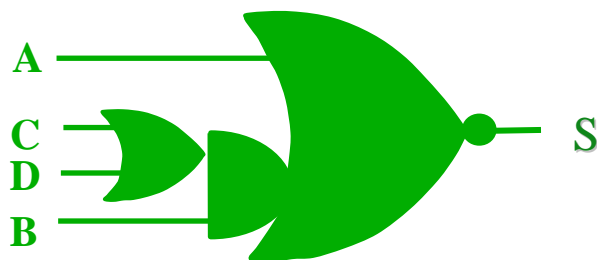
## Portas CMOS Complexas SCCG (Static CMOS Complex Gate)



# Portas Lógicas

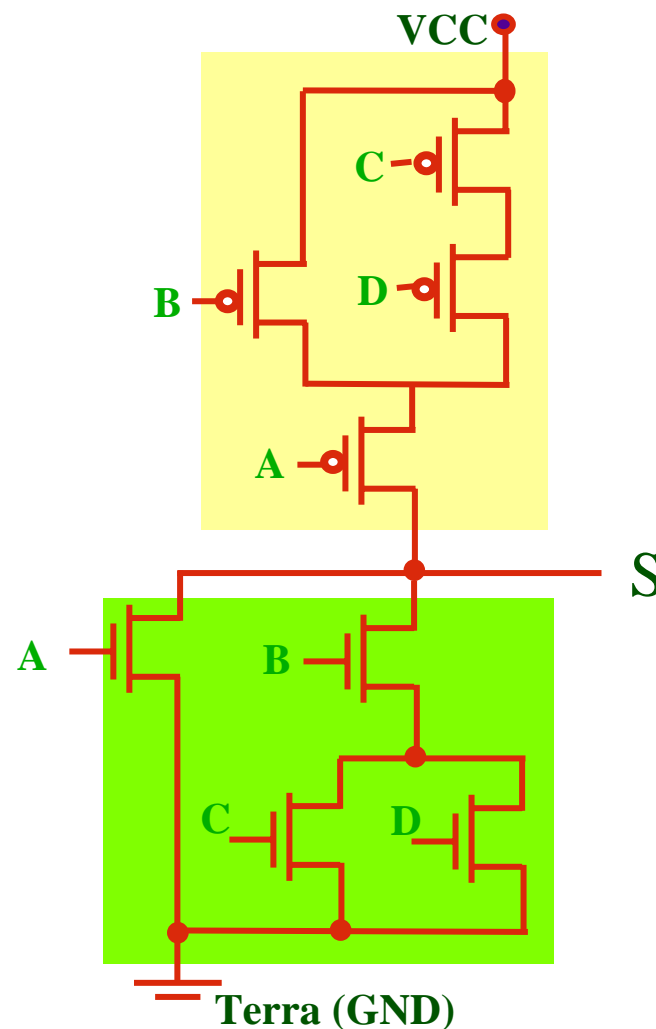
## Portas CMOS Complexas SCCG (Static CMOS Complex Gate)

Exemplo:



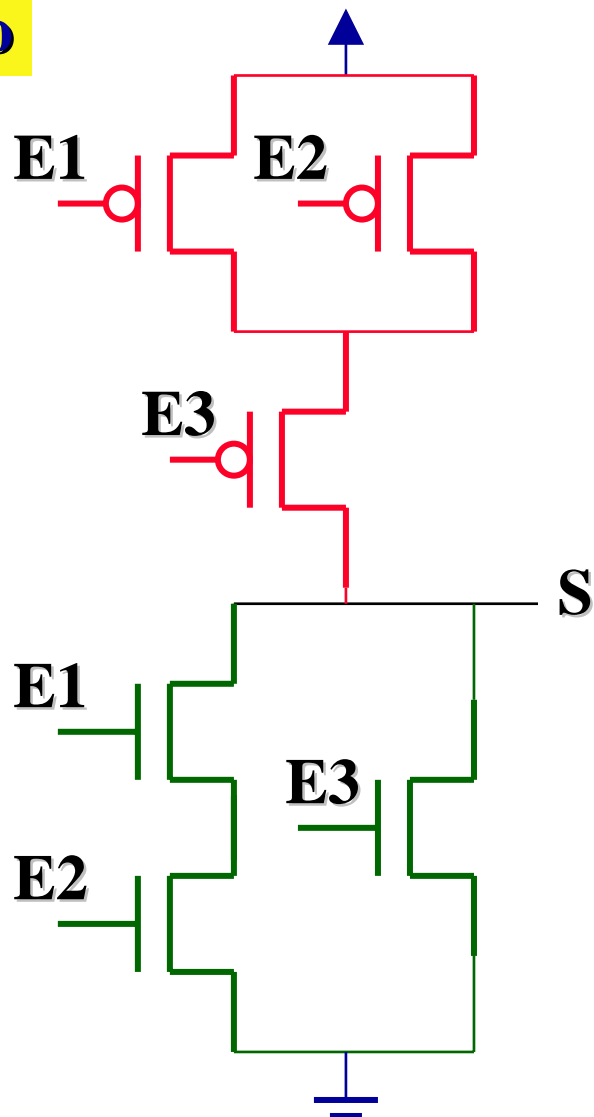
$$S = A + (B \cdot (C + D))$$

O funcionamento complementar das redes (P e N) é definido pela topologia dual das redes de “pull up” e de “pull down”.

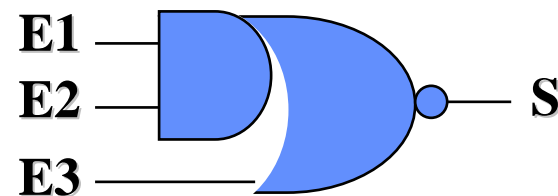


# Portas Lógicas

## Exercício



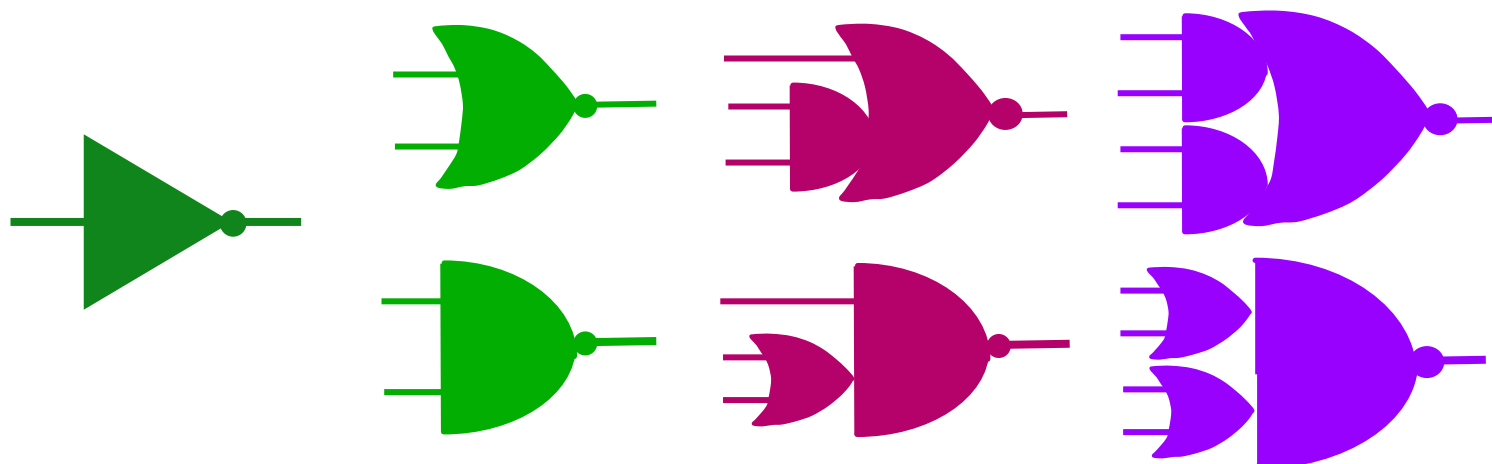
E1	E2	E3	S
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



# Portas Lógicas

## Portas CMOS Complexas

**SCCG** (Static CMOS Complex Gate)



Exemplo: Funções com até 2 transistores em série