INF01 118

Técnicas Digitais para Computação

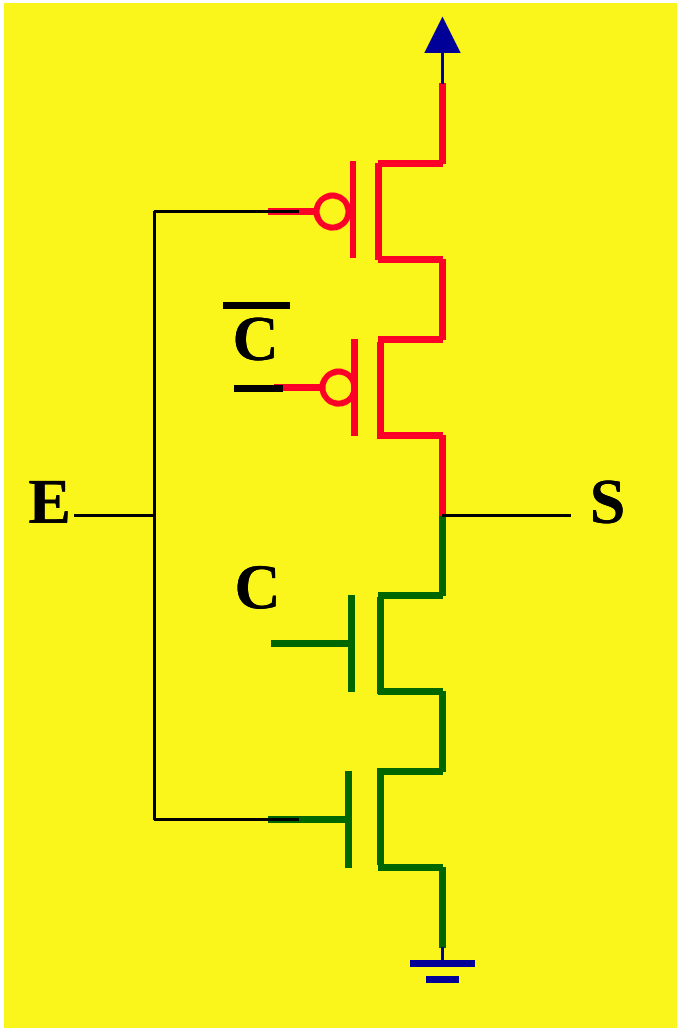
Alta Impedância
Parasitas RC em Portas CMOS
Célula RAM

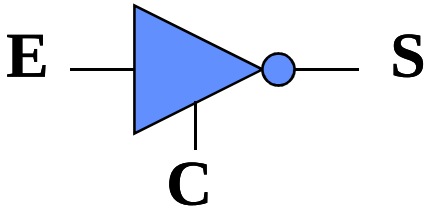
UFRGS

Aula 6

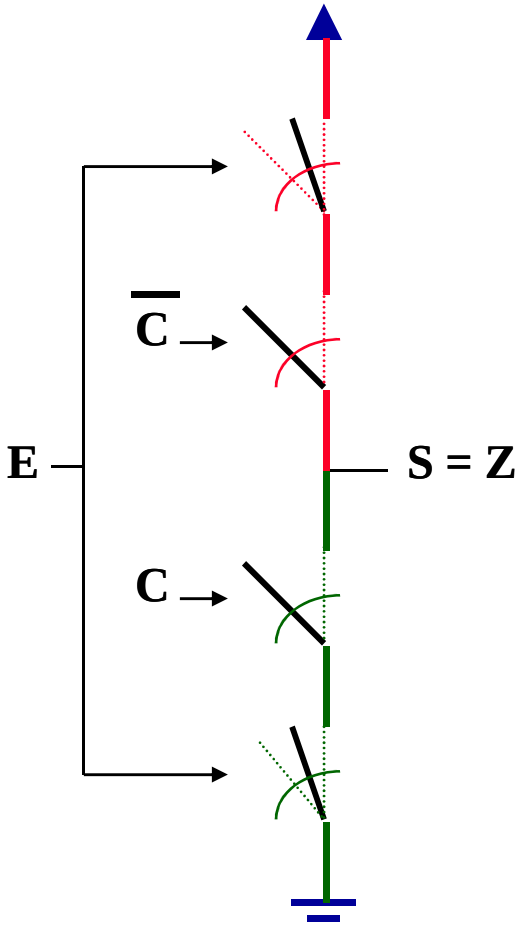
Alta Impedância (Z)

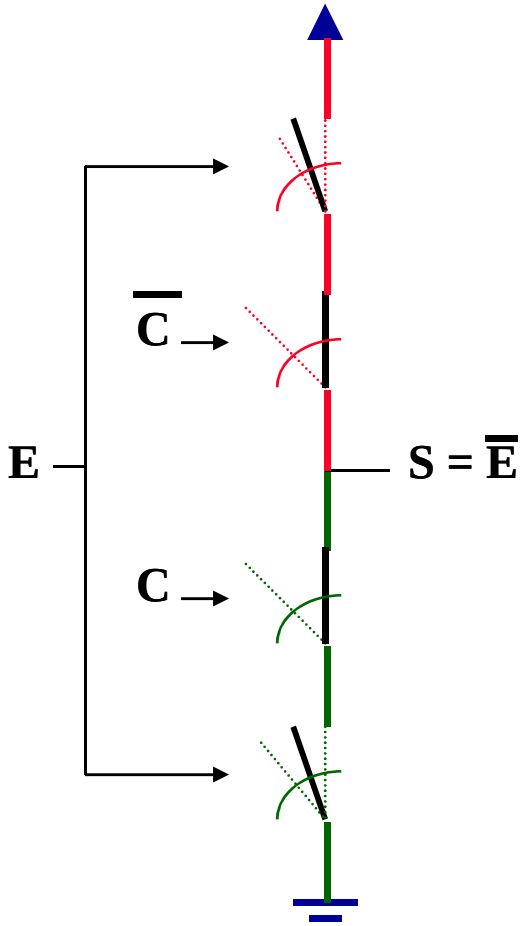
Inversor Tri-State (INVTR)



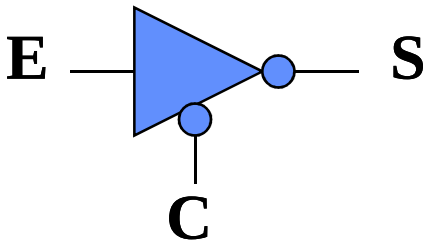


E	C	$\overline{C}$	S
0	0	1	Z
1	0	1	Z
0	1	0	1
1	1	0	0





Outra opção... (*controle negado*)

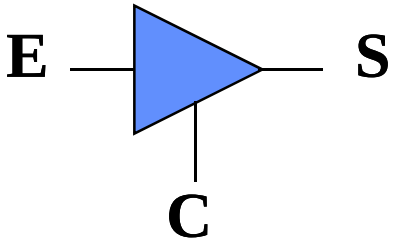


E	C	S
0	0	1
1	0	0
0	1	Z
1	1	Z

OU

C	S
0	$\overline{E}$
1	Z

Buffer Tri-State (BUFTR)

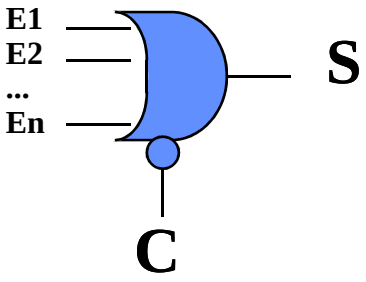


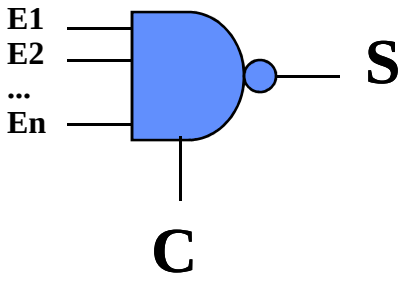
E	C	S
0	0	0
1	0	1
0	1	Z
1	1	Z

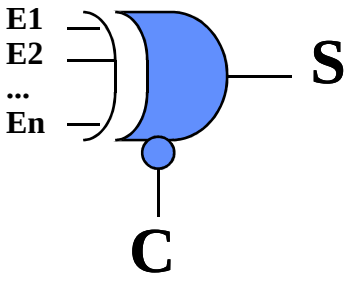
OU

C	S
0	Z
1	E

*** PODE-SE PENSAR EM QUALQUER PORTA LÓGICA COM SAÍDA TRI-STATE OU ALTA-IMPEDÂNCIA (Z) !!!**

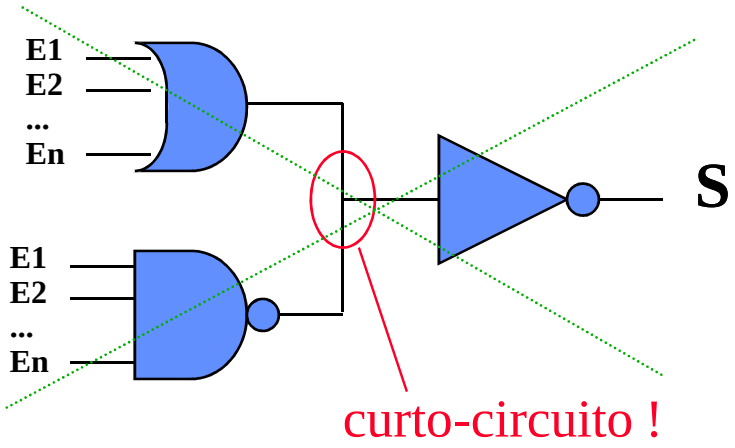




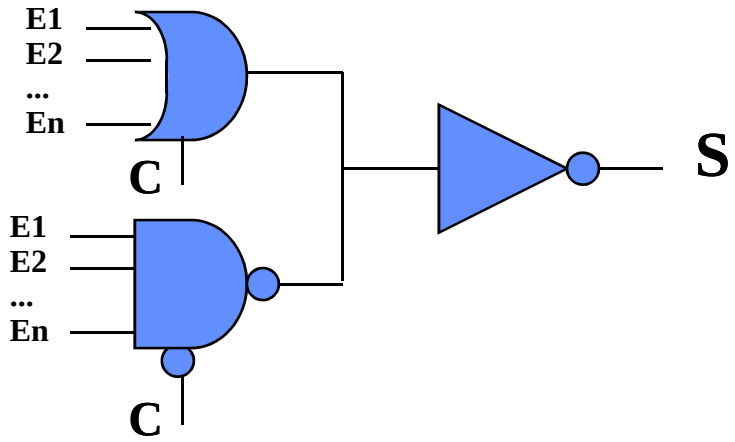


Uso de Porta Tri-State ...

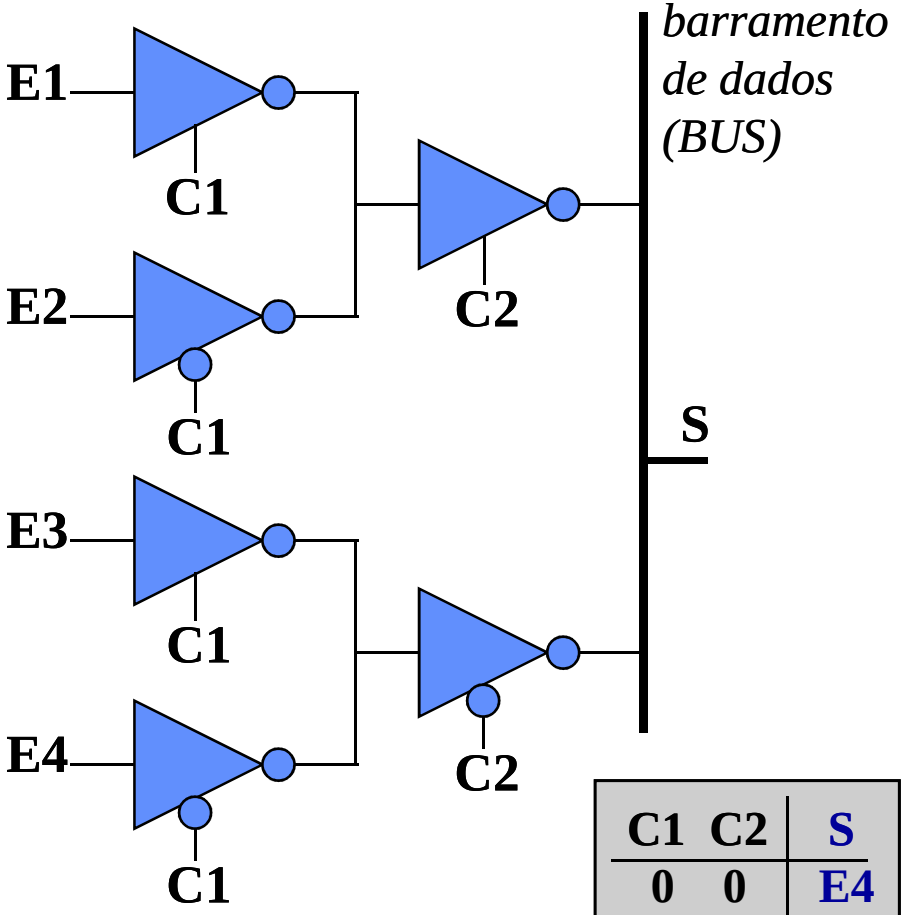
* NÃO É PERMITIDO EM CMOS :



* CORRETO :



* BARRAMENTO DE SINAIS :

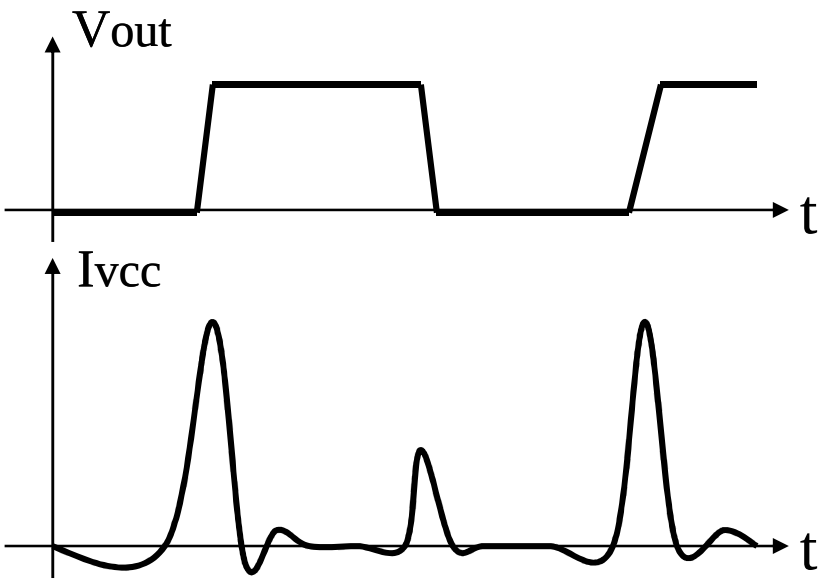


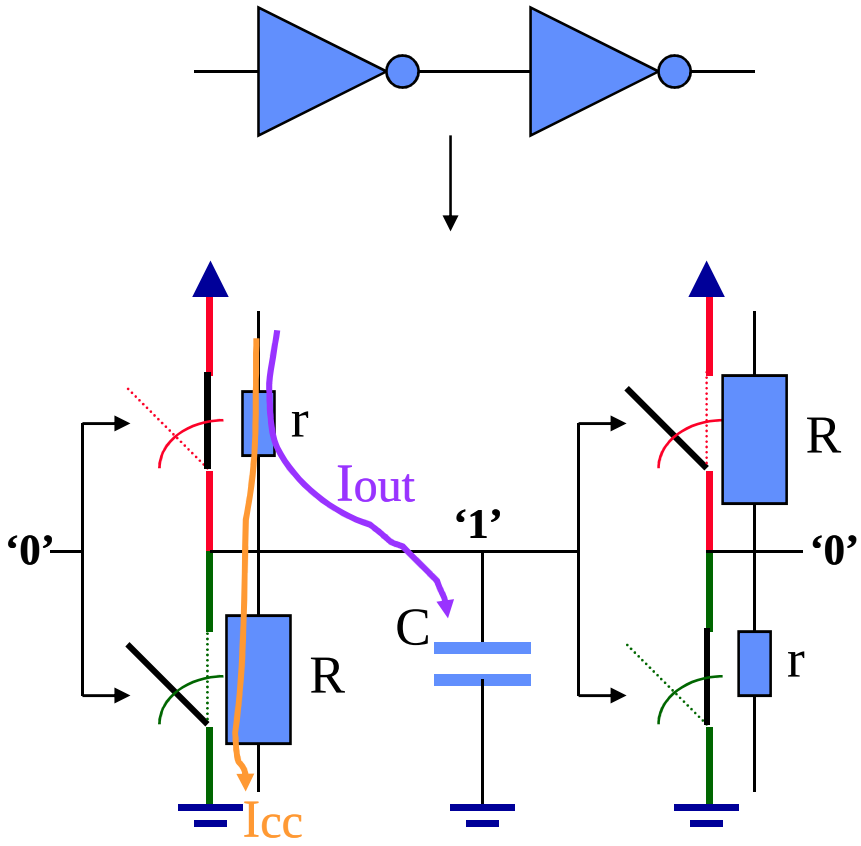
C1	C2	S
0	0	E4
1	0	E3
0	1	E2
1	1	E1

Consumo (Dissipação de Potência)

- Corrente de Carga: Iout
- Corrente de Curto-Circuito: Icc

- consumo estático ≈ 0
- consumo dinâmico (transição) = Iout + Icc
- consumo total = estático + dinâmico



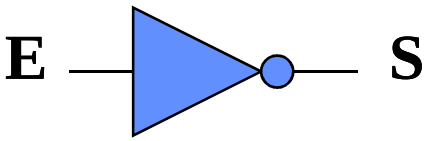


* A variação de W e L afeta o tempo de transição dos sinais e o consumo da porta lógica.

Portas Lógicas (revisão ...)

INV

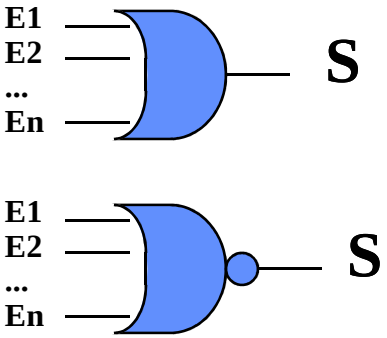
$E = \overline{S}$



E	INV
0	1
1	0

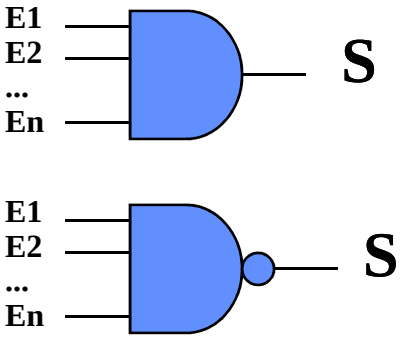
OR (NOR)

$S = E1 + E2$



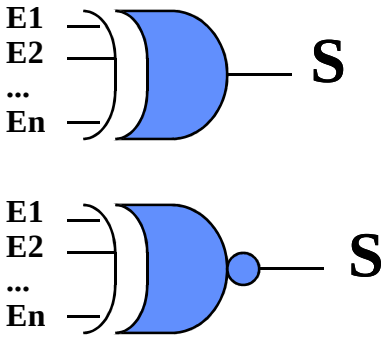
AND (NAND)

$S = E1 \bullet E2$



XOR (XNOR)

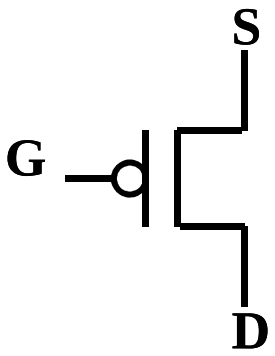
$S = E1 \oplus E2$



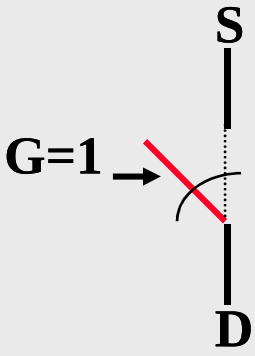
E1	E2	AND	NAND	OR	NOR	XOR	XNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

Transistores PMOS e NMOS (revisão ...)

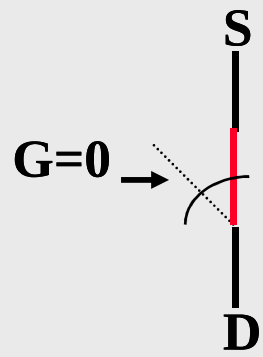
PMOS:



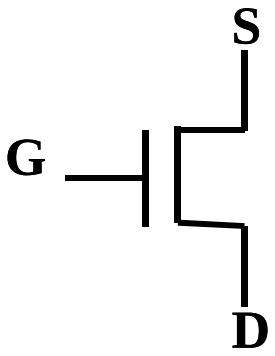
Se **G = 5V (‘1’)**
Chave aberta (off)



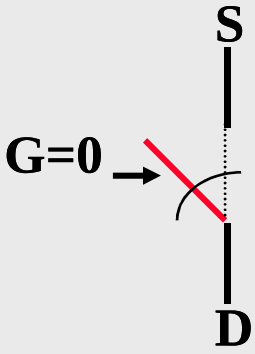
Se **G = 0V (‘0’)**
Chave fechada (on)



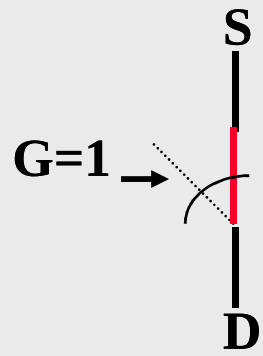
NMOS:



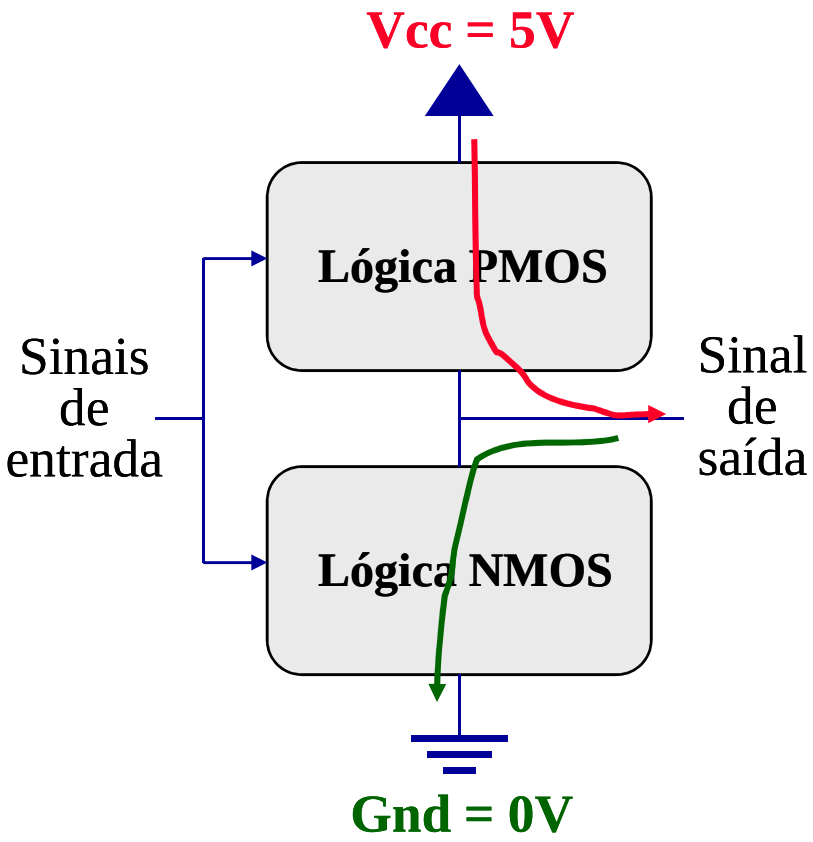
Se **G = 0V (‘0’)**
Chave aberta (off)

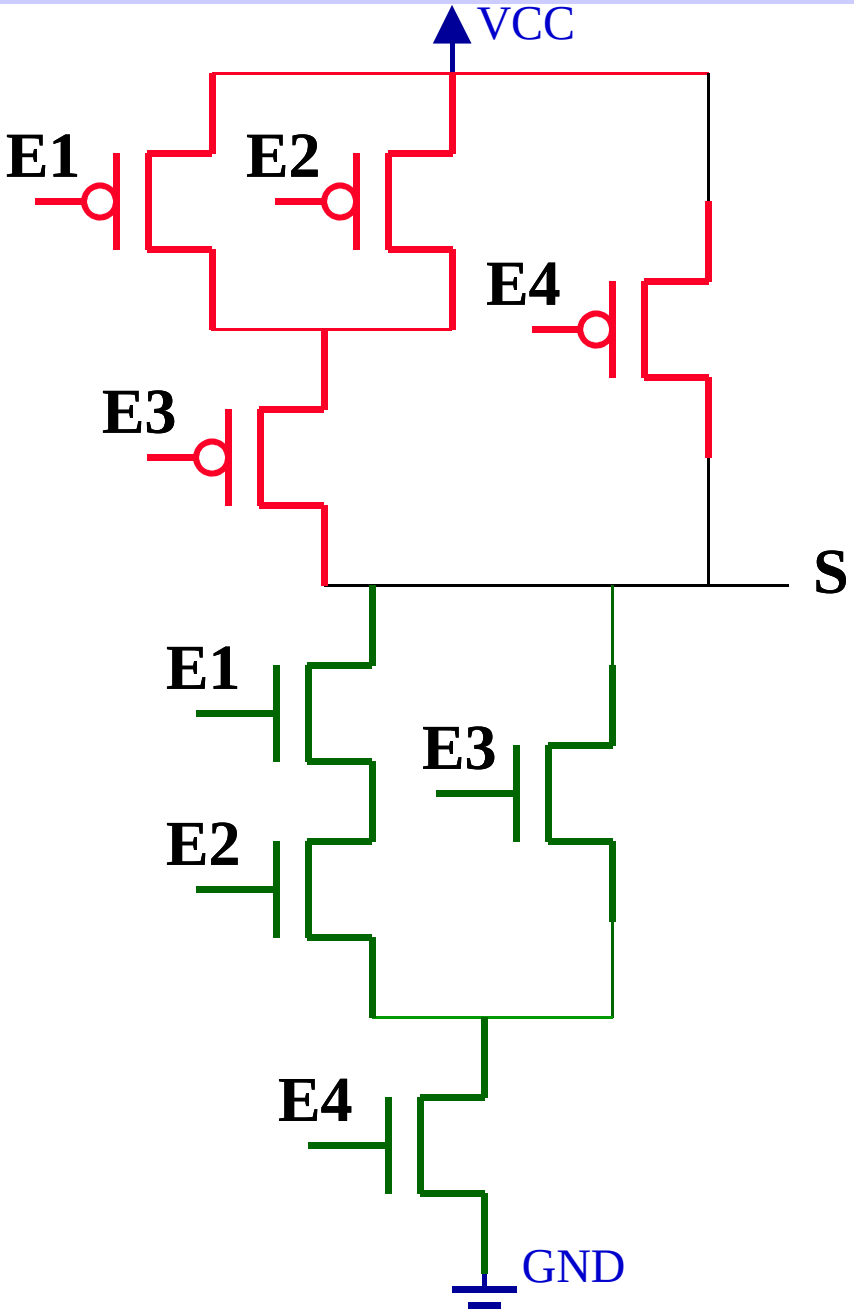


Se **G = 5V (‘1’)**
Chave fechada (on)



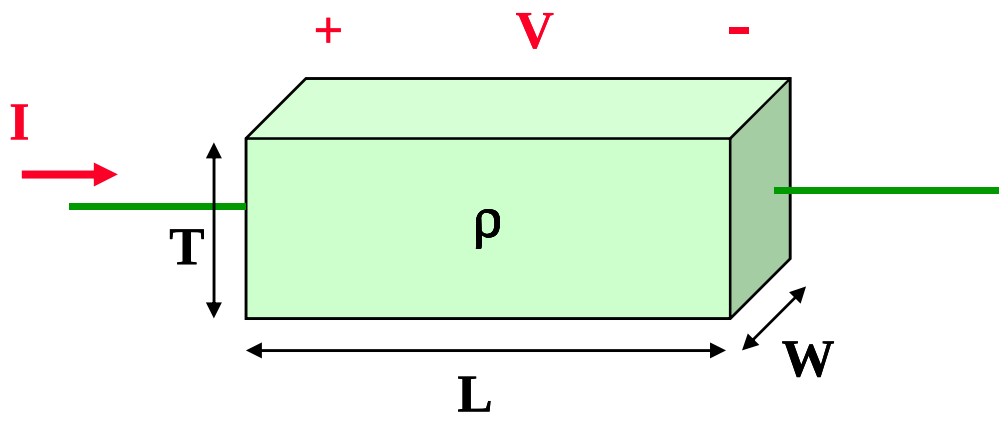
Porta Lógica CMOS (revisão)





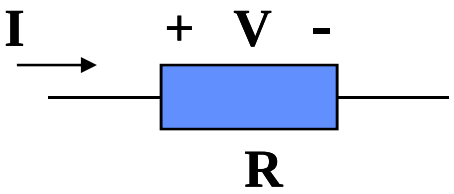
Resistência (R)

$$R = \rho \cdot \frac{L}{W \cdot T}$$

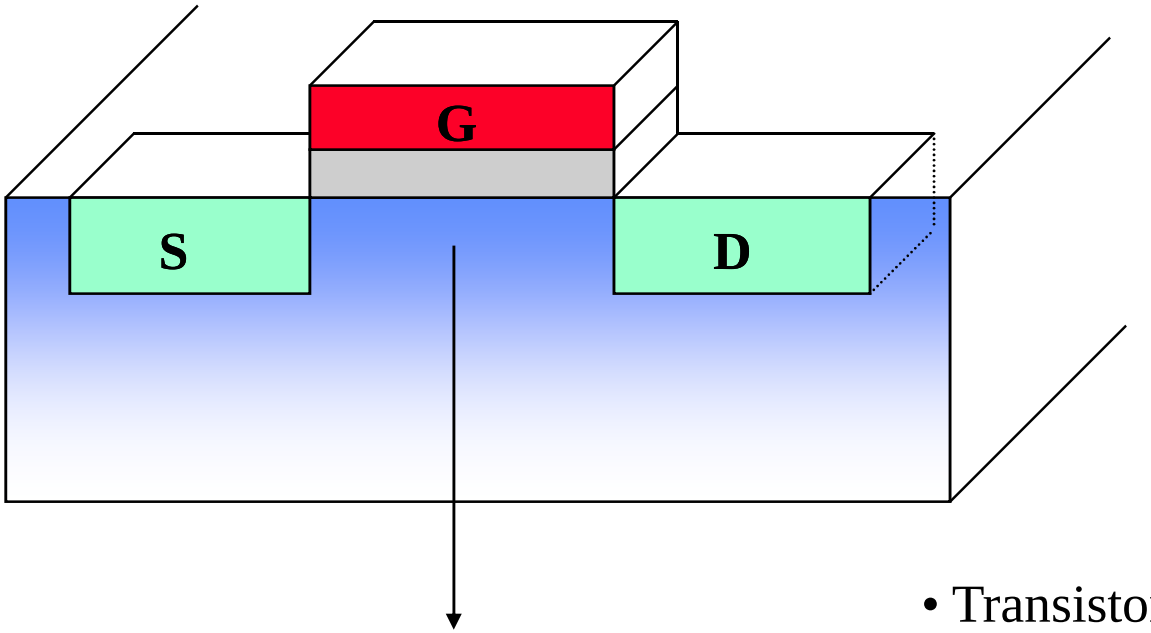


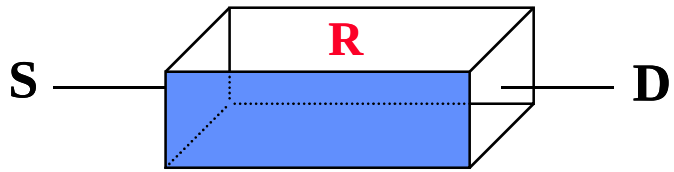
Lei de Ohm:

$$R = V / I$$



Resistência de Canal do Transistor





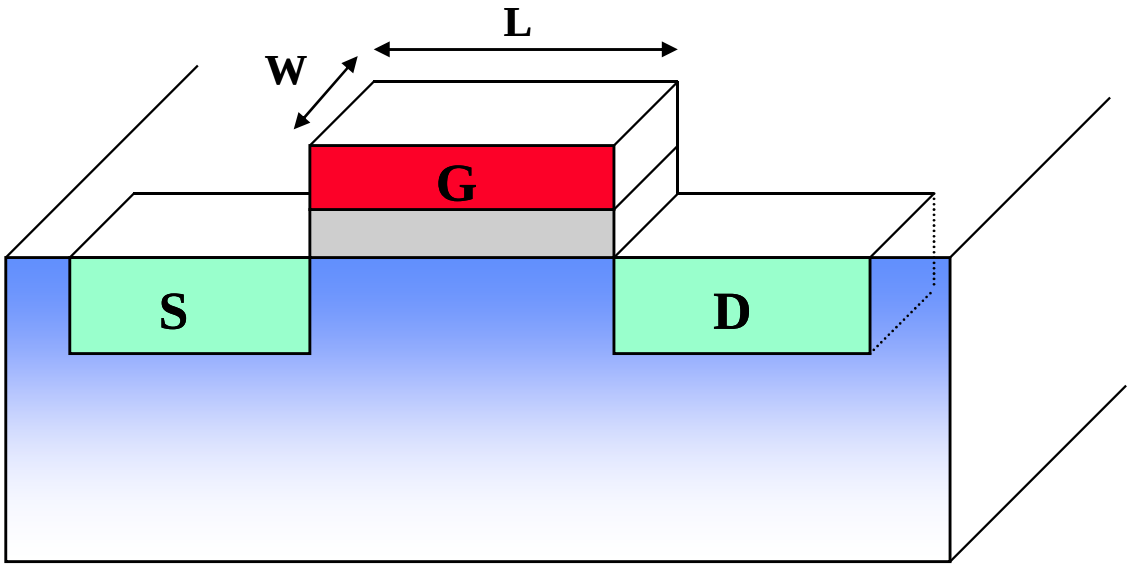
canal do transistor

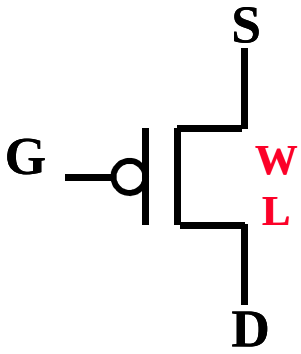
- Transistor não é ‘chave ideal’.
- Canal do transistor $\Rightarrow$ resistência
- Transistor conduzindo:

  resistência pequena ($R \Rightarrow 0$)
- Transistor ‘cortado’:

  resistência muito alta ($R \Rightarrow \infty$)

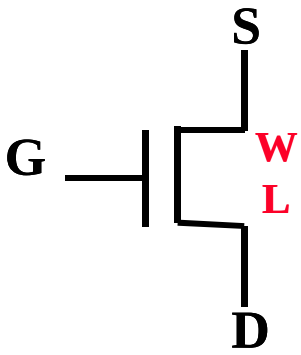
Dimensionamento do Transistor MOS



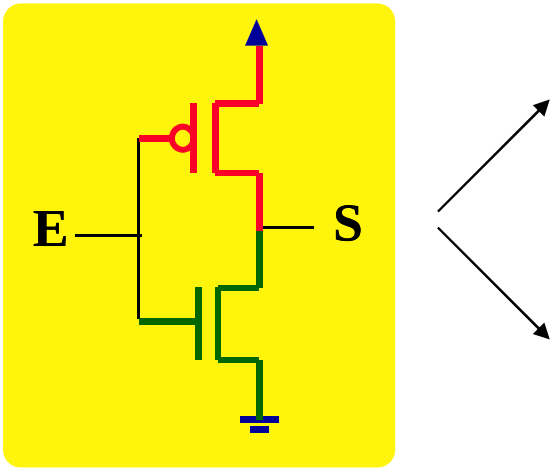


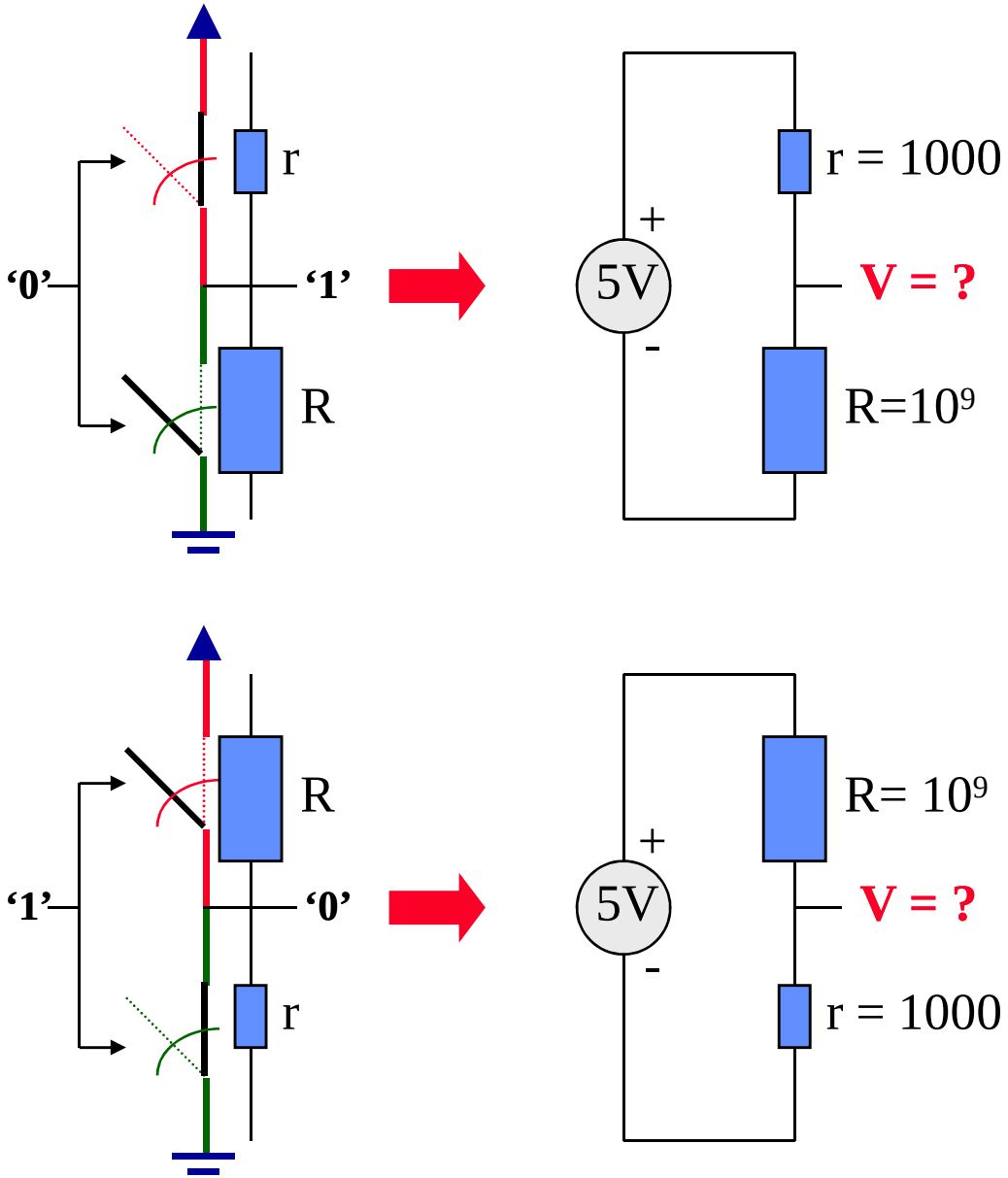
Análise de ‘r’ (‘*on*’) e C:

- W ↑ : r ↓ e C ↑
- L ↑ : r ↑ e C ↑

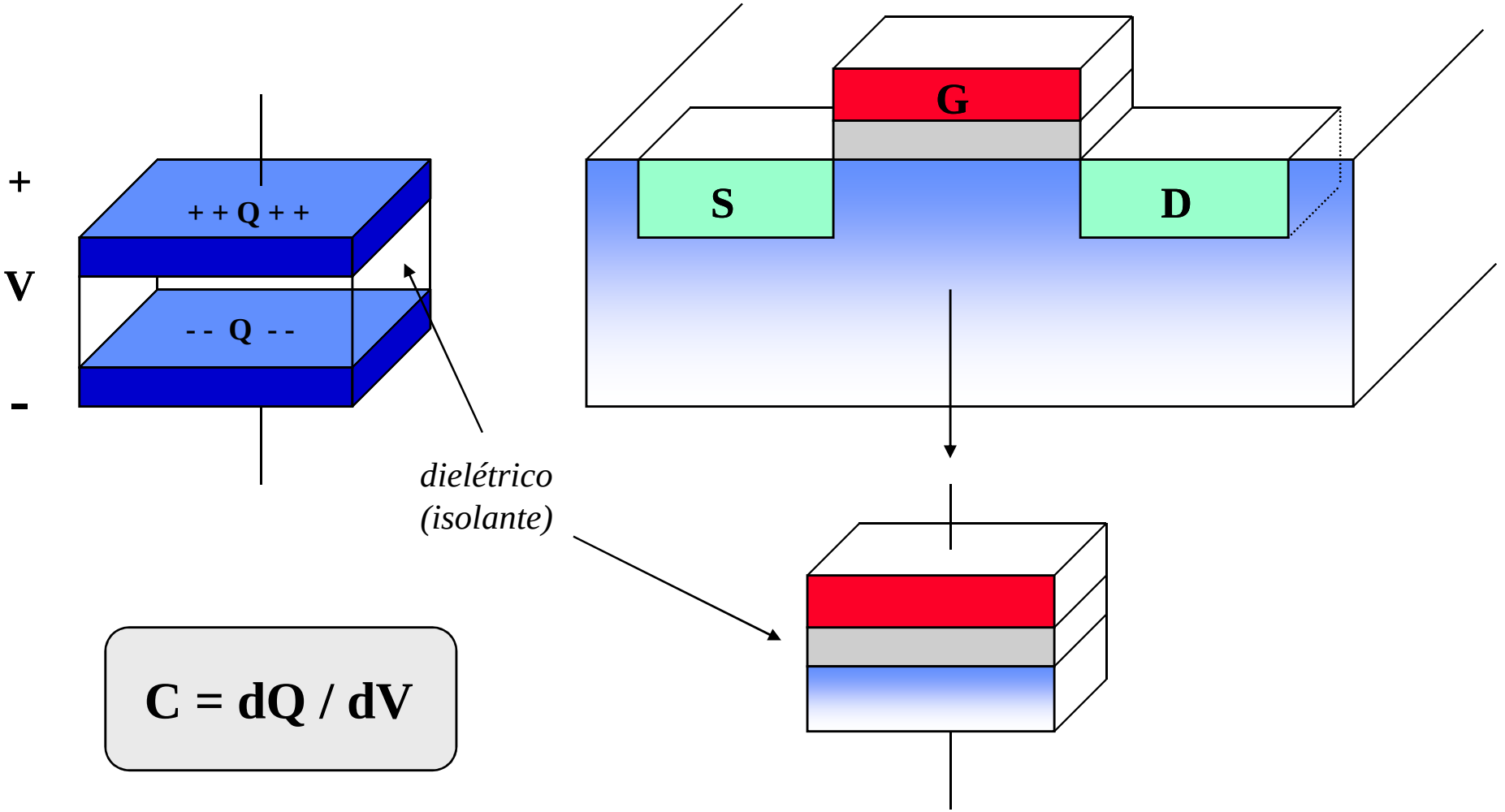


Inversor CMOS : (resistência parasita)



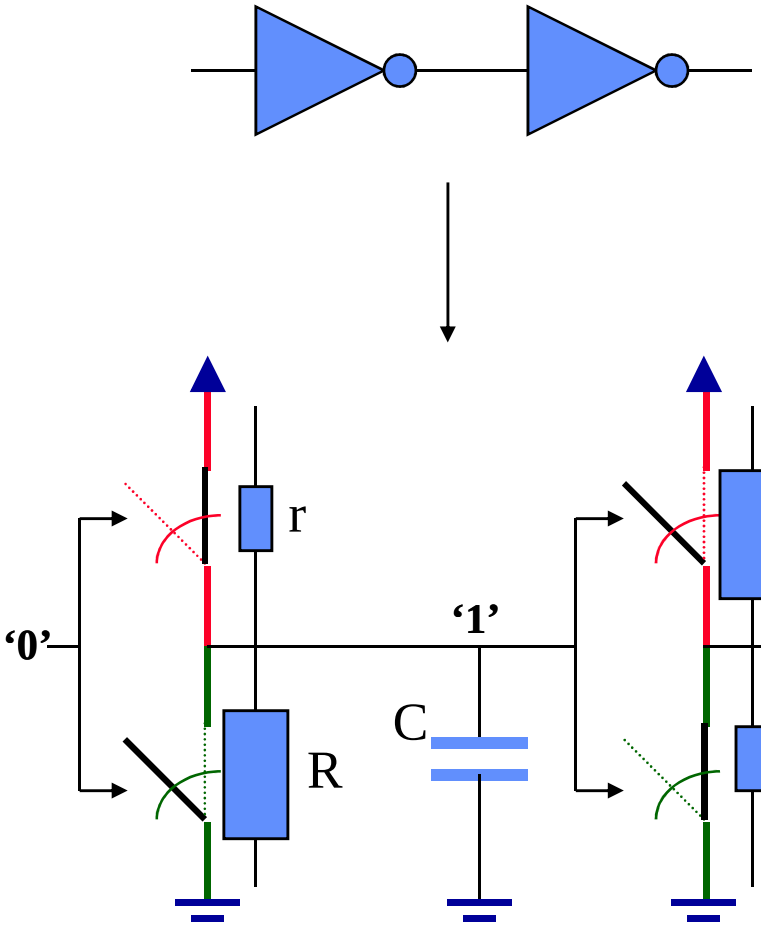


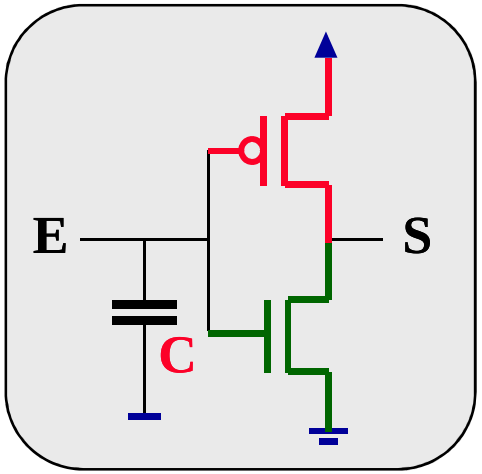
Capacitância (C)

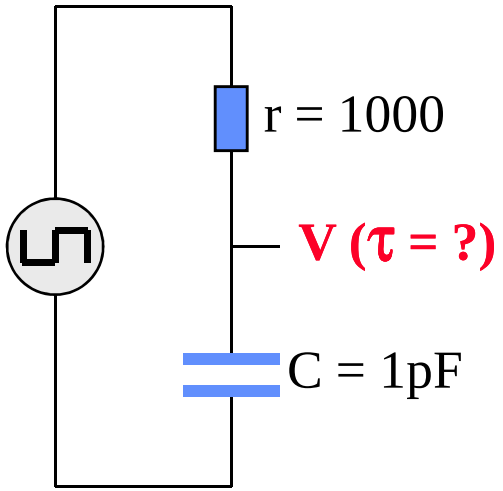


$$C = dQ / dV$$

Inversor CMOS : (capacitância parasita)

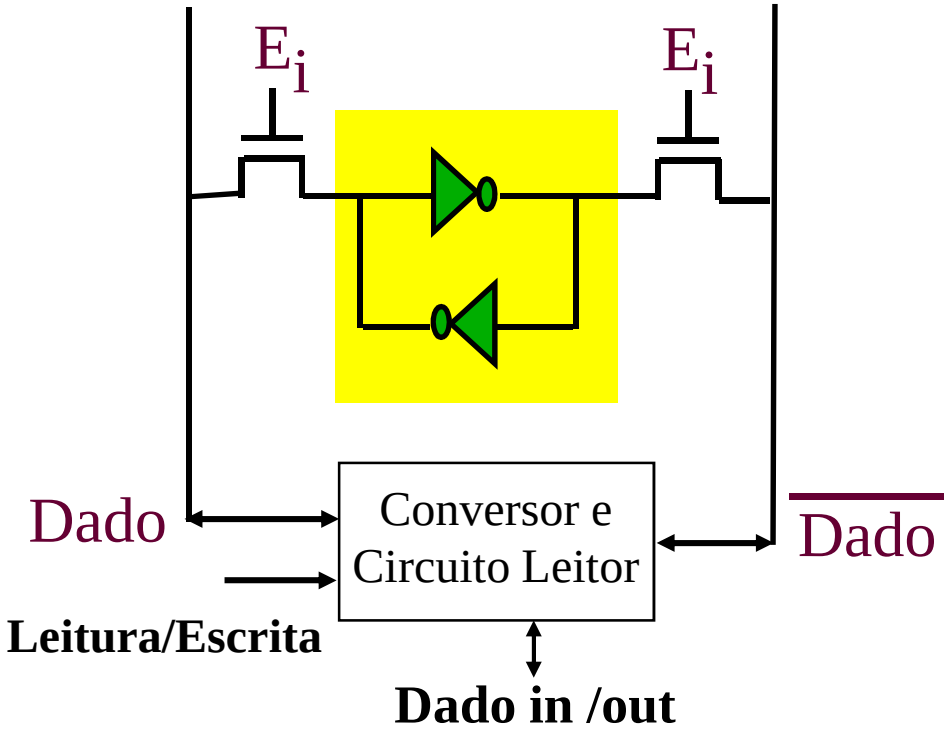




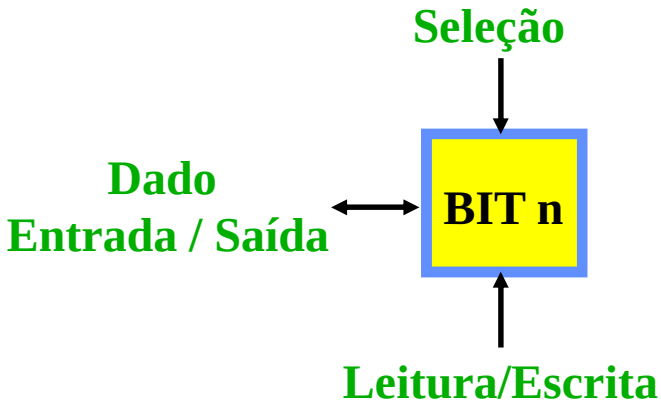


Célula de Memória RAM Estática

Célula de Memória (1 bit)



Memória de Leitura e Escrita

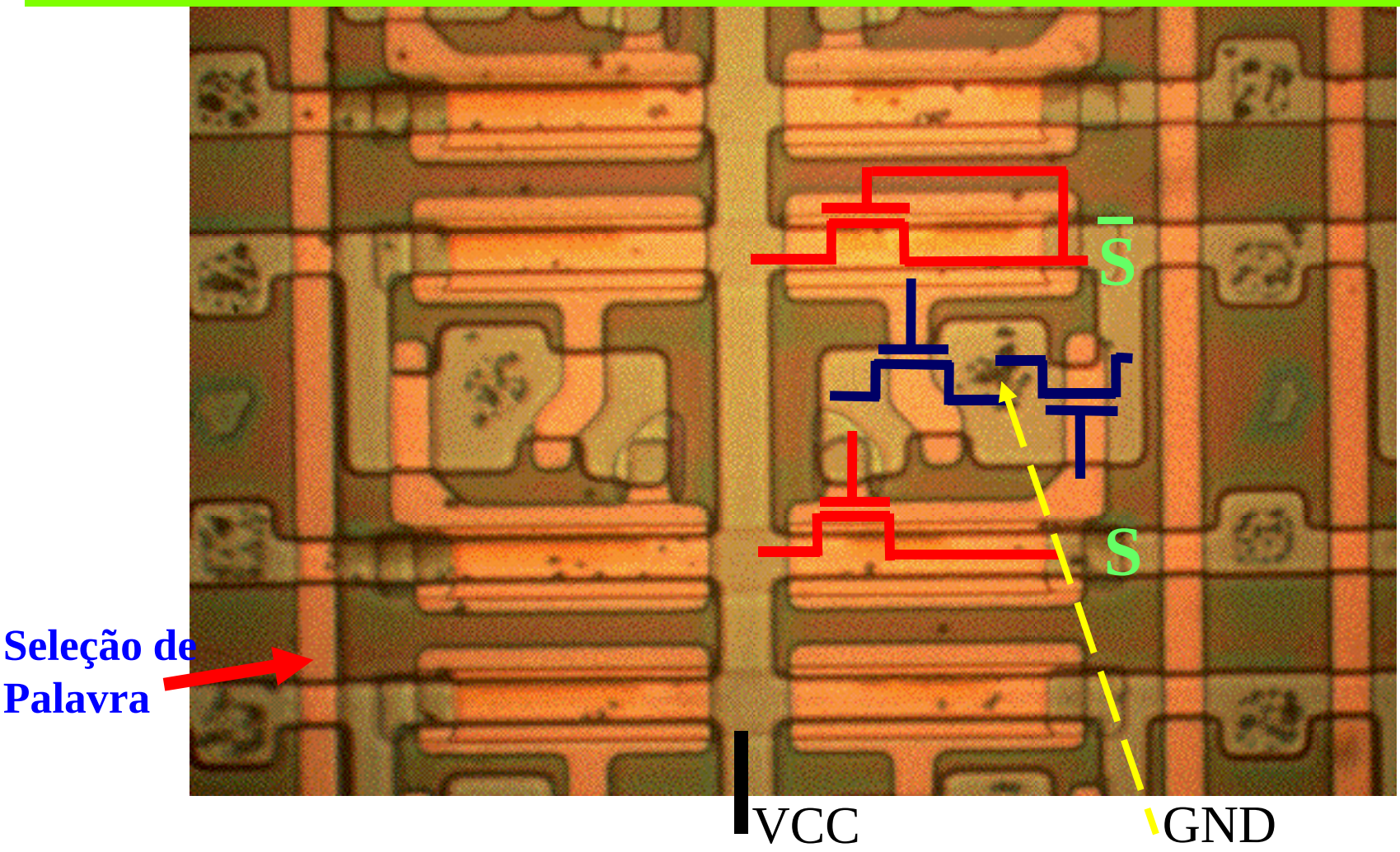


Barramento de dados: Dado e $\overline{\text{Dado}}$

Barramento de endereços: E_i (Seleção da Palavra)

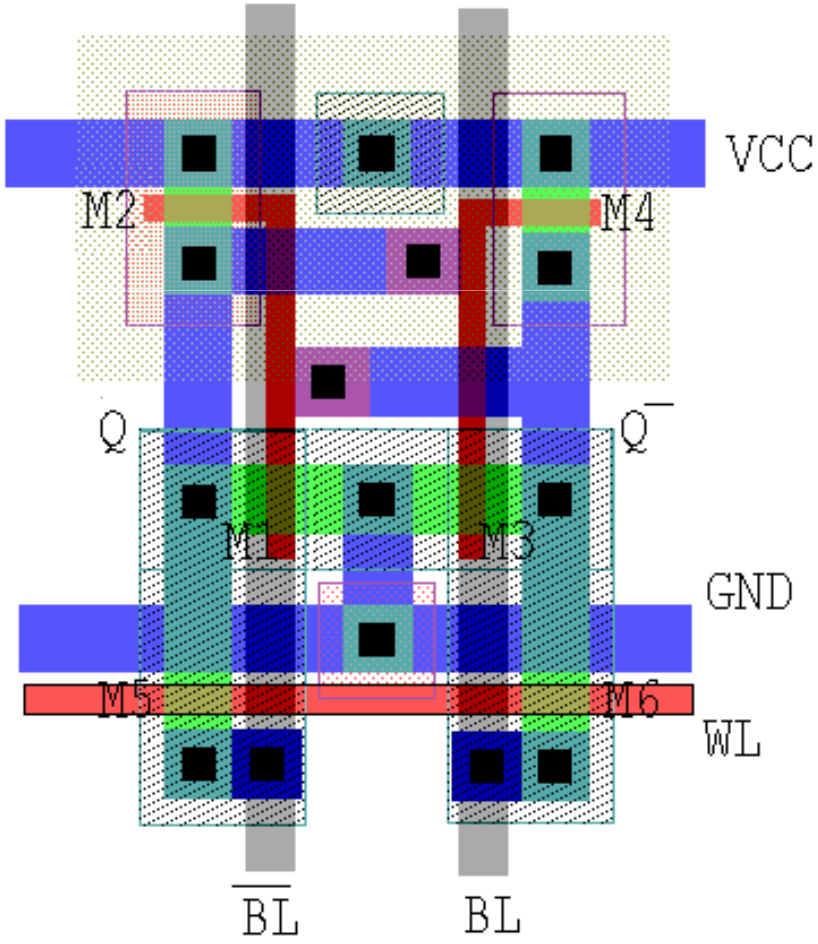
Memória RAM

Célula de Memória RAM do Banco de Registradores do processador 8085 (NMOS)

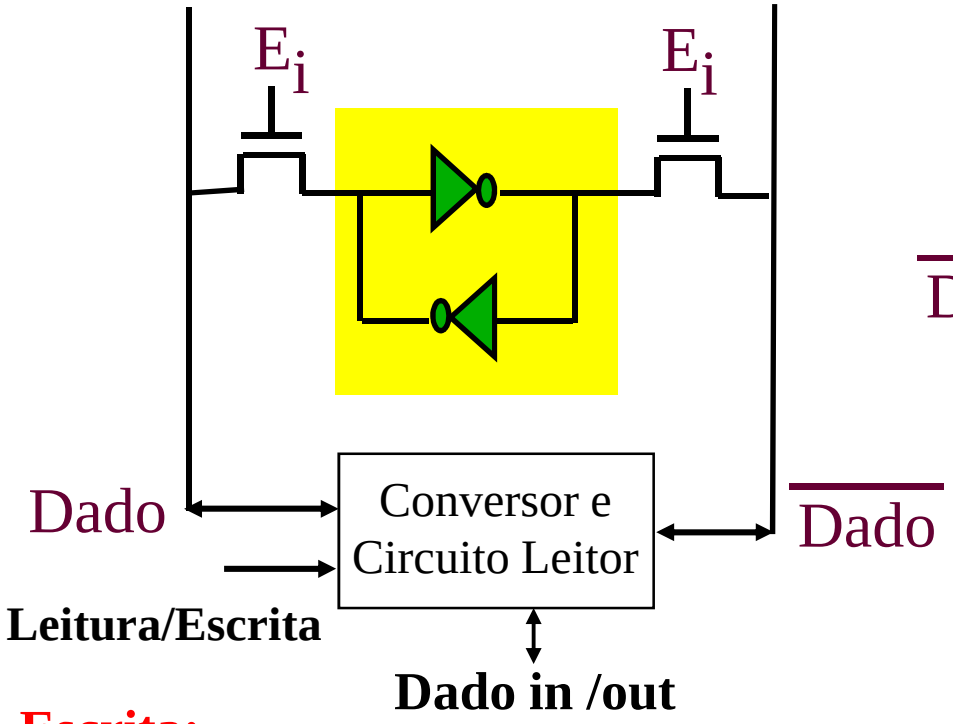


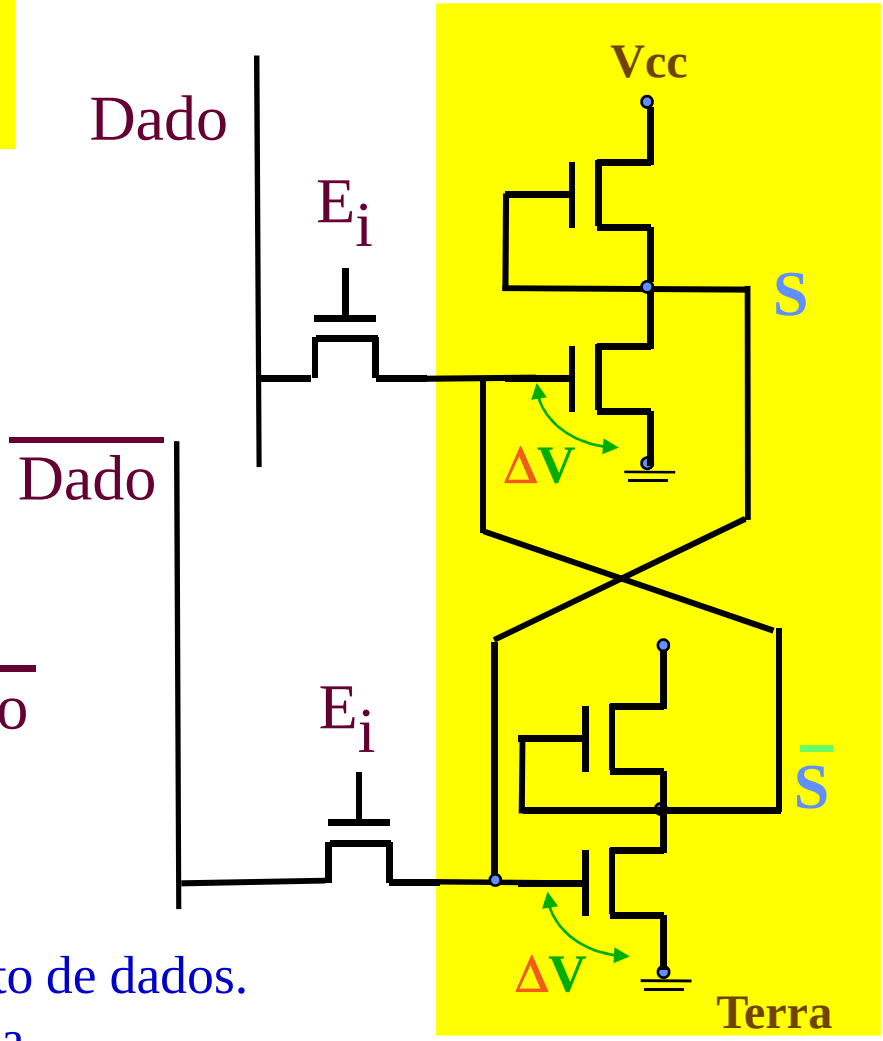
Memória RAM

Layout de uma célula SRAM 6T CMOS



Memória RAM





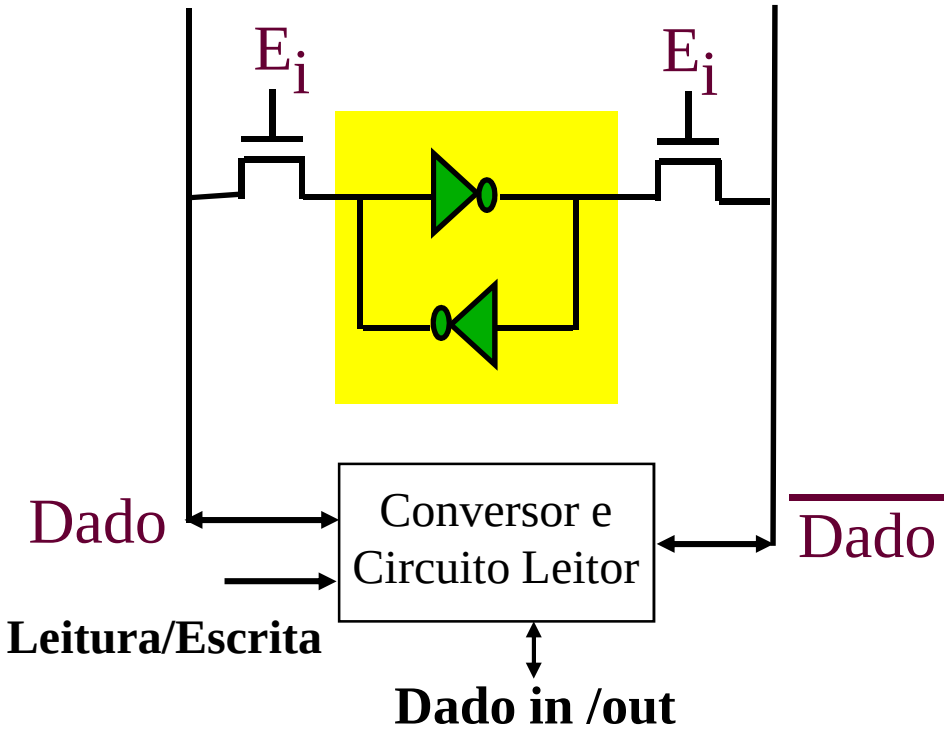
Escrita:

1- Coloca valor a ser escrito no barramento de dados.

2- Aciona endereço da palavra a ser escrita.

3- Valores existentes no barramento de dados são gravados na célula independentemente do valor existente anteriormente, devido a grande capacitância do barramento de dados.

Memória RAM



Pré-Carga

Dado

$\overline{\text{Dado}}$

"1"

Leitura:

1- Carrega-se os barramento com o valor "1" (PRÉ-CARGA).

2- Aciona endereço da palavra a ser lida.

3- Valores existentes na célula memória são transferidos para o barramento, que se descarrega pelo "lado" que está em "zero".