INF01 118

# Técnicas Digitais para Computação

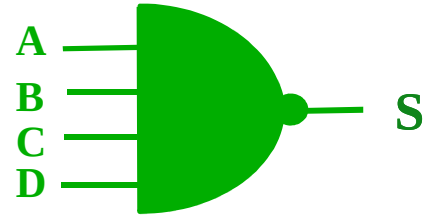
## Portas complexas
## Transmission gates
## Alta impedância

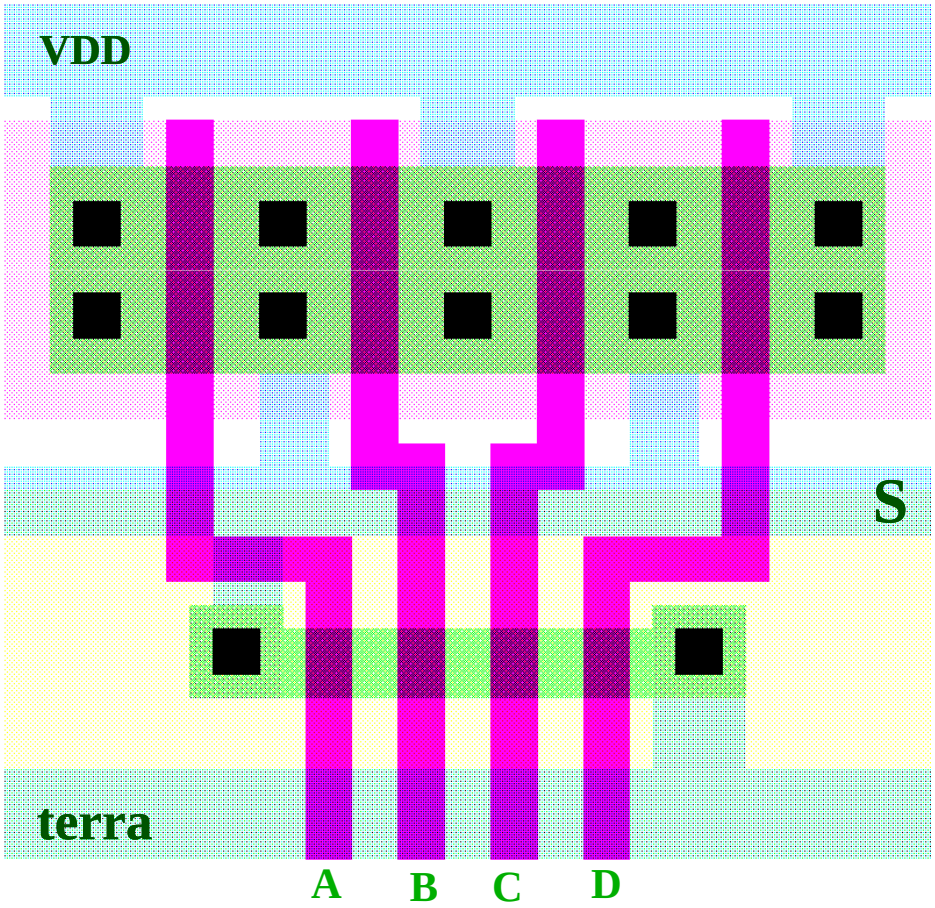
UFRGS

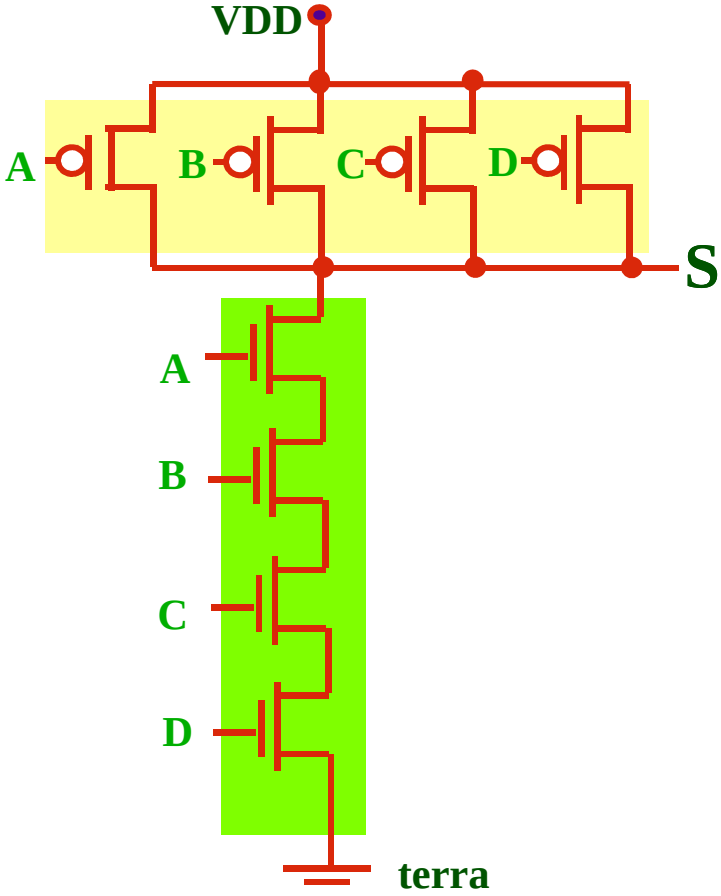
**Aula 5**

# Portas Lógicas

## Porta NAND CMOS



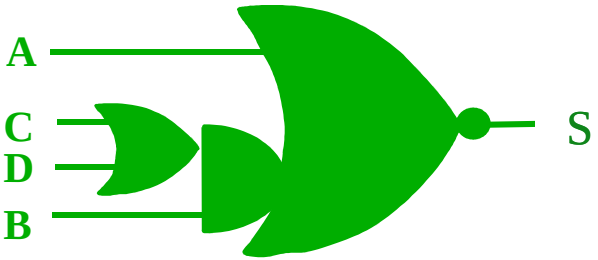



# Portas Lógicas

## Portas CMOS Complexas

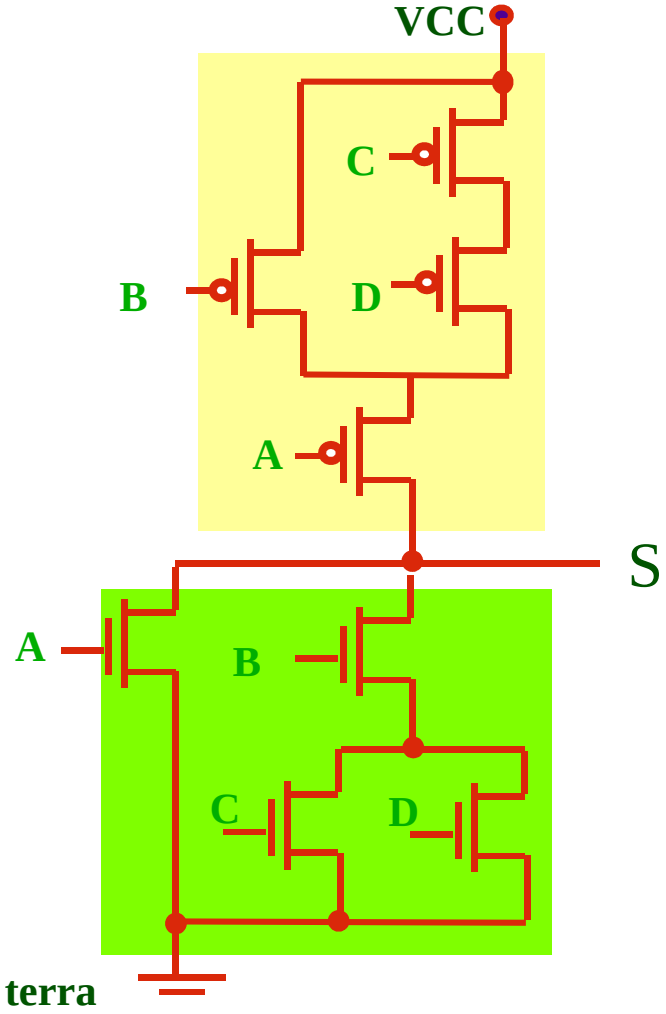
**SCCG** (Static CMOS Complex Gate)

Exemplo:



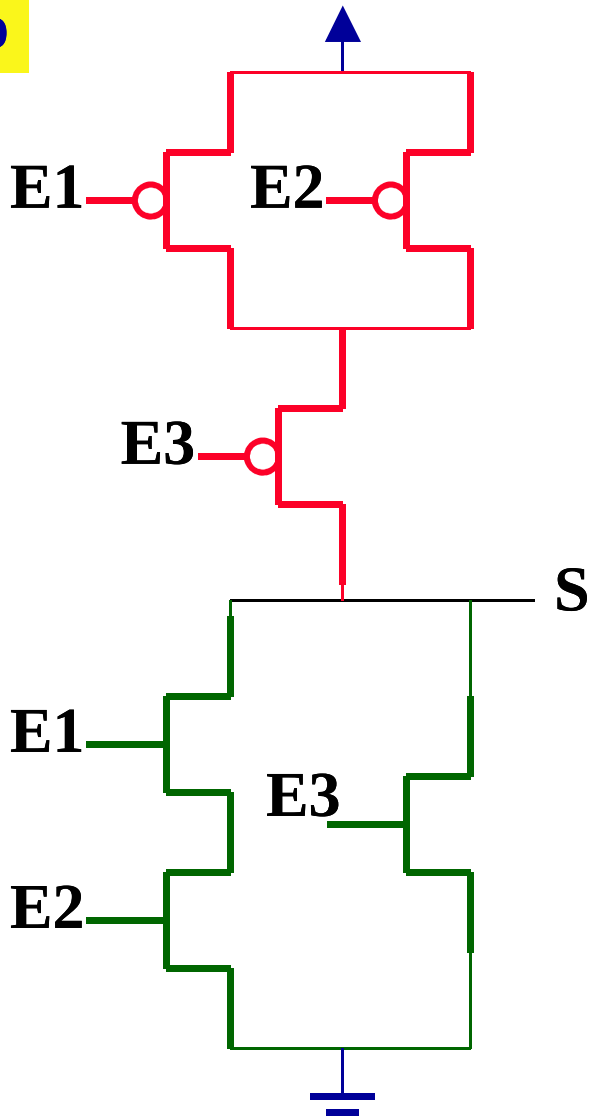

$$S = \overline{A + ( B \,.(C+D))}$$

A lógica da porta pode definida pelos transistores de pull down.

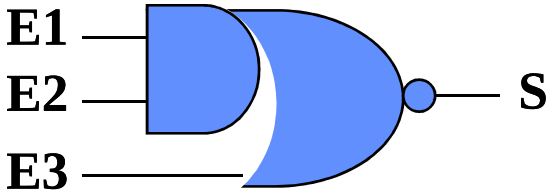


# Portas Lógicas

## Exercício



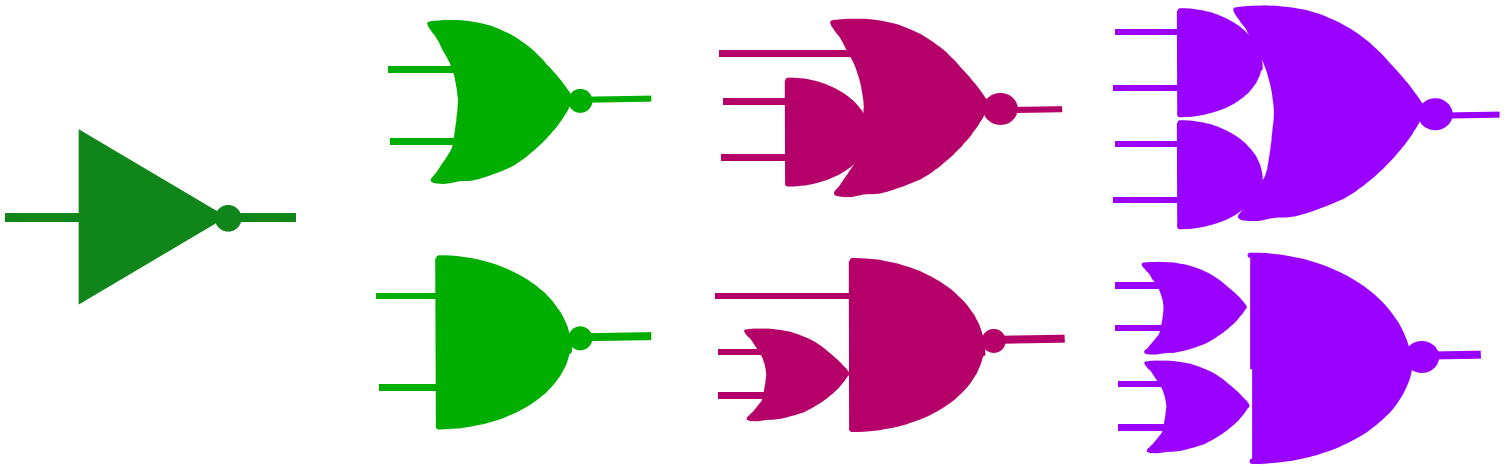

| E1 | E2 | E3 | S |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |



# Portas Lógicas

## Portas CMOS Complexas

**SCCG** (Static CMOS Complex Gate)



Funções com até 2 transistores em série

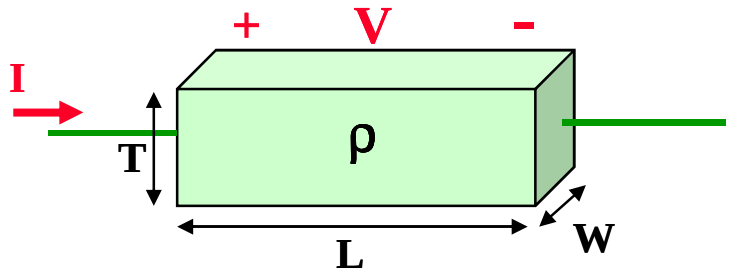
# Dimensionamento de Transistor MOS

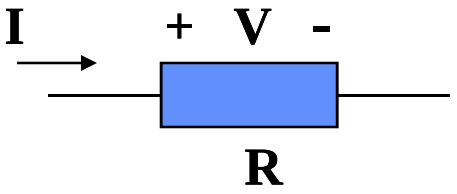
## Revisão de Resistência

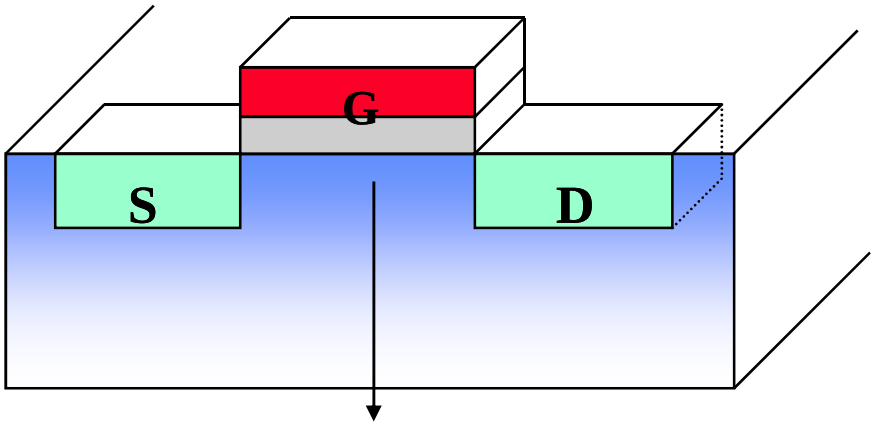
$$R = \rho \cdot \frac{L}{W \cdot T}$$

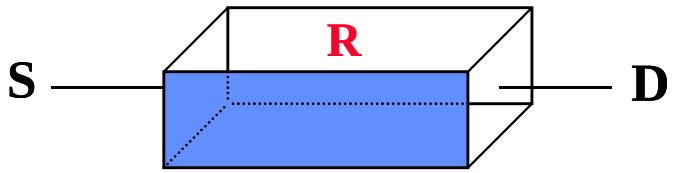
Lei de Ohm:

$$I = V / R$$

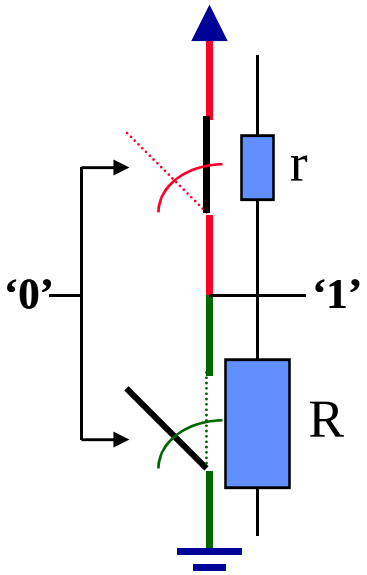


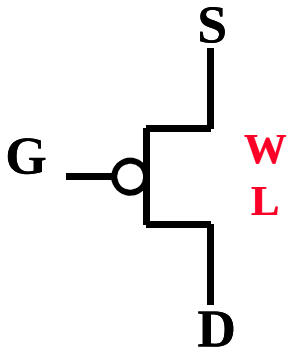




*canal do transistor*

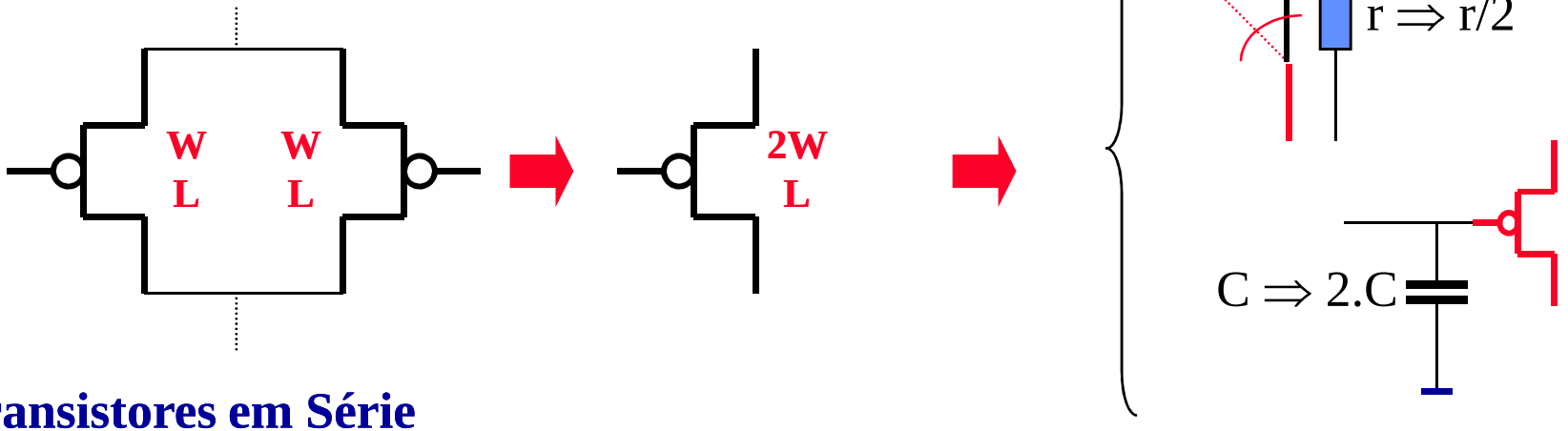



$$\begin{cases} W\uparrow : r\downarrow, C\uparrow \\ L\uparrow : r\uparrow, C\uparrow \end{cases}$$

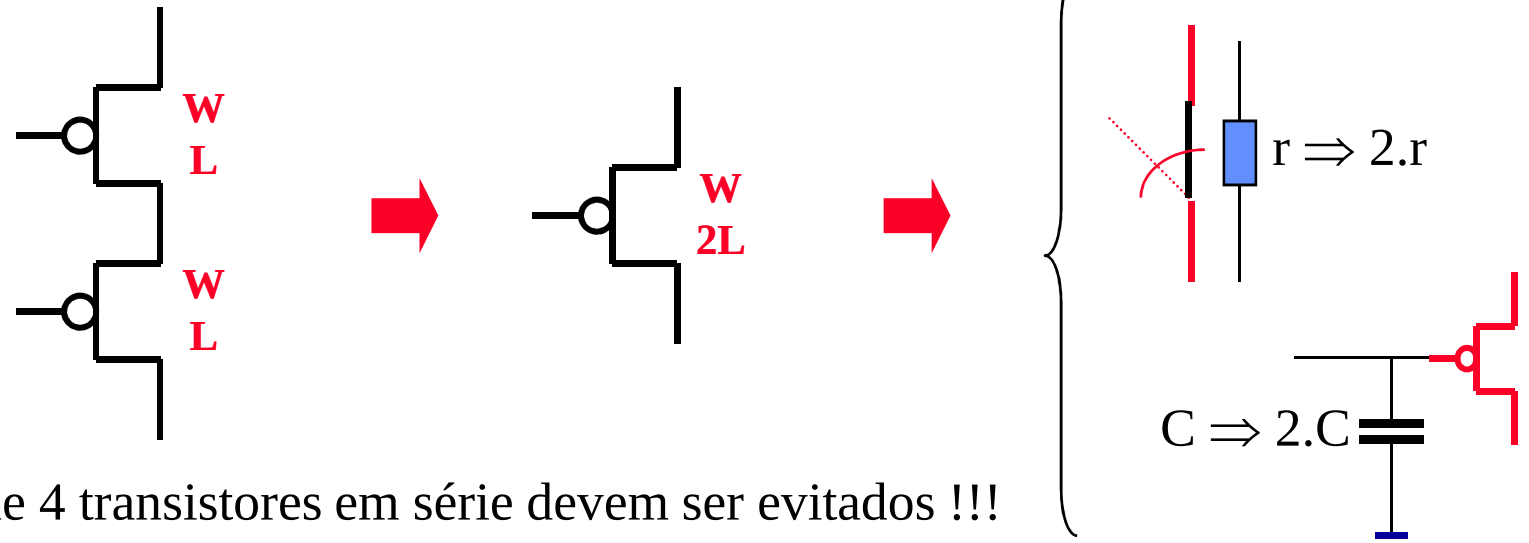


# Associação de Transistores

## Transistores em Paralelo



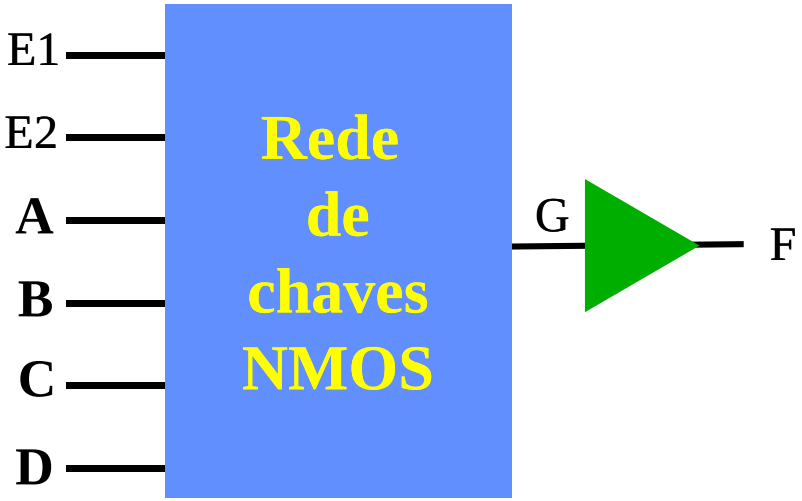

## Transistores em Série

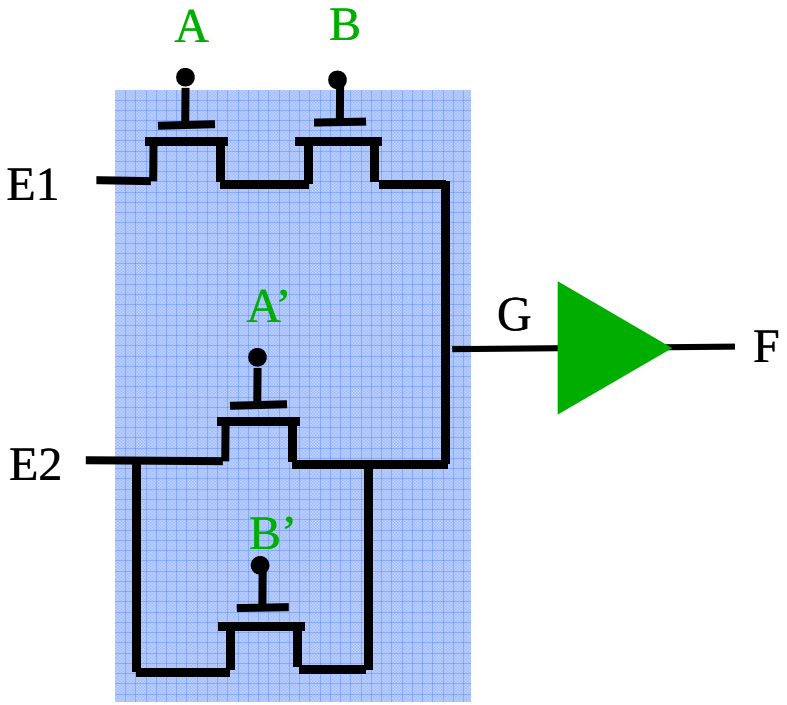



* Mais de 4 transistores em série devem ser evitados !!!

# Portas Lógicas

## Lógica com chaves NMOS

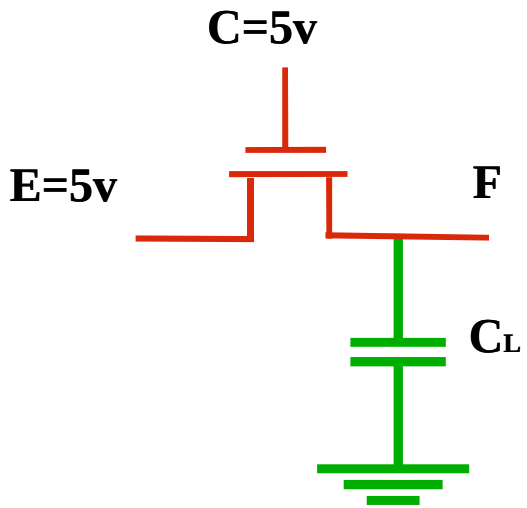



Transistores N
Sem consumo estático
Vg alto varia em função da lógica
O buffer “regenera” o sinal. Por que?

# Portas Lógicas

## Chaves NMOS

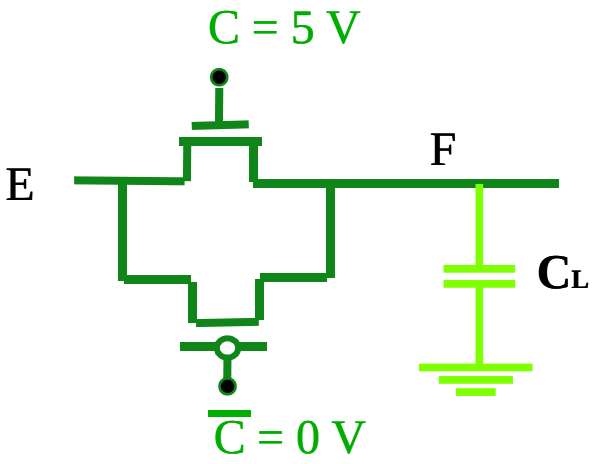



**$V_F$ não consegue atingir 5V, mas 5V -$V_{Tn}$**

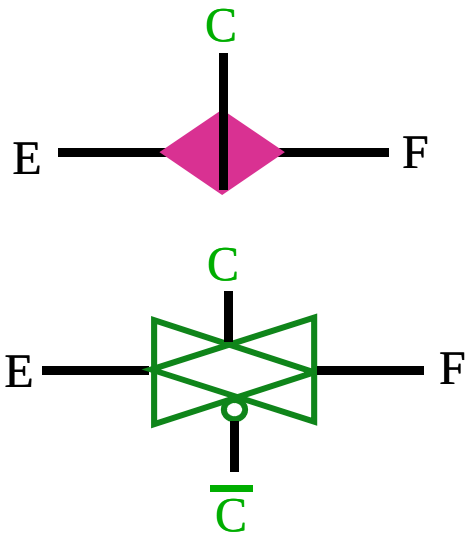
o transistor NMOS passa um 0 forte e um 1 fraco

# Portas Lógicas

## Chaves CMOS




**Símbolos:**




OBS: o transistor PMOS passa um 0 fraco e um 1 forte

o transistor NMOS passa um 0 forte e um 1 fraco

**$R_{eq}$ de uma chave CMOS: cerca de 10 KΩ**

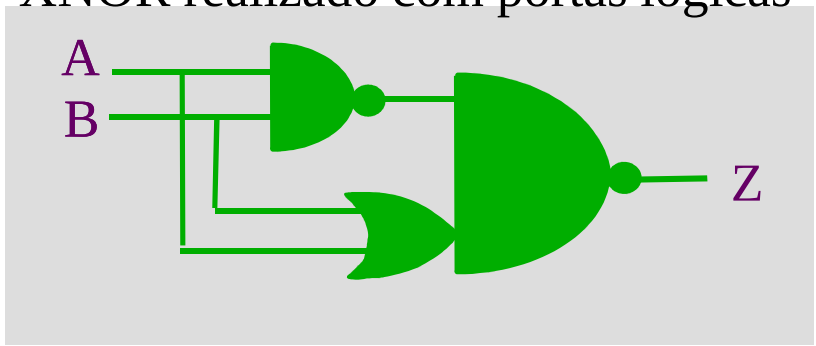
**Desvantagem: temos que ter C e $\overline{C}$**

# Portas Lógicas

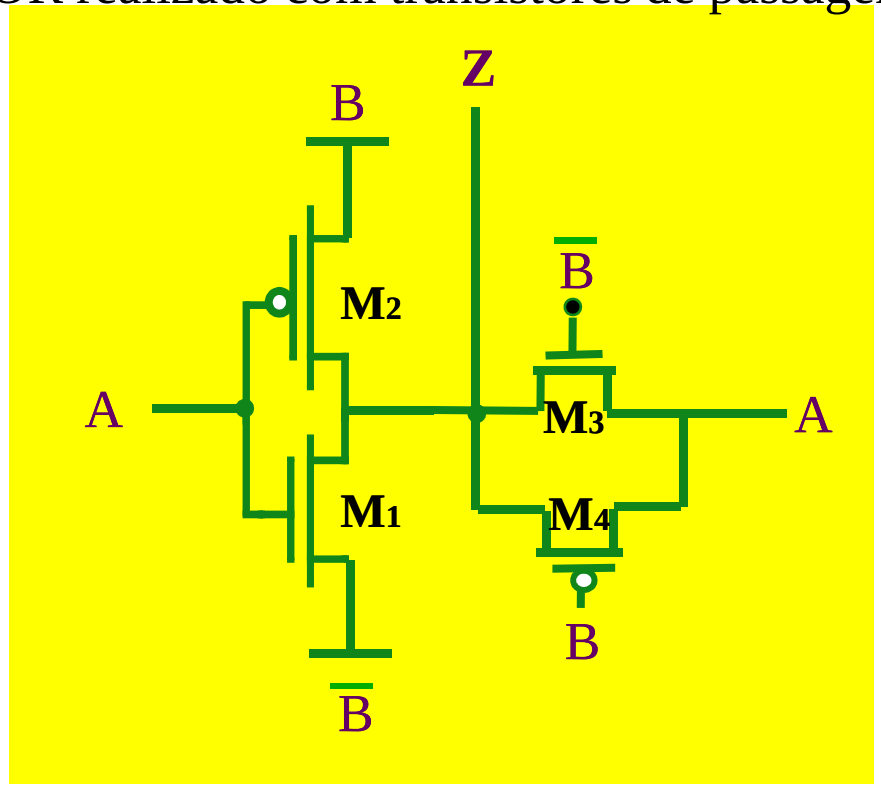
## Lógica com chaves CMOS

### XNOR e XOR

XNOR realizado com portas lógicas

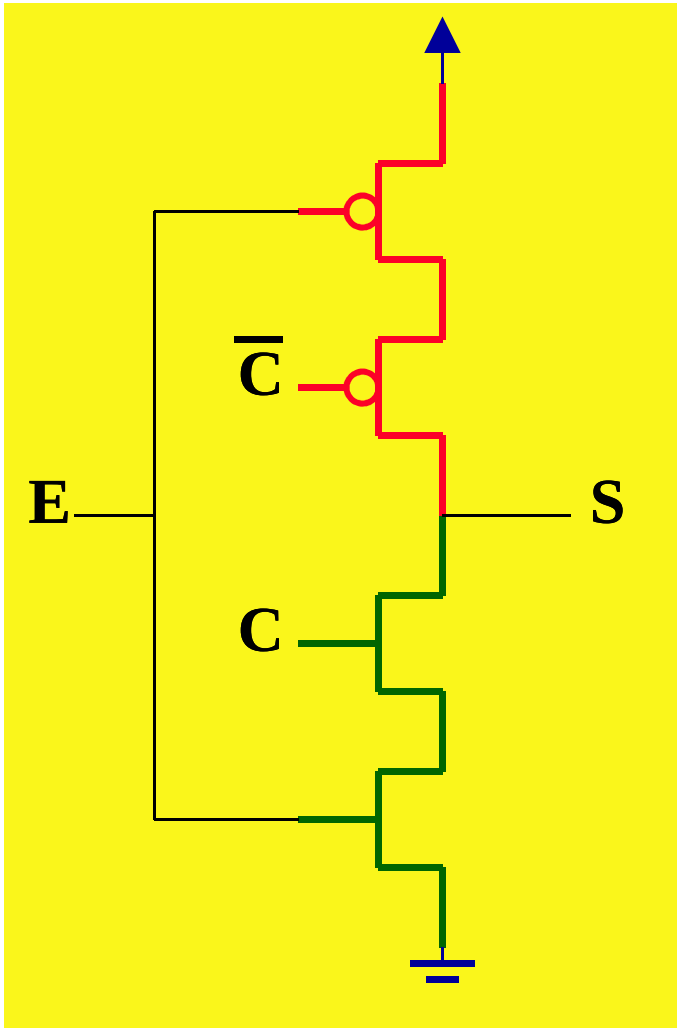


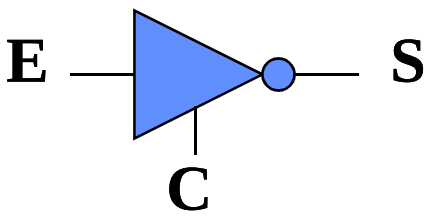

XOR realizado com transistores de passagem



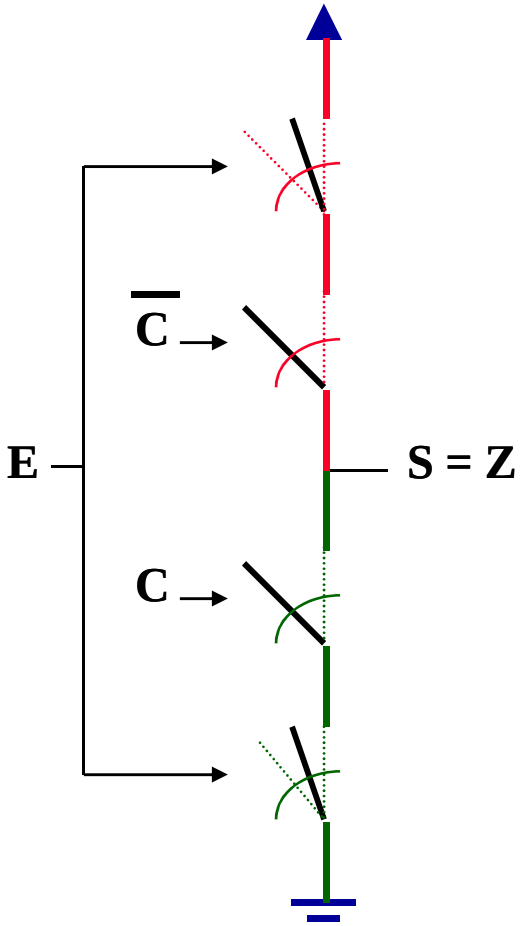
# Alta Impedância (Z)

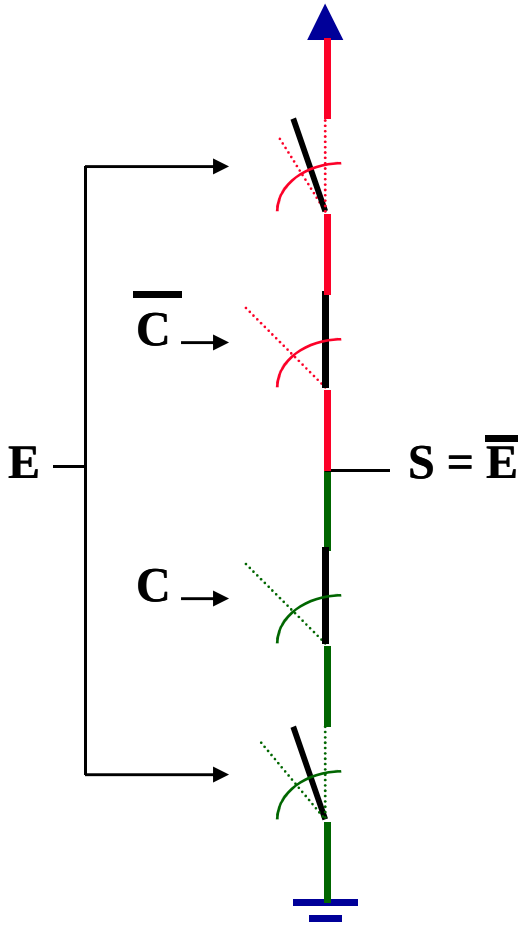
## Inversor Tri-State (INVTR)



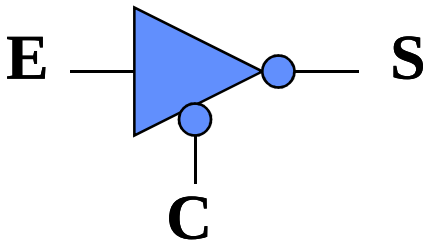




| E | C | $\overline{C}$ | S |
|---|---|---|---|
| 0 | 0 | 1 | Z |
| 1 | 0 | 1 | Z |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 |



## Outra opção... (*controle negado*)

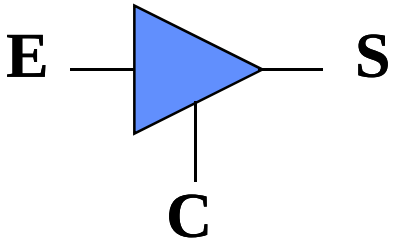



| E | C | S |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | Z |
| 1 | 1 | Z |

*OU*

| C | S |
|---|---|
| 0 | $\overline{E}$ |
| 1 | Z |

## Buffer Tri-State (BUFTR)

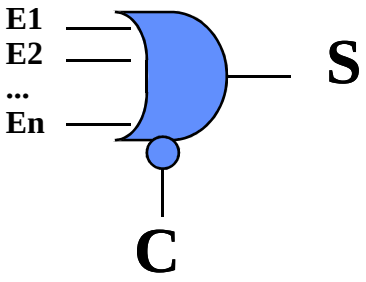


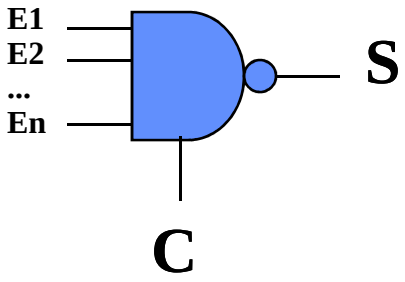

| E | C | S |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | Z |
| 1 | 1 | Z |

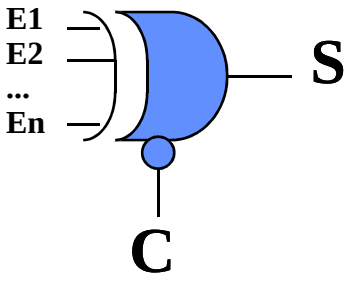
*OU*

| C | S |
|---|---|
| 0 | Z |
| 1 | E |

*** PODE-SE PENSAR EM QUALQUER PORTA LÓGICA COM SAÍDA TRI-STATE OU ALTA-IMPEDÂNCIA (Z) !!!**

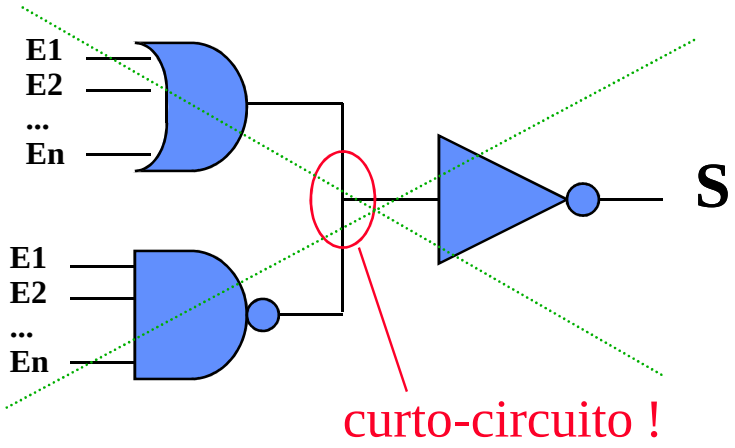


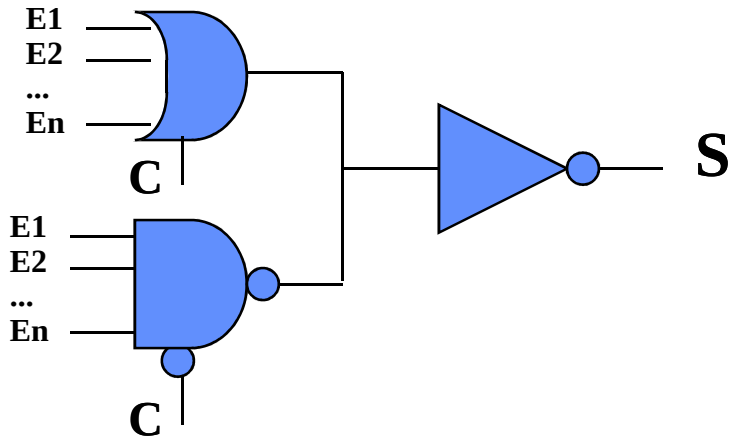



# Uso de Porta Tri-State ...

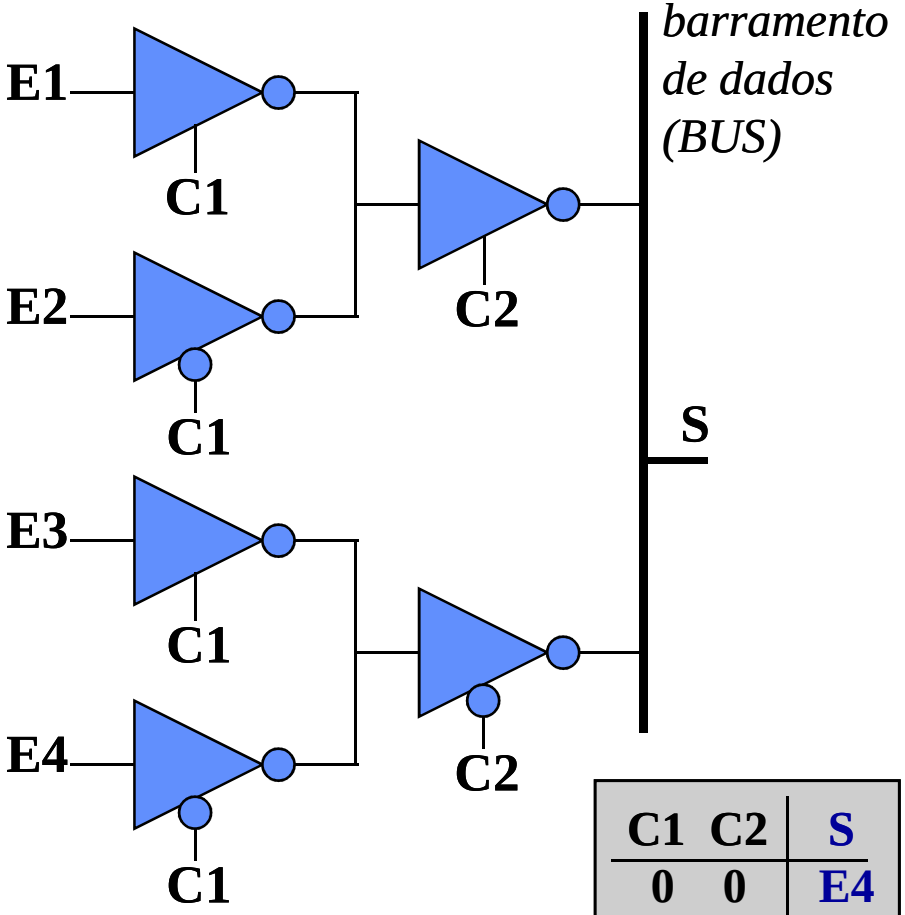
* NÃO É PERMITIDO EM CMOS :




* CORRETO :




* BARRAMENTO DE SINAIS :

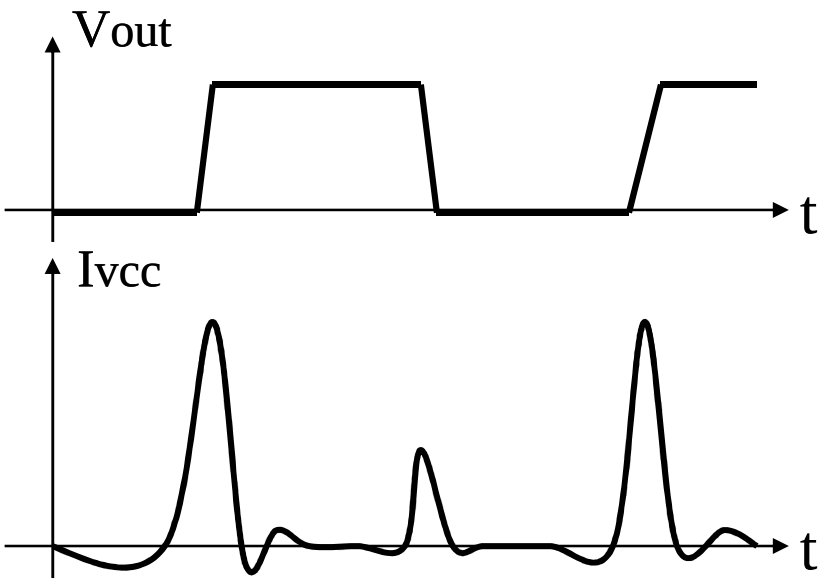


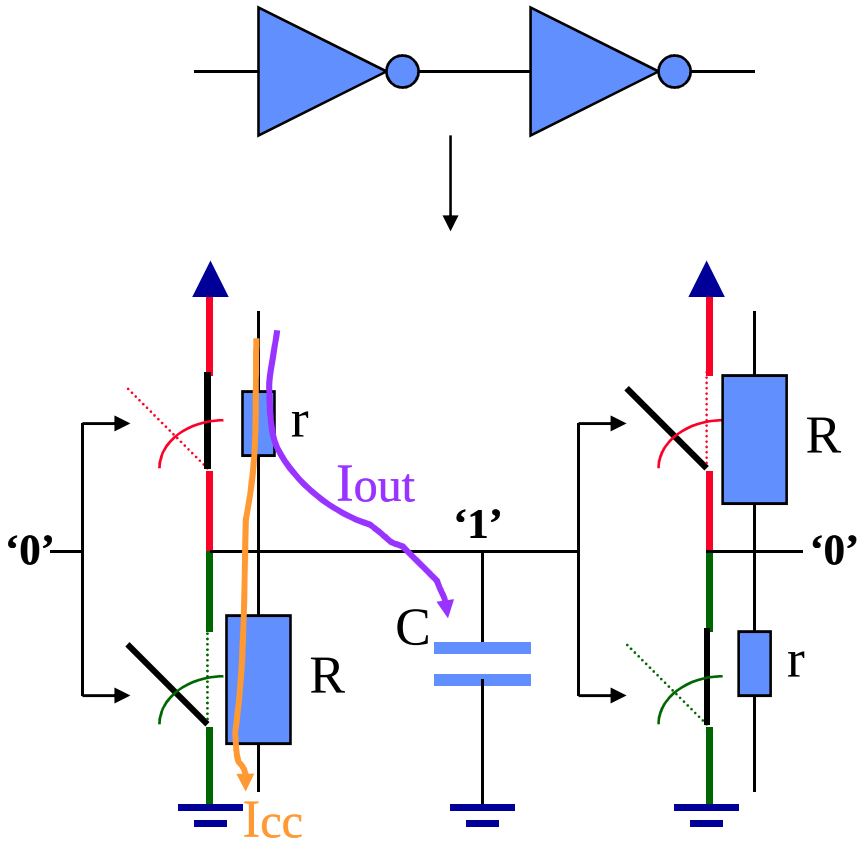

| C1 | C2 | S |
|---|---|---|
| 0 | 0 | E4 |
| 1 | 0 | E3 |
| 0 | 1 | E2 |
| 1 | 1 | E1 |

# Consumo (Dissipação de Potência)

- Corrente de Carga: Iout
- Corrente de Curto-Circuito: Icc

- consumo estático ≈ 0
- consumo dinâmico (transição) = Iout + Icc
- consumo total = estático + dinâmico




* A variação de W e L afeta no tempo de transição dos sinais e no consumo da porta lógica.