

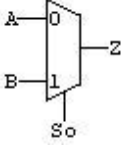
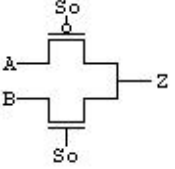
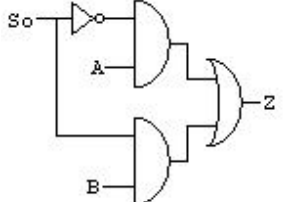
Gabarito Exercícios Área 2

Questão 2

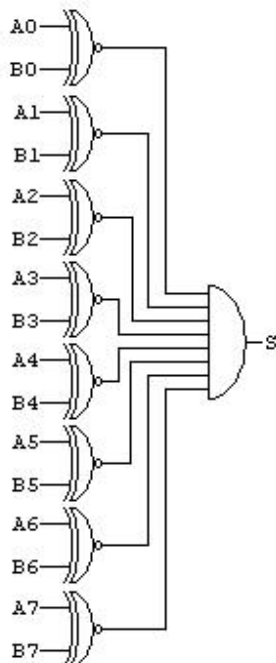
$$Z1 = A \oplus B \oplus C = A'.B'.C + A'.B.C' + A.B'.C' + A.B.C$$

$$Z2 = A.B + B.C + A.C = A.(B+C) + B.C = A.C + B.(A+C) = A.B + C.(A+B)$$

Questão 6

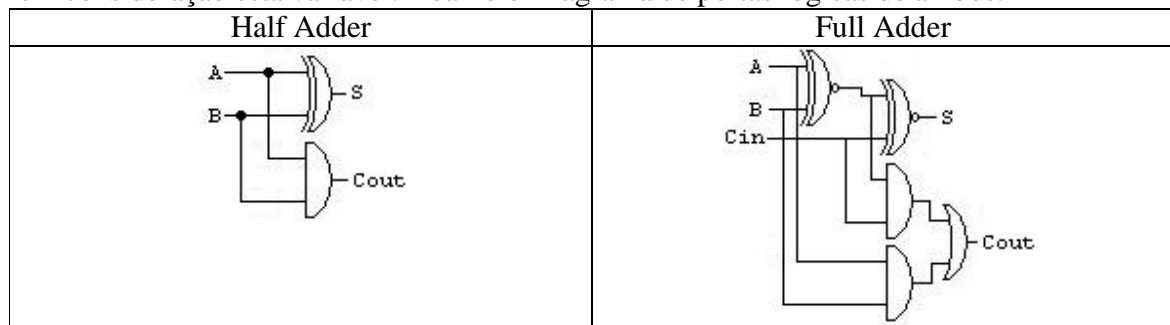
Multiplexador	Transistores de Passagem	Portas Lógicas CMOS
		
	2 Transistores	1 INV = 2 transistores 2 AND = 12 transistores 1 OR = 6 transistores TOTAL = 20 transistores

Questão 8



Questão 10

O Half Adder não considera o Carry de entrada na sua soma, enquanto o Full Adder leva em consideração esta variável. Abaixo o Diagrama de portas lógicas de ambos:



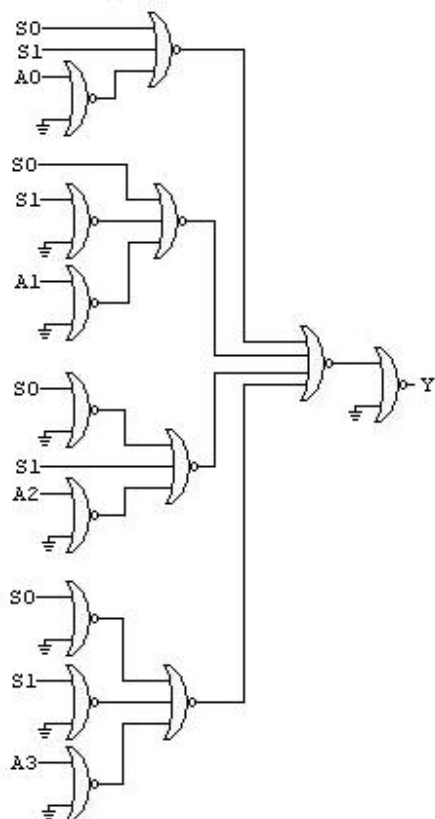
Questão 12

$$y = S0'.S1'.A0' + S0'.S1.A1 + S0.S1'.A2 + S0.S1.A3$$

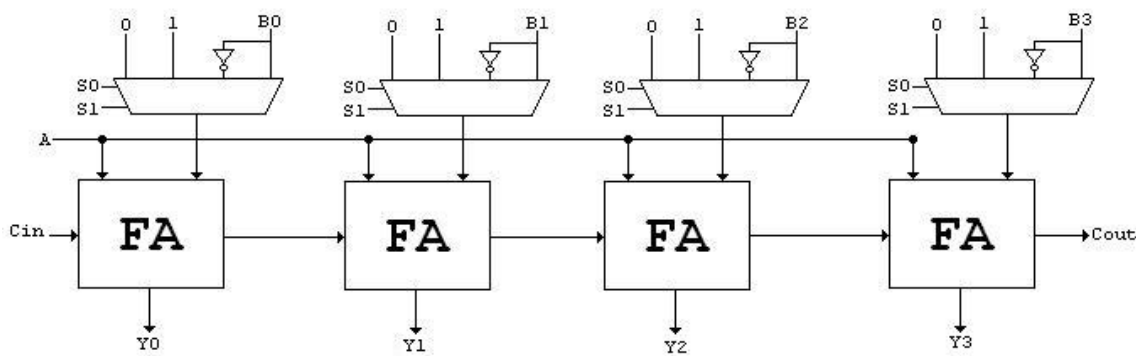
$$y' = (S0 + S1 + A0') \cdot (S0 + S1' + A1') \cdot (S0' + S1 + A2') \cdot (S0' + S1' + A3')$$

$$y = (S0 + S1 + A0')' + (S0 + S1' + A1')' + (S0' + S1 + A2')' + (S0' + S1' + A3')'$$

$$y' = ((S0 + S1 + A0')' + (S0 + S1' + A1')' + (S0' + S1 + A2')' + (S0' + S1' + A3')')'$$



Questão 22

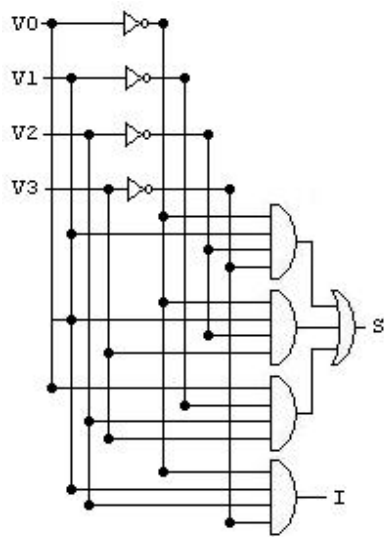


S0	S1	Função
0	0	$A + B$
0	1	$A - B$
1	0	$A + 1$
1	1	$A - 1$

Questão 24

Morador	Código (V3,V2,V1,V0)
A	0010
B	1010
C	1101
D	0110

$$S = V0'.V1.V2'.V3' + V0'.V1.V2'.V3 + V0.V1'.V2.V3$$
$$I = V0'.V1.V2.V3'$$



Questão 26

Tabela Verdade

G1	G0	S1	S0	Z1	Z0
0	0	0	0	1	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	0
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	0

Mapa de Karnaugh Z1

S1S0/ G1G0	00	01	11	10
00	1	0	0	0
01	1	0	0	0
11	1	1	0	0
10	1	1	0	1

Mapa de Karnaugh Z2

S1S0/ G1G0	00	01	11	10
00	1	1	1	1
01	0	0	1	1
11	0	0	1	0
10	0	0	0	0

Função Lógica:

$$Z1 = G1.S1' + S1'.S0' + S0'.G1.G0'$$

$$Z2 = G1'.G0' + S1.G0' + S'.S0.G0$$