i.

$$S = Cin'(A'B + AB') + Cin(A'B + AB)' \qquad ; Doble\ XOR$$

$$Cout = CinA + CinB + AB \qquad ; SOP$$

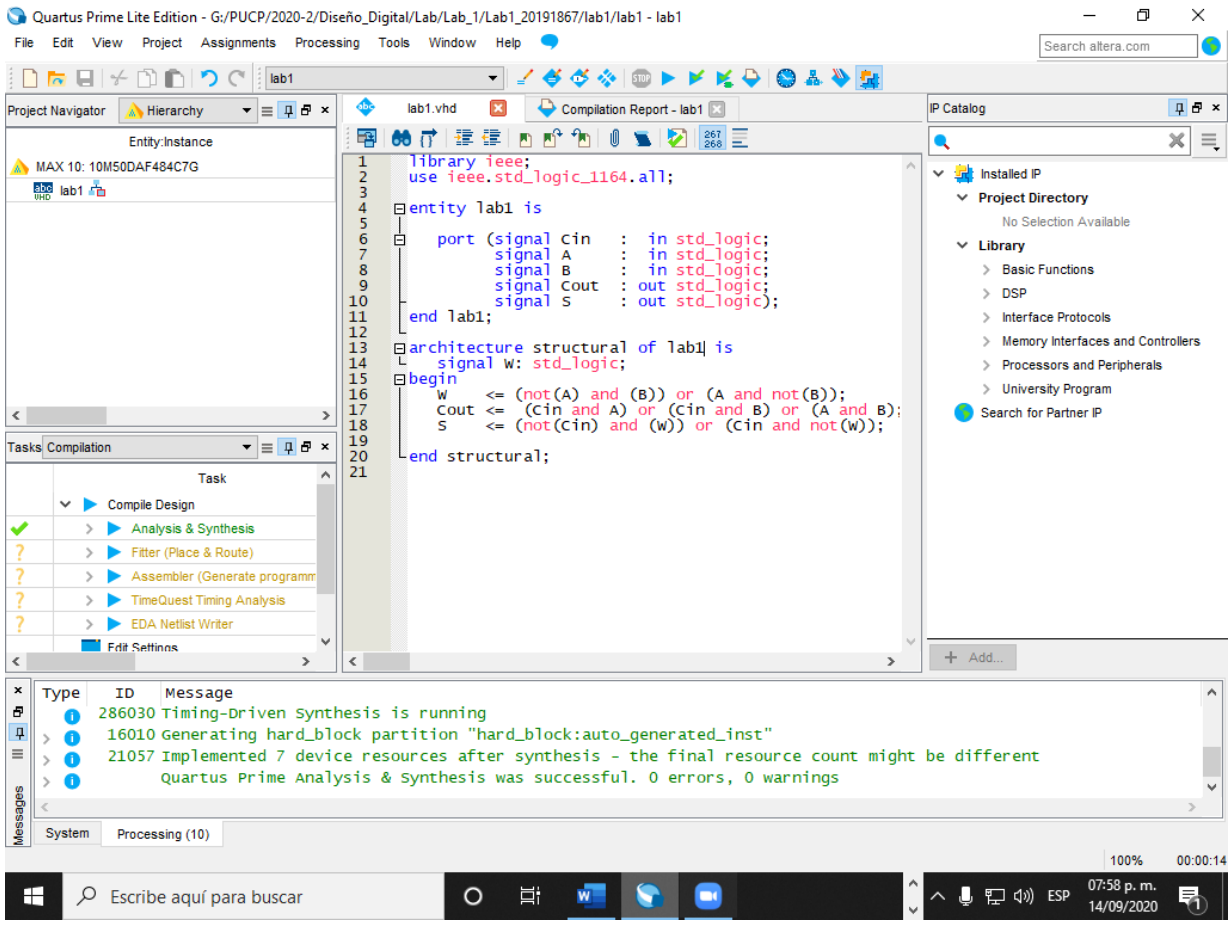
---

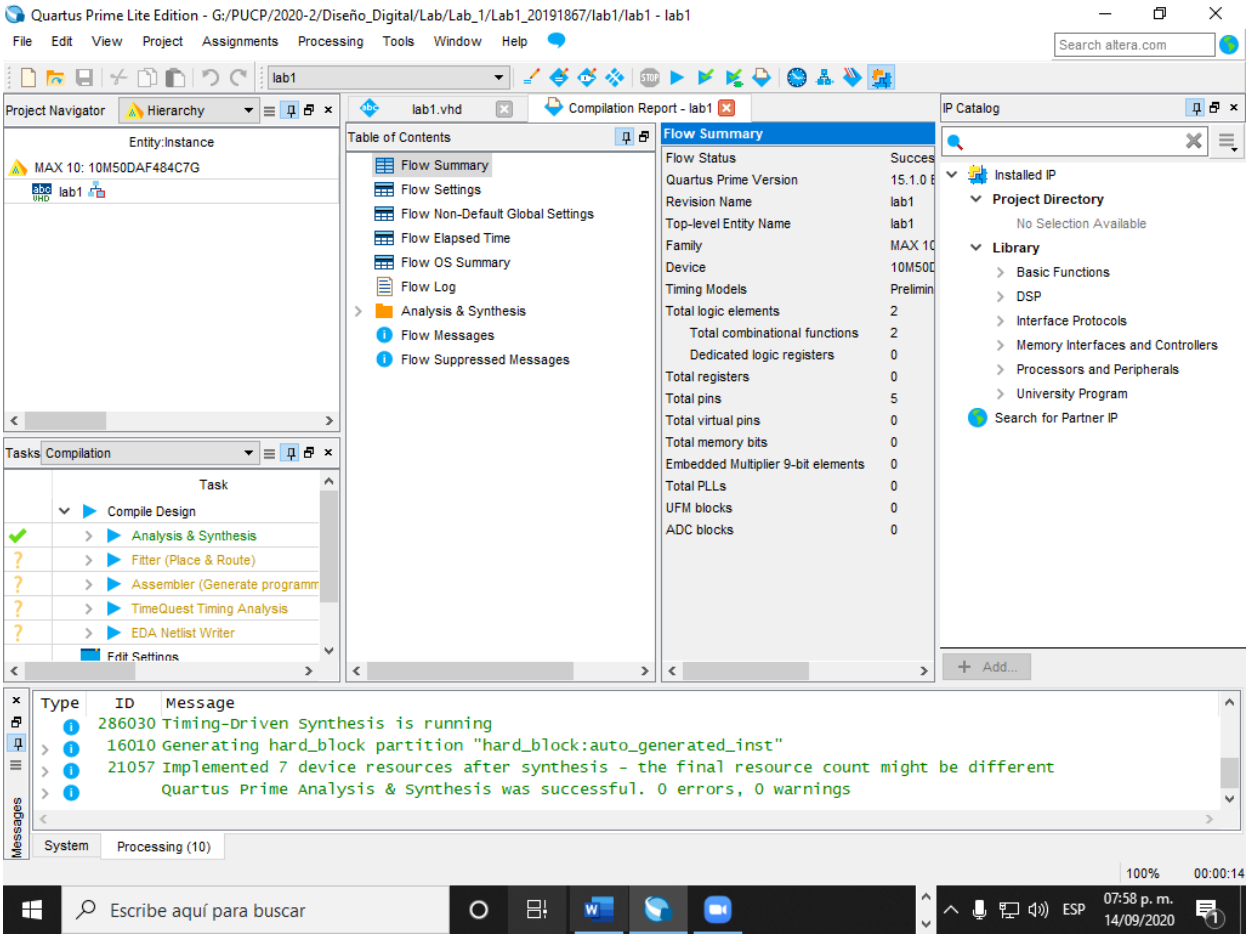
ii.

Nro	Entradas			Acarreo	Suma
Fila	Cin	A	B	Cout	S
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	1

---

iii.




Quartus Prime Lite Edition - G:/PUCP/2020-2/Diseño_Digital/Lab/Lab_1/Lab1_20191867/lab1/lab1 - lab1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator
Hierarchy
Entity:Instance
MAX 10: 10M50DAF484C7G
lab1
lab1.vhd
Compilation Report - lab1
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Flow Summary
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Flow Elapsed Time
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Flow Messages
Flow Suppressed Messages
Flow Summary
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Revision Name
Top-level Entity Name
Family
Device
Timing Models
Total logic elements
Total combinational functions
Dedicated logic registers
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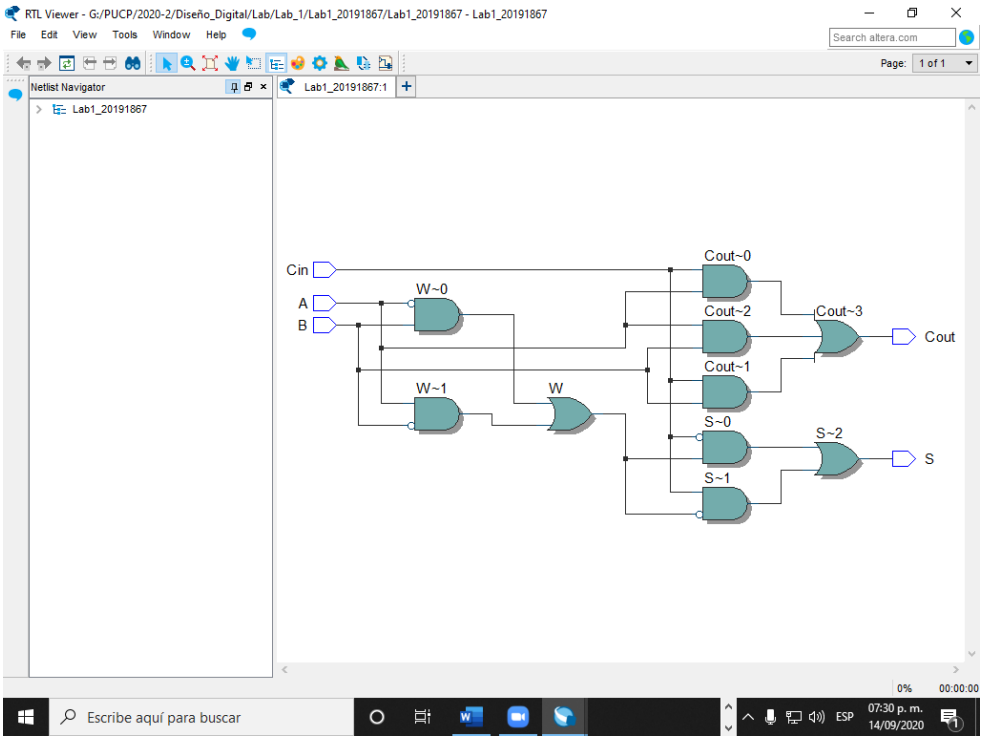
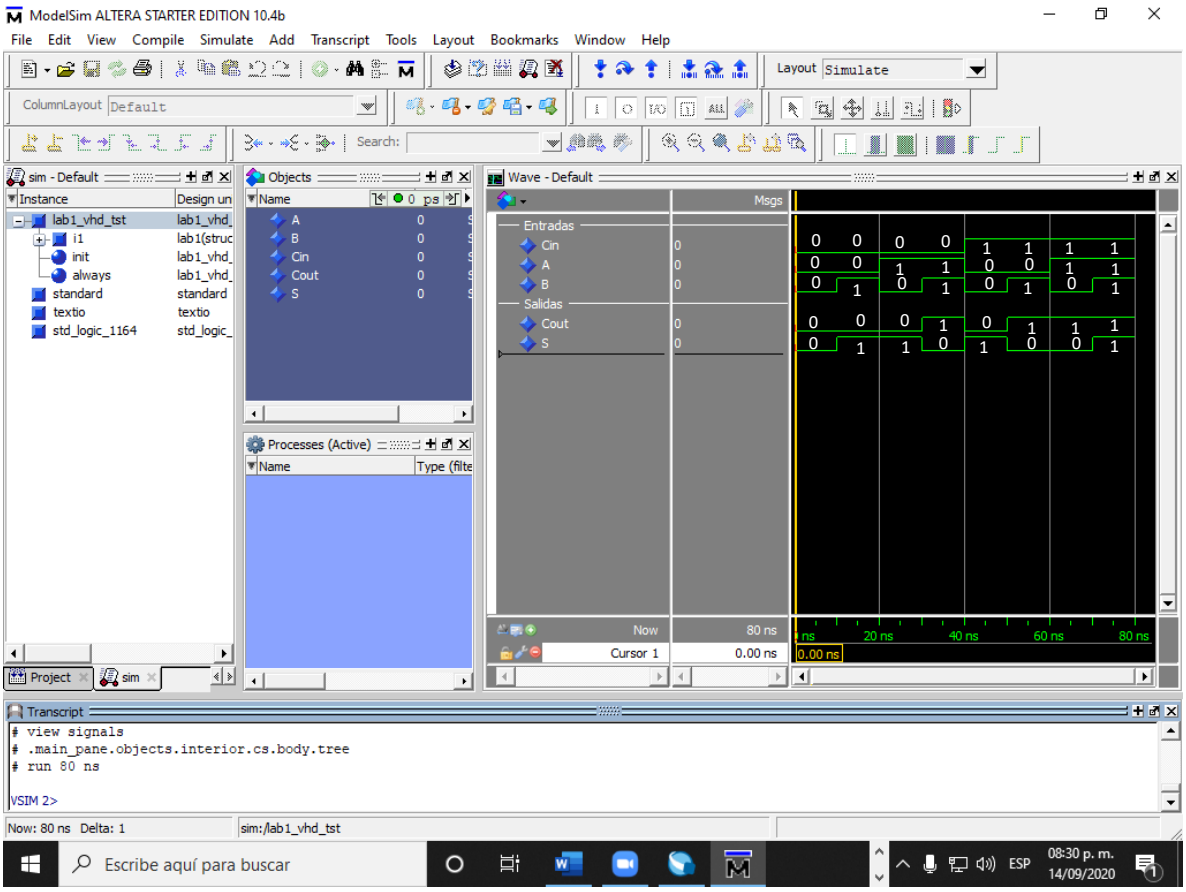
Processors and Peripherals
University Program
Search for Partner IP
Add...
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
TimeQuest Timing Analysis
EDA Netlist Writer
Edit Settings
Type ID Message
286030 Timing-Driven Synthesis is running
16010 Generating hard_block partition "hard_block:auto_generated_inst"
21057 Implemented 7 device resources after synthesis - the final resource count might be different
Quartus Prime Analysis & Synthesis was successful. 0 errors, 0 warnings
Messages
System
Processing (10)
100%
00:00:14
Escribe aquí para buscar
ESP
07:58 p. m.
14/09/2020


RTL Viewer - G:/PUCP/2020-2/Diseño_Digital/Lab/Lab_1/Lab1_20191867/Lab1_20191867 - Lab1_20191867
File Edit View Tools Window Help
Search altera.com
Page: 1 of 1
Netlist Navigator
Lab1_20191867
Lab1_20191867:1
Cin
A
B
W~0
W~1
W
Cout~0
Cout~2
Cout~1
Cout~3
Cout
S~0
S~1
S~2
S
0%
00:00:00
Escribe aquí para buscar
ESP
07:30 p. m.
14/09/2020

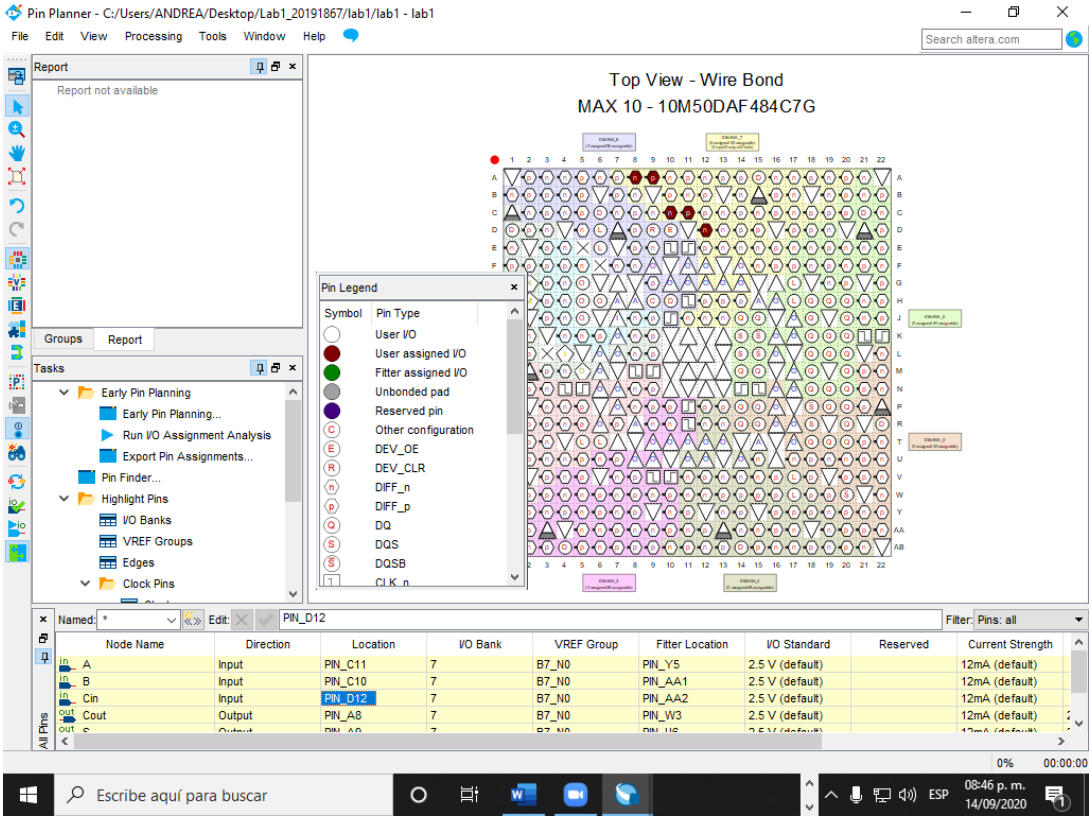
iv.

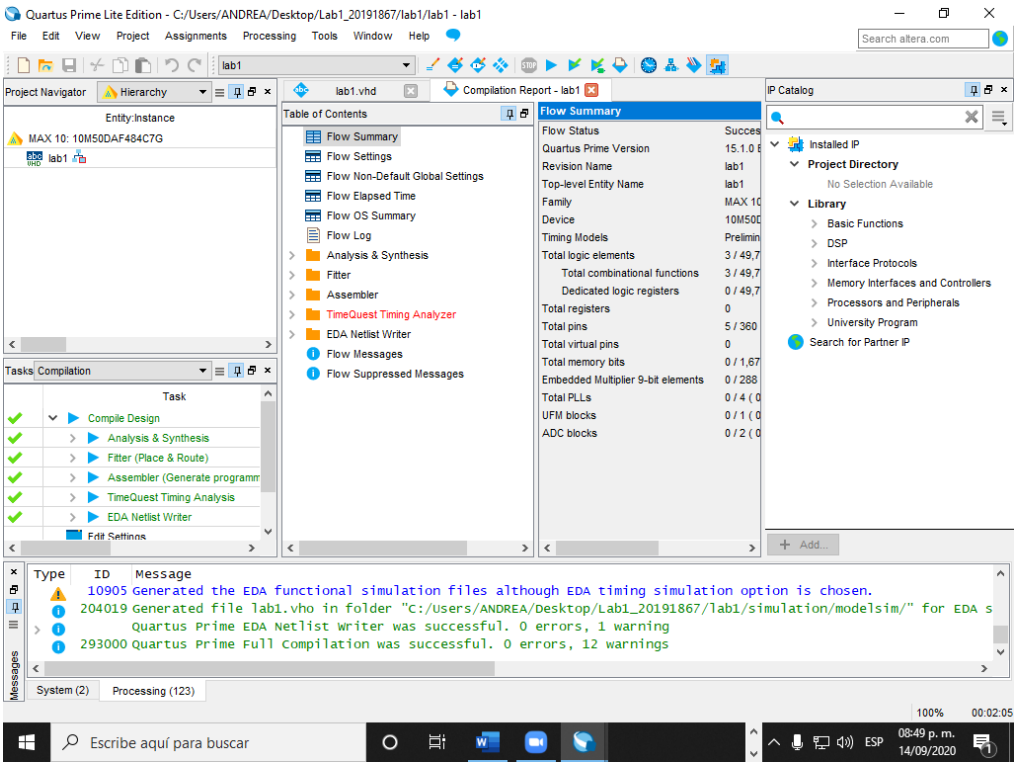


Nro	Entradas			Acarreo	Suma
Fila	Cin	A	B	Cout	S
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	1

La gráfica (Binario/tiempo) muestra en ondas la tabla de verdad.

V.


Pin Planner - C:/Users/ANDREA/Desktop/Lab1_20191867/lab1/lab1 - lab1
File Edit View Processing Tools Window Help
Search altera.com
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Run I/O Assignment Analysis
Export Pin Assignments...
Pin Finder...
Highlight Pins
I/O Banks
VREF Groups
Edges
Clock Pins
Top View - Wire Bond
MAX 10 - 10M50DAF484C7G
Pin Legend
Symbol Pin Type
User I/O
User assigned I/O
Fitter assigned I/O
Unbonded pad
Reserved pin
Other configuration
DEV_OE
DEV_CLR
DIFF_n
DIFF_p
DQ
DQS
DQSB
CLK_n
Named: * Edit: PIN_D12 Filter: Pins: all
Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard Reserved Current Strength
A Input PIN_C11 7 B7_N0 PIN_Y5 2.5 V (default) 12mA (default)
B Input PIN_C10 7 B7_N0 PIN_AA1 2.5 V (default) 12mA (default)
Cin Input PIN_D12 7 B7_N0 PIN_AA2 2.5 V (default) 12mA (default)
Cout Output PIN_A8 7 B7_N0 PIN_W3 2.5 V (default) 12mA (default)
All Pins
0% 00:00:00
Escribe aquí para buscar
ESP 08:46 p. m. 14/09/2020


Quartus Prime Lite Edition - C:/Users/ANDREA/Desktop/Lab1_20191867/lab1/lab1 - lab1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator Hierarchy
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EDA Netlist Writer
Flow Messages
Flow Suppressed Messages
Flow Summary
Flow Status Succes
Quartus Prime Version 15.1.0 E
Revision Name lab1
Top-level Entity Name lab1
Family MAX 10
Device 10M50D
Timing Models Prelimin
Total logic elements 3 / 49,7
Total combinational functions 3 / 49,7
Dedicated logic registers 0 / 49,7
Total registers 0
Total pins 5 / 360
Total virtual pins 0
Total memory bits 0 / 1,67
Embedded Multiplier 9-bit elements 0 / 288
Total PLLs 0 / 4 (0
UFM blocks 0 / 1 (0
ADC blocks 0 / 2 (0
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Add...
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
TimeQuest Timing Analysis
EDA Netlist Writer
Edit Settings
Type ID Message
10905 Generated the EDA functional simulation files although EDA timing simulation option is chosen.
204019 Generated file lab1.vho in folder "C:/Users/ANDREA/Desktop/Lab1_20191867/lab1/simulation/modelsim/" for EDA s
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 12 warnings
Messages
System (2) Processing (123)
100% 00:02:05
Escribe aquí para buscar
ESP 08:49 p. m. 14/09/2020