PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERU

FACULTAD DE ESTUDIOS GENERALES CIENCIAS

Resolución Experiencia 1 y Experiencia 2

SEGUNDO LABORATORIO DISEÑO DIGITAL

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2020-1

Lima, 21 de Septiembre, 2020

Experiencia Práctica Parcial N°1

Describa un circuito de 3 entradas a, b, c y 2 salidas, f, g, cada una de 1 bit, que realice las siguientes funciones:

- f vale ‘1’ cuando las 3 entradas combinadas representan números primos.
- g vale ‘0’ cuando las 3 entradas combinadas, representan múltiplos de 2 (aclaración 0 es múltiplo de 2).

Tabla de Verdad

N	a	b	c	f	g
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	1	0
3	0	1	1	1	1
4	1	0	0	0	0
5	1	0	1	1	1
6	1	1	0	0	0
7	1	1	1	1	1

Mapa de Karnaugh

Con f

a / bc	00	01	11	10
0	0	0	1	1
1	0	1	1	0

$$f = (a + b)(a' + c)$$

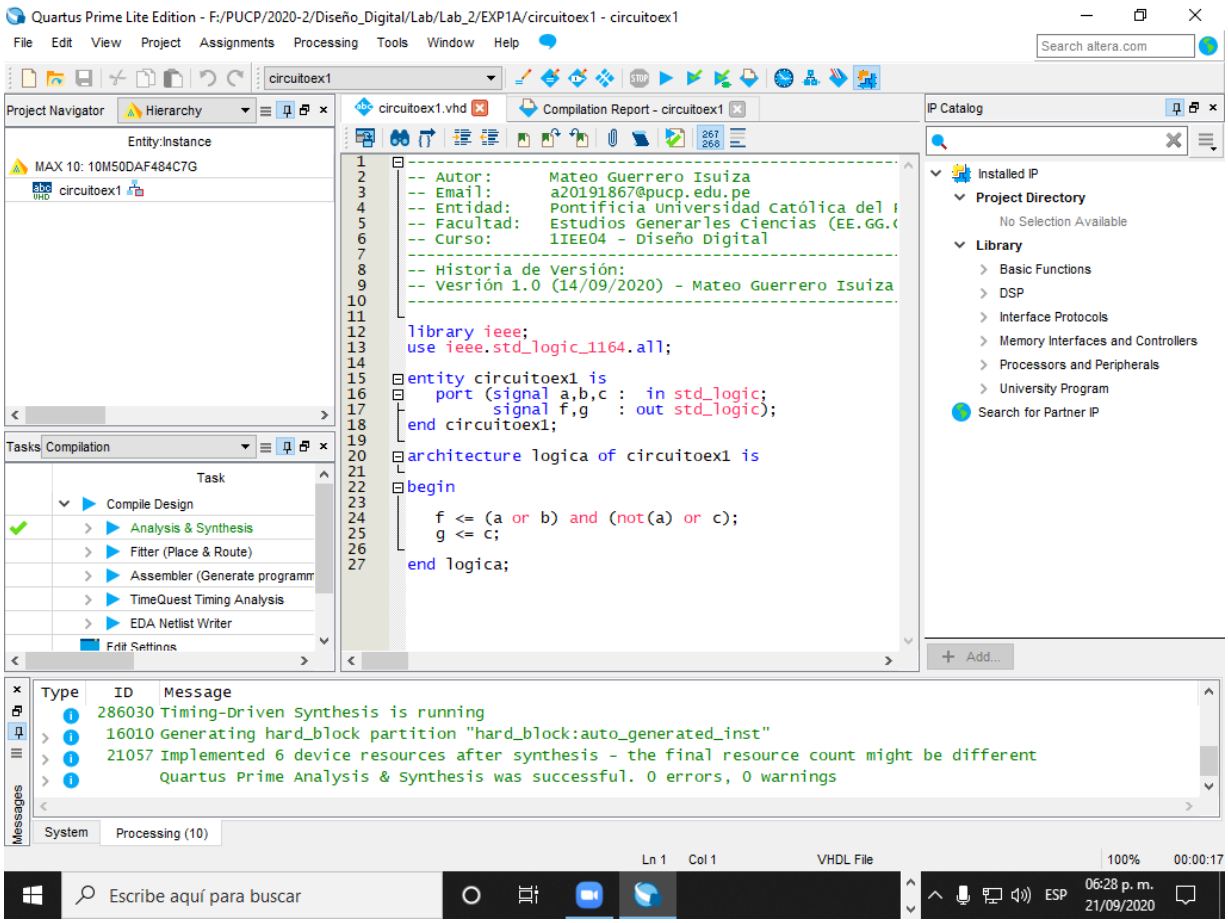
Con g

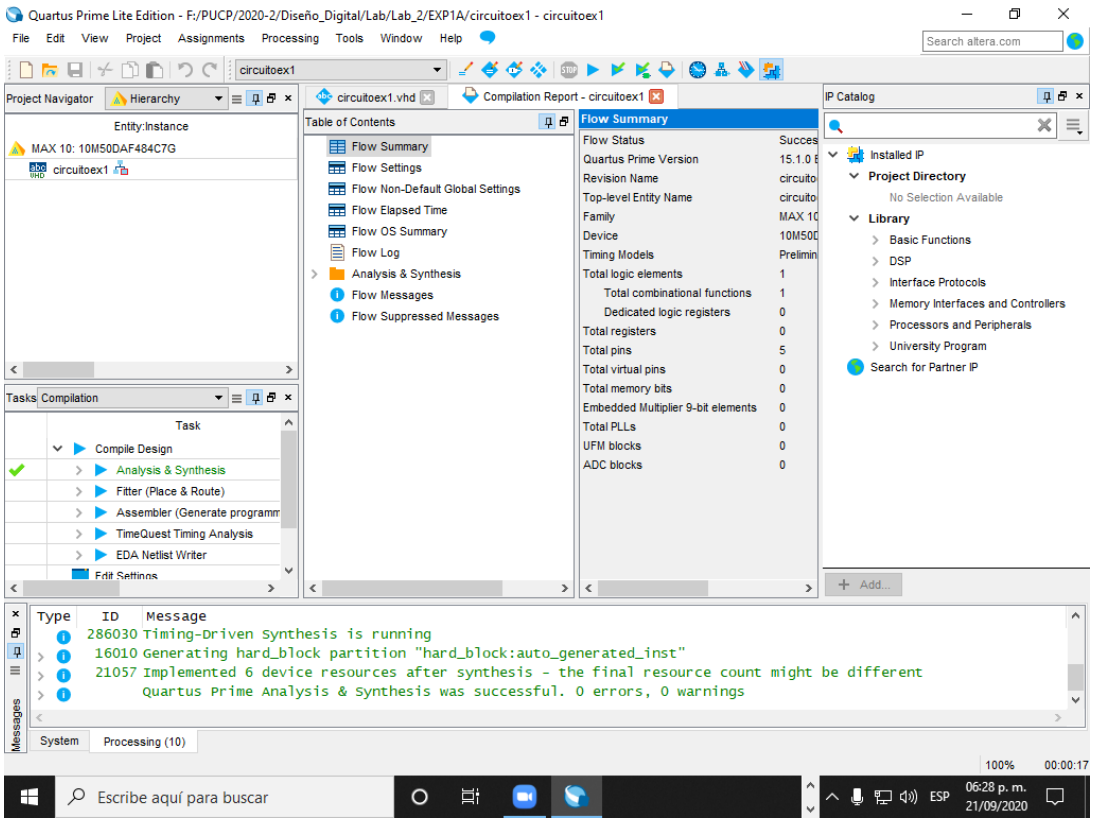
a / bc	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$$g = c$$

Experiencia A

Circuito en VHDL




Quartus Prime Lite Edition - F:/PUCP/2020-2/Diseño_Digital/Lab/Lab_2/EXP1A/circuitoex1 - circuitoex1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator
Hierarchy
Entity:Instance
MAX 10: 10M50DAF484C7G
circuitoex1
circuitoex1.vhd
Compilation Report - circuitoex1
Table of Contents
Flow Summary
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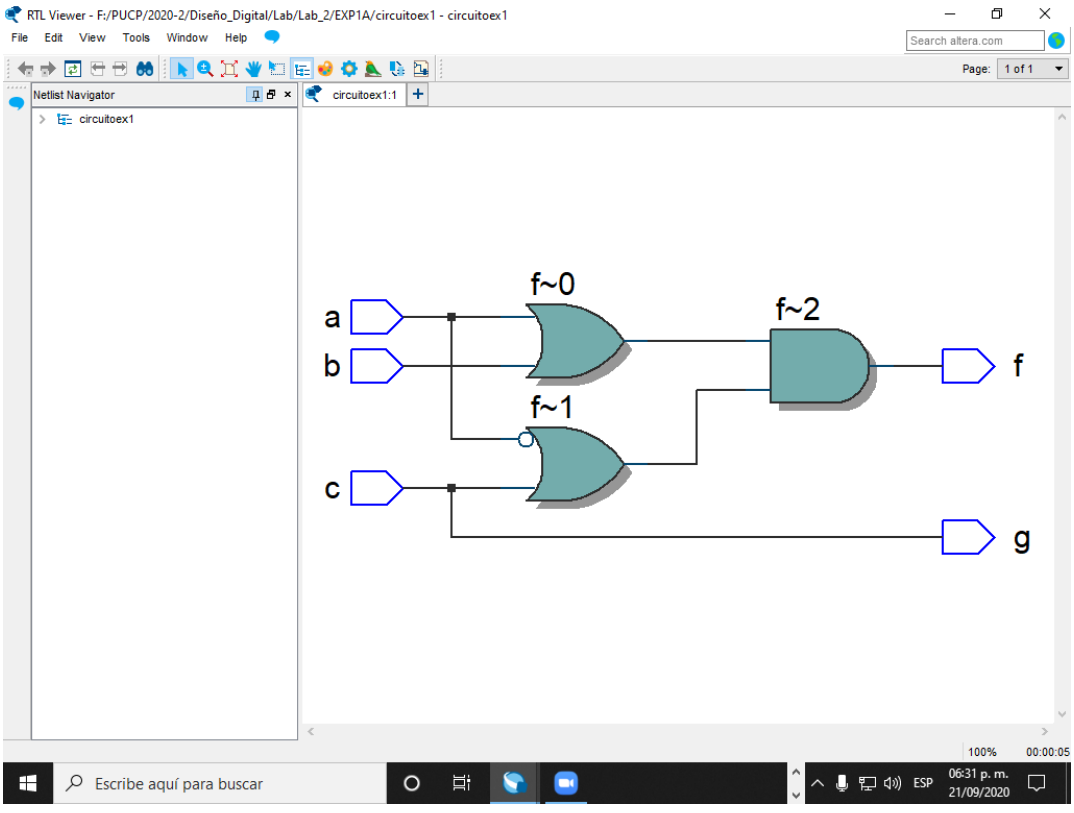
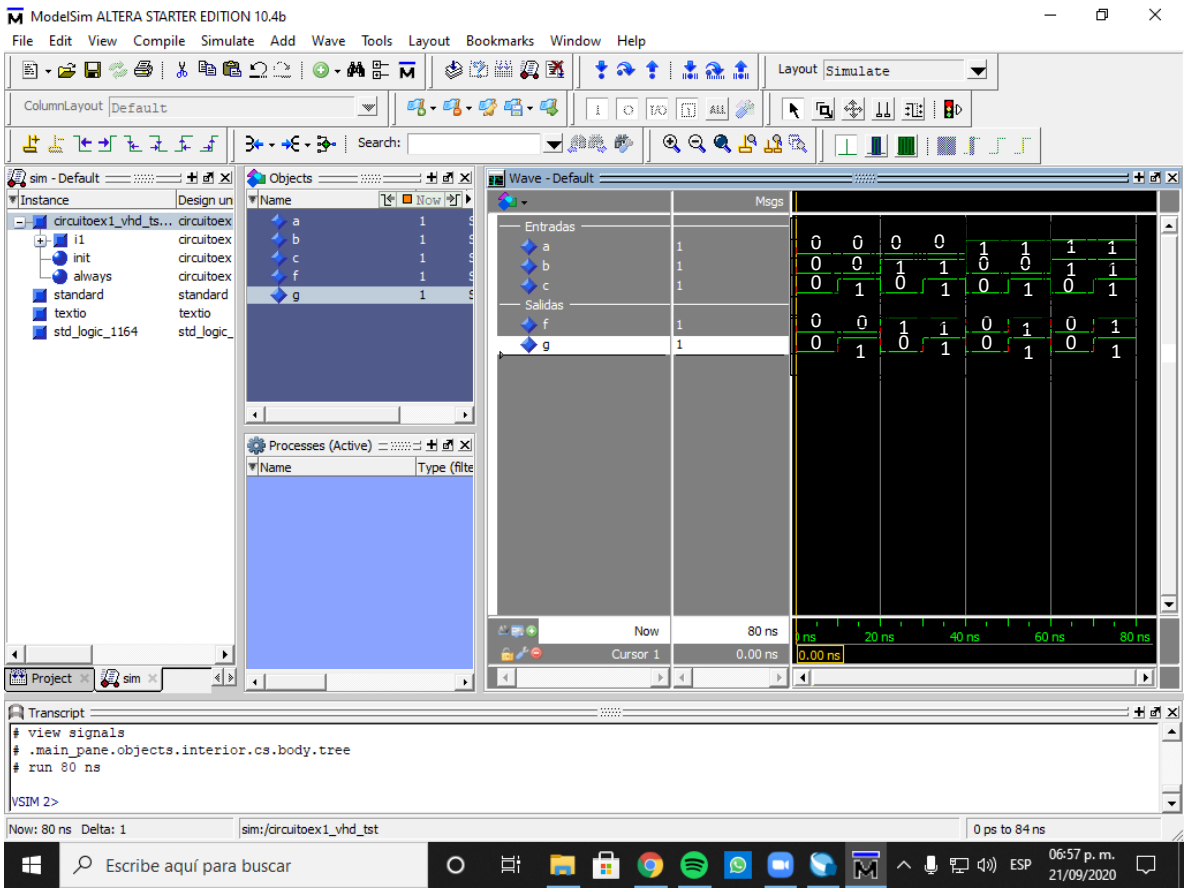
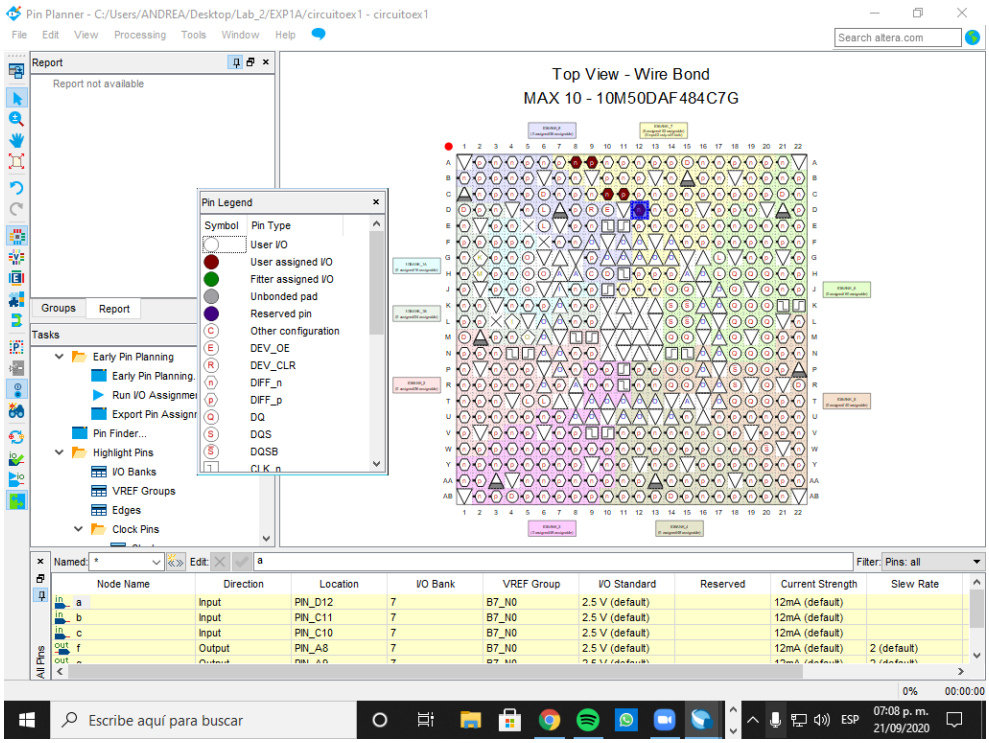
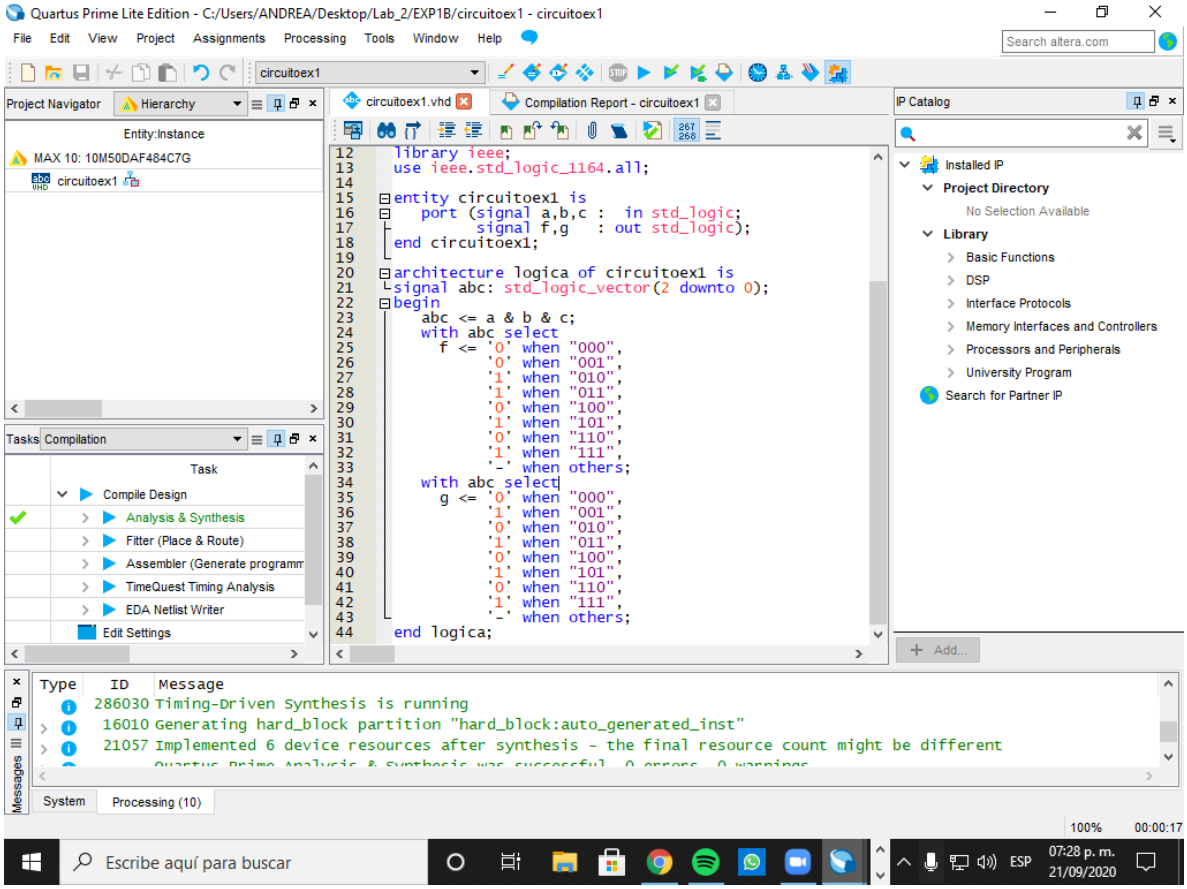
Flow Status
Quartus Prime Version
Revision Name
Top-level Entity Name
Family
Device
Timing Models
Total logic elements
Total combinational functions
Dedicated logic registers
Total registers
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier 9-bit elements
Total PLLs
UFM blocks
ADC blocks
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Add...
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
TimeQuest Timing Analysis
EDA Netlist Writer
Edit Settings
Type ID Message
286030 Timing-Driven Synthesis is running
16010 Generating hard_block partition "hard_block:auto_generated_inst"
21057 Implemented 6 device resources after synthesis - the final resource count might be different
Quartus Prime Analysis & Synthesis was successful. 0 errors, 0 warnings
Messages
System
Processing (10)
100%
00:00:17
Escribe aquí para buscar
ESP
06:28 p. m.
21/09/2020

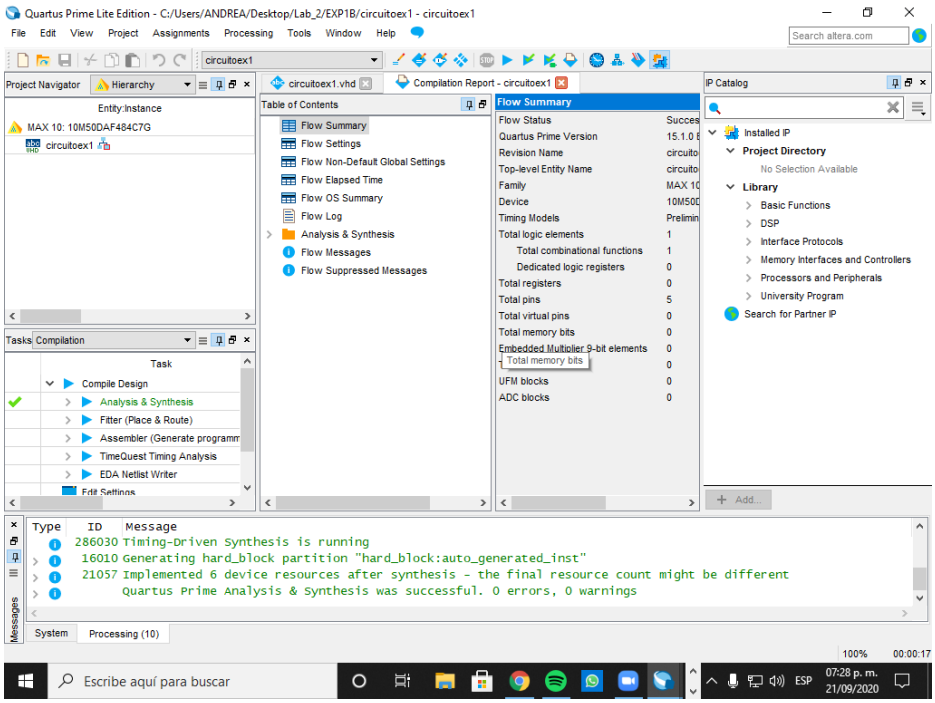

RTL Viewer - F:/PUCP/2020-2/Diseño_Digital/Lab/Lab_2/EXP1A/circuitoex1 - circuitoex1
File Edit View Tools Window Help
Search altera.com
Page: 1 of 1
Netlist Navigator
circuitoex1
circuitoex1:1
a
b
c
f~0
f~1
f~2
f
g
100%
00:00:05
Escribe aquí para buscar
ESP
06:31 p. m.
21/09/2020

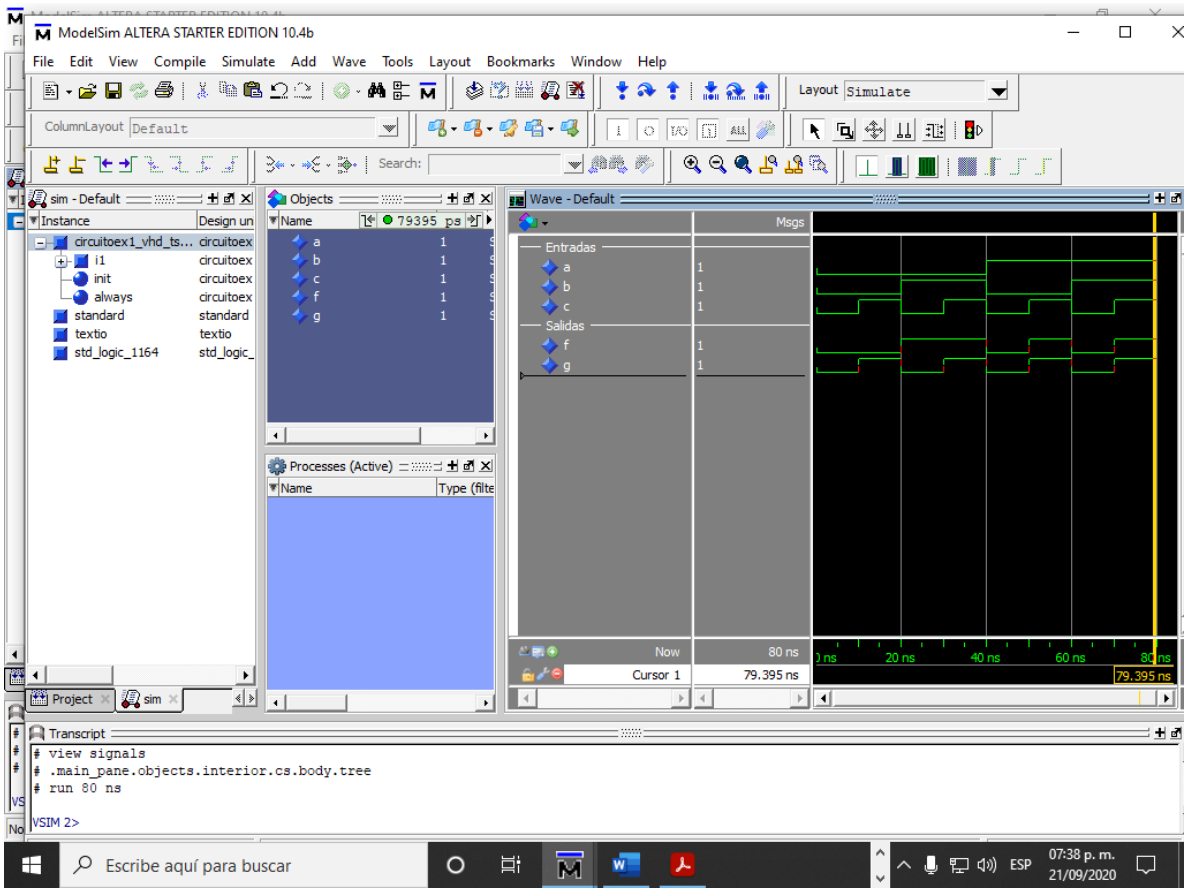

ModelSim ALTERA STARTER EDITION 10.4b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
Processes (Active)
Transcript
view signals
.main_pane.objects.interior.cs.body.tree
run 80 ns
VSIM 2>
Now: 80 ns Delta: 1
sim:/circuitoex1_vhd_tst
Escribe aquí para buscar
06:57 p. m.
21/09/2020


Pin Planner - C:/Users/ANDREA/Desktop/Lab_2/EXP1A/circuitoex1 - circuitoex1
Top View - Wire Bond
MAX 10 - 10M50DAF484C7G
Pin Legend
Report not available
Tasks
Node Name
Direction
Location
I/O Bank
VREF Group
I/O Standard
Reserved
Current Strength
Slew Rate
Escribe aquí para buscar
07:08 p. m.
21/09/2020

Experiencia B






ModelSim ALTERA STARTER EDITION 10.4b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
Design un
circuitoex1_vhd_ts...
circuitoex
i1
init
always
standard
textio
std_logic_1164
Objects
Name
79395 ps
a
b
c
f
g
Processes (Active)
Name
Type (filte
Wave - Default
Msgs
Entradas
Salidas
Now
80 ns
Cursor 1
79.395 ns
20 ns
40 ns
60 ns
Project
sim
Transcript
view signals
.main_pane.objects.interior.cs.body.tree
run 80 ns
VSIM 2>
Escribe aquí para buscar
ESP
07:38 p. m.
21/09/2020

Experiencia Práctica Parcial N°2

N	A	Caracter	g	f	e	d	c	b	a
0	0000	0	1	0	0	0	0	0	0
1	0001	1	1	1	1	1	0	0	1
2	0010	2	0	1	0	0	1	0	0
3	0011	3	0	1	1	0	0	0	0
4	0100	4	0	0	1	1	0	0	1
5	0101	5	0	0	1	0	0	1	0
6	0110	6	0	0	0	0	0	1	0
7	0111	7	1	1	1	1	0	0	0
8	1000	8	0	0	0	0	0	0	0
9	1001	9	0	0	1	1	0	0	0
10	1010	A	0	0	0	1	0	0	0
11	1011	b	0	0	0	0	0	1	1
12	1100	C	1	0	0	0	1	1	0
13	1101	d	0	1	0	0	0	0	1
14	1110	E	0	0	0	0	1	1	0
15	1111	F	0	0	0	1	1	1	0

```
library ieee;

use ieee.std_logic_1164.all;
```

```
entity exp2 is
     port (signal x,y,z,w         : IN std_logic;
                        signal a,b,c,d,e,f,g    : OUT std_logic);
end exp2;

architecture logica of exp2 is

    signal xyzw : std_logic_vector(3 downto 0);

begin

     xyzw <= x & y & z & w;
     with xyzw select
       a <= '0' when "0000",
                        '1' when "0001",
            '0' when "0010",
            '0' when "0011",
                        '1' when "0100",
```

```
                    '0' when "0101",
                    '0' when "0110",
                    '0' when "0111",
                    '0' when "1000",
                    '0' when "1001",
        '0' when "1010",
        '1' when "1011",
                    '0' when "1100",
                    '1' when "1101",
                    '0' when "1110",
                    '0' when "1111",
                    '-' when others;
with xyzw select
  b <= '0' when "0000",
                    '0' when "0001",
        '0' when "0010",
        '0' when "0011",
                    '0' when "0100",
```

```
                    '1' when "0101",
                    '1' when "0110",
                    '0' when "0111",
                    '0' when "1000",
                    '0' when "1001",
        '0' when "1010",
        '1' when "1011",
                    '1' when "1100",
                    '0' when "1101",
                    '1' when "1110",
                    '1' when "1111",
                    '-' when others;
with xyzw select
  c <= '0' when "0000",
                    '0' when "0001",
        '1' when "0010",
        '0' when "0011",
                    '0' when "0100",
```

```
                    '0' when "0101",
                    '0' when "0110",
                    '0' when "0111",
                    '0' when "1000",
                    '0' when "1001",
        '0' when "1010",
        '0' when "1011",
                    '1' when "1100",
                    '0' when "1101",
                    '1' when "1110",
                    '1' when "1111",
                    '-' when others;
with xyzw select
  d <= '0' when "0000",
                    '1' when "0001",
        '0' when "0010",
        '0' when "0011",
                    '1' when "0100",
```

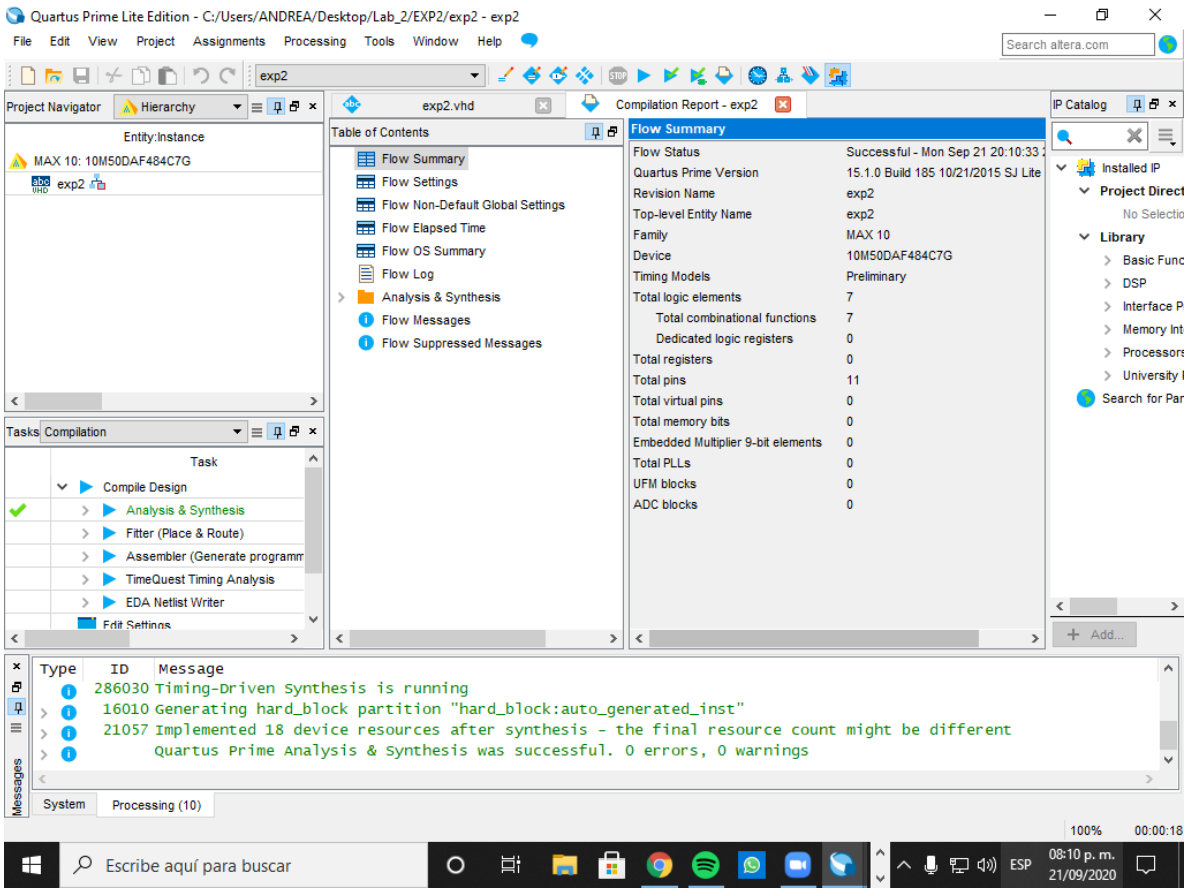
```
                    '0' when "0101",
                    '0' when "0110",
                    '1' when "0111",
                    '0' when "1000",
                    '1' when "1001",
        '1' when "1010",
        '0' when "1011",
                    '0' when "1100",
                    '0' when "1101",
                    '0' when "1110",
                    '1' when "1111",
                    '-' when others;
with xyzw select
  e <= '0' when "0000",
                    '1' when "0001",
        '0' when "0010",
        '1' when "0011",
                    '1' when "0100",
```

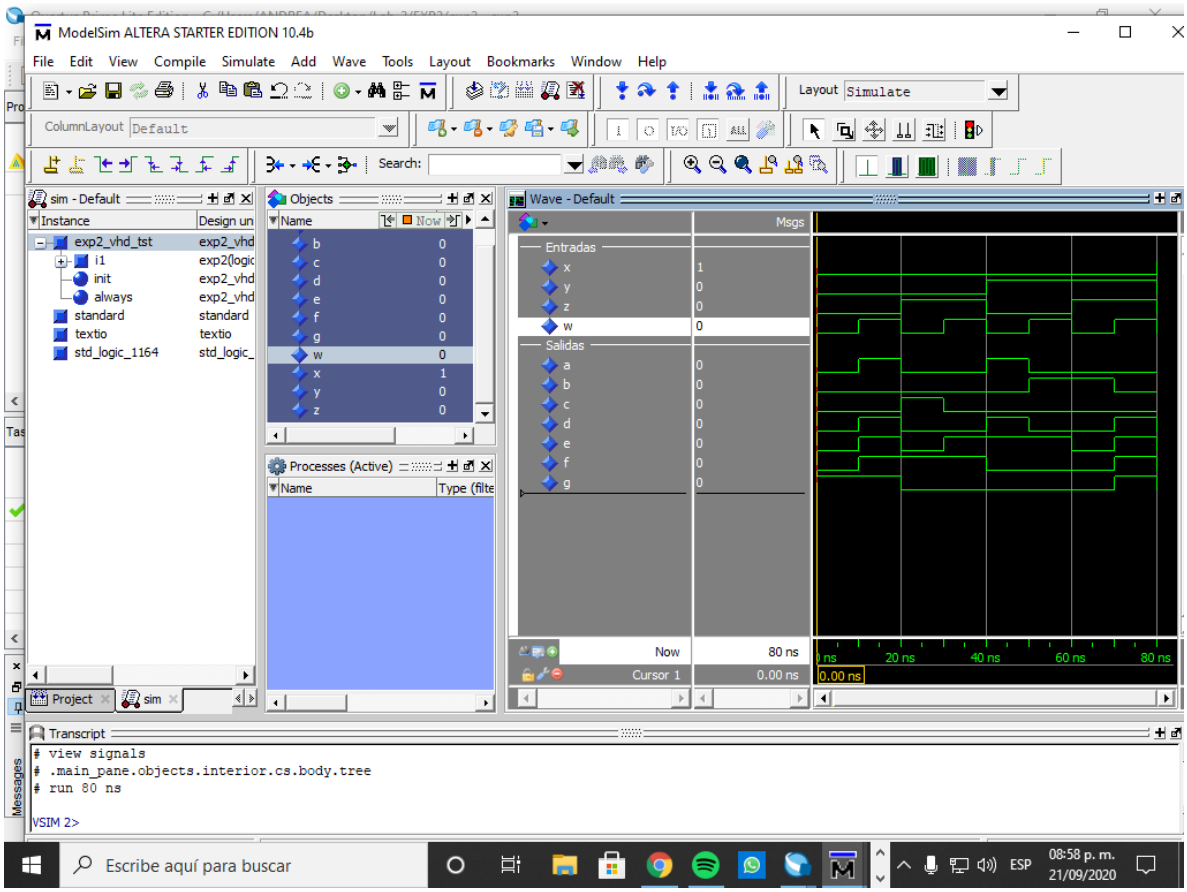
```
                '1' when "0101",
                '0' when "0110",
                '1' when "0111",
                '0' when "1000",
                '1' when "1001",
        '0' when "1010",
        '0' when "1011",
                '0' when "1100",
                '0' when "1101",
                '0' when "1110",
                '0' when "1111",
                '-' when others;
with xyzw select
  f <= '0' when "0000",
                '1' when "0001",
        '1' when "0010",
        '1' when "0011",
                '0' when "0100",
```

```
                    '0' when "0101",
                    '0' when "0110",
                    '1' when "0111",
                    '0' when "1000",
                    '0' when "1001",
        '0' when "1010",
        '0' when "1011",
                    '0' when "1100",
                    '1' when "1101",
                    '0' when "1110",
                    '0' when "1111",
                    '-' when others;
with xyzw select
  g <= '1' when "0000",
                    '1' when "0001",
        '0' when "0010",
        '0' when "0011",
                    '0' when "0100",
```

```
                '0' when "0101",
                '0' when "0110",
                '1' when "0111",
                '0' when "1000",
                '0' when "1001",
'0' when "1010",
'0' when "1011",
                '1' when "1100",
                '0' when "1101",
                '0' when "1110",
                '0' when "1111",
                '-' when others;
```

end logica;


Quartus Prime Lite Edition - C:/Users/ANDREA/Desktop/Lab_2/EXP2/exp2 - exp2
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
exp2
Project Navigator
Hierarchy
Entity:Instance
MAX 10: 10M50DAF484C7G
exp2
exp2.vhd
Compilation Report - exp2
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Flow Messages
Flow Suppressed Messages
Flow Summary
Flow Status Successful - Mon Sep 21 20:10:33
Quartus Prime Version 15.1.0 Build 185 10/21/2015 SJ Lite
Revision Name exp2
Top-level Entity Name exp2
Family MAX 10
Device 10M50DAF484C7G
Timing Models Preliminary
Total logic elements 7
Total combinational functions 7
Dedicated logic registers 0
Total registers 0
Total pins 11
Total virtual pins 0
Total memory bits 0
Embedded Multiplier 9-bit elements 0
Total PLLs 0
UFM blocks 0
ADC blocks 0
IP Catalog
Installed IP
Project Direct
No Selectio
Library
Basic Func
DSP
Interface P
Memory Int
Processors
University
Search for Par
Add...
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
TimeQuest Timing Analysis
EDA Netlist Writer
Edit Settings
Type ID Message
286030 Timing-Driven Synthesis is running
16010 Generating hard_block partition "hard_block:auto_generated_inst"
21057 Implemented 18 device resources after synthesis - the final resource count might be different
Quartus Prime Analysis & Synthesis was successful. 0 errors, 0 warnings
Messages
System
Processing (10)
100%
00:00:18
Escribe aquí para buscar
ESP
08:10 p. m.
21/09/2020


ModelSim ALTERA STARTER EDITION 10.4b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
exp2_vhd_tst
i1
init
always
standard
textio
std_logic_1164
Objects
Name
b
c
d
e
f
g
w
x
y
z
Processes (Active)
Name
Type
Wave - Default
Msgs
Entradas
Salidas
Now
80 ns
Cursor 1
0.00 ns
20 ns
40 ns
60 ns
Project
sim
Transcript
view signals
.main_pane.objects.interior.cs.body.tree
run 80 ns
VSIM 2>
Messages
Escribe aquí para buscar
ESP
08:58 p. m.
21/09/2020