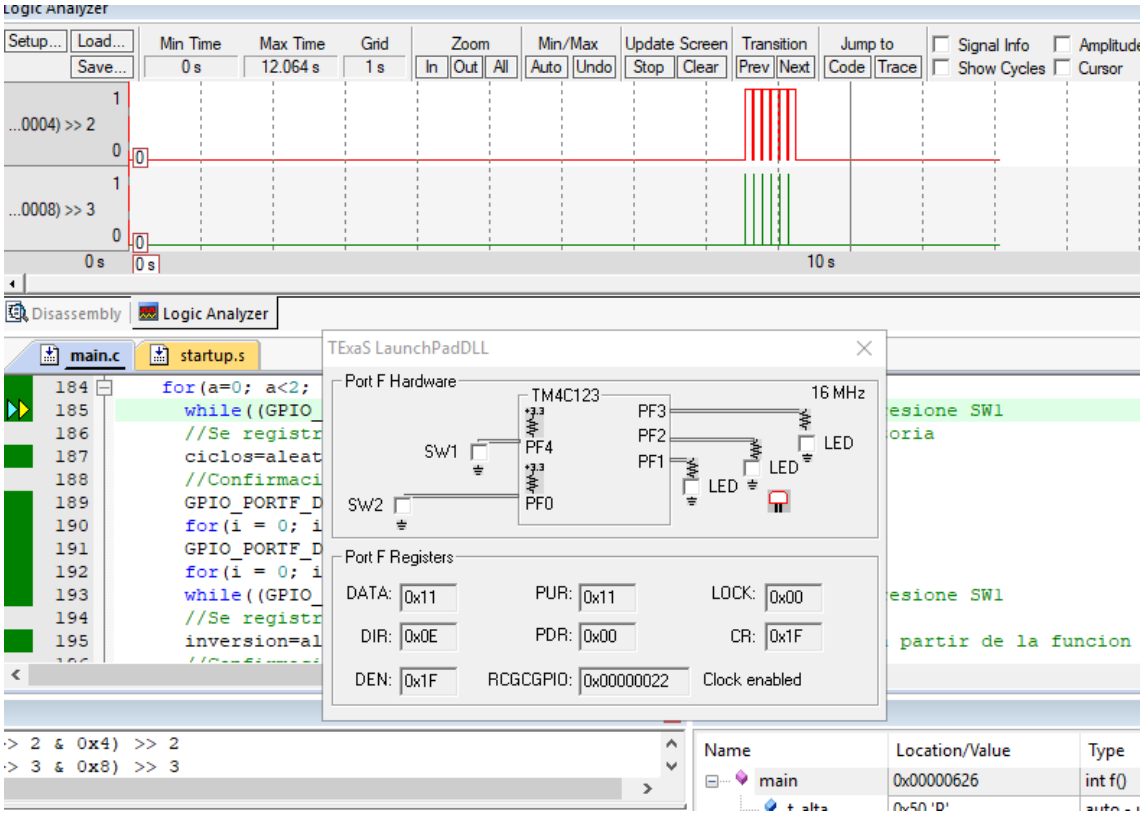
Logic Analyzer
Setup...
Load...
Save...
Min Time
0 s
Max Time
12.064 s
Grid
1 s
Zoom
In
Out
All
Min/Max
Auto
Undo
Update Screen
Stop
Clear
Transition
Prev
Next
Jump to
Code
Trace
Signal Info
Show Cycles
Amplitude
Cursor
...0004) >> 2
...0008) >> 3
0 s
10 s
Disassembly
Logic Analyzer
main.c
startup.s
TExaS LaunchPadDLL
Port F Hardware
TM4C123
16 MHz
SW1
SW2
PF4
PF0
PF3
PF2
PF1
LED
LED
LED
Port F Registers
DATA: 0x11
PUR: 0x11
LOCK: 0x00
DIR: 0x0E
PDR: 0x00
CR: 0x1F
DEN: 0x1F
RCGCGPIO: 0x00000022
Clock enabled
for(a=0; a<2;
while((GPIO_
//Se registr
ciclos=aleat
//Confirmaci
GPIO_PORTF_D
for(i = 0; i
GPIO_PORTF_D
for(i = 0; i
while((GPIO_
//Se registr
inversion=al
esione SW1
oria
esione SW1
partir de la funcion
> 2 & 0x4) >> 2
> 3 & 0x8) >> 3
Name
Location/Value
Type
main
0x00000626
int f()