The course **Analog and mixed-signal integrated circuits** follows the textbook 'Analog Design Essentials' (author Willy M. C. Sansen, Springer, 2006)
Academic year 2011/2012

1. block:
    - Chapter 1: sl. 01.1 – 01.32, 01.36, 01.39, 01.43 – 01.45, 01.58 – 01.63, 01.66 – 01.72 (no circuits with bipolar transistors)
    - Chapter 2: sl. 02.1 – 02.55 (only have a look at 02.56 – 02.57), 02.58 – 02.63 (only have a look at 02.64 – 02.65), 02.66 – 02.67 (no circuits with bipolar transistors)
    - Chapter 3: sl. 03.1 – 03.7 (only have a look at 03.8 – 03.10), 03.14 – 03.41 (no circuits with bipolar transistors)
    - Chapter 5: sl. 05.1 – 05.46

Typical questions:

Chapter 1:

1. Draw technology cross-sections of an NMOS and a PMOS transistor processed on the p-type Si substrate (also draw substrate contacts for both transistors).
2. Write down the definitions of the deplation C_D and oxide C_{ox} capacitance per unit area of a MOS transistor. Which one is larger and why?
3. Write down the expression for the drain current of an NMOS transistor in saturation as a function of W, L and λ. What is the dependence of λ on the channel length L? Draw a small-signal equivalent circuit of a MOS transistor at low frequencies (sl. 01.22 - 01.25)
4. What is f_T and how to calculate it (sl. 01.61)? What is the value of the output voltage when f_T is calculated and why?
5. Draw an RF small-signal equivalent circuit of a MOS transistor (sl. 01.68 and 01.69).

Chapter 2:

1. Draw a simple one-stage amplifier having an NMOS transistor and a current source I_B connected to the drain. Assume that the output dynamic resistance of the current source r_{IB} is much larger than the output resistance of the NMOS transistor r_d. Draw a small-signal equivalent circuit and calculate the gain A_V (sl. 2.4).
2. Draw a diode-connected NMOS transistor and derive the expression for the output dynamic resistance between the drain and source contacts (sl. 2.17 i 2.18).
3. Derive the expression for the voltage gain of the circuit on sl. 2.20.
4. Derive the expression for the voltage gain of the circuit on sl. 2.21.
5. Izvesti izraz za naponsko pojačanje sklopova na sl. 2.22.
6. Calculate the gain A_{V0}, bandwidth BW and GBW of the circuit in Fig. 1. Assume that the output dynamic resistance r_{IDC} of the current source I_{DC} is equal to the output resistance r_d of the NMOS transistor T_1. Draw a Bode diagram (amplitude and phase).

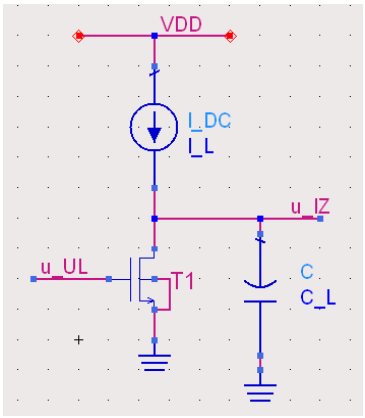
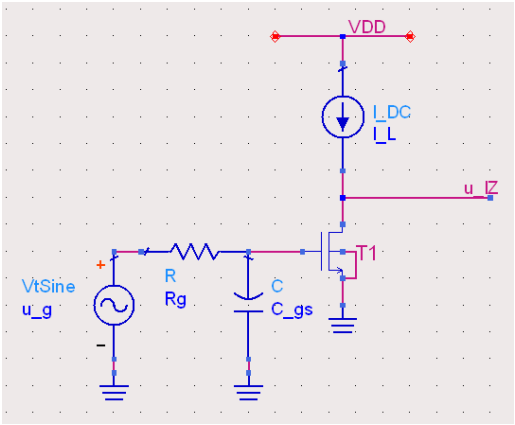


Figure 1 Simple amplifier with capacitive load.

7. Calculate the gain A_{V0}, bandwidth BW and GBW of the circuit in Fig. 2. Assume that the output dynamic resistance r_{IDC} of the current source I_{DC} is equal to the output resistance r_d of the NMOS transistor T_1. Draw a Bode diagram (amplitude and phase).



Slika 2 Simple amplifier.

8. Calculate the gain A_{V0}, bandwidth BW and GBW of the circuit in sl. 02.11. Assume that the output dynamic resistance r_{IL} of the current source I_L is equal to the output resistance r_d of the NMOS transistor.
9. Calculate the gain A_{V0}, bandwidth BW and GBW of the circuit in sl. 02.13. Assume that the output dynamic resistance r_{IL} of the current source I_L is much larger than the output resistance r_d of the NMOS transistor. When you mirror the capacitance C_F to the output, use the full expression for the mirrored capacitance to obtain the value of the positive zero.
10. When an NMOS/PMOS complementary pair of transistors works as an amplifier, how do you ensure the same currents of transistors and how do you ensure the same output resistance (sl. 02.27 i 02.29)?
11. For both circuits in sl. 02.53 calculate the voltage gain A_{V0}, bandwidth BW and GBW if the output is loaded by C_L. Assume that the output dynamic resistance r_{IB} of the current source I_B is equal to the output resistance r_d of the NMOS transistor M_1 for the left circuit and equal to the output resistance of the cascode for the right circuit. Draw the small-signal equivalent circuit.

12. Draw the circuit of a telescopic cascode. What is the gain A_{V0}, bandwidth BW and GBW of this circuit if the output is loaded by C_L?
13. Draw the circuit of a folded cascode. What is the gain A_{V0}, bandwidth BW and GBW of this circuit if the output is loaded by C_L? Write down the assumptions used in the calculation.

Chapter 3:

1. Draw a simple current mirror circuit: a) using NMOS transistors; b) using PMOS transistors.
2. Draw a cascode version of the current mirror using NMOS transistors. What is the expected minimum output voltage if V_T = 0,5 V?
3. Draw an improved version of the cascode current mirror using NMOS transistors which allows the operation under a reduced supply voltage VDD.
4. Draw a basic scheme of a voltage differential amplifier by using NMOS (PMOS) transistors in the input differential stage. What is the main difference between the NMOS and PMOS input differential stage when the p-substrate CMOS technology is used (hint: check the potential of the sources of the transistors in the differential pair).
5. Draw a basic scheme of a differential amplifier by using PMOS transistors in the input differential stage and current mirror as an active load. Calculate the gain A_{V0}, bandwidth BW and GBW of the circuit if the output is loaded by C_L.

Chapter 5:

1. Draw a schematic of an amplifier with feedback and diagram(s) that show the open loop gain and closed loop gain. What is the loop gain. Which of these 'gains' is used to define the phase margin?
2. Which phase margin we have to achieve in the design of a two-stage operational amplifier to get the characteristics without peaking in the frequency domain and without ringing in the time domain? What is the design rule for GBW of the two stage opamp and what is the design rule for the non-dominant pole? How do we choose the compensation capacitance C_c? What is the position of the non-dominant pole to ensure necessary phase margin?
3. Which element introduces a positive zero in the transfer characteristic A_V of the two-stage opamp? How the positive zero is reflected in the Bode plot? Which circuits can be used to abolish the influence of the positive zero?
4. For the given GBW = 50 MHz and C_L = 4 pF, calculate the compensation capacitance C_c, g_{m1} and g_{m2} to ensure stable operation. Calculate I_{D1} and I_{D2}. Calculate the usual figure of merit FOM = $(GBW \cdot C_L)/I_{tot}$ where GBW is given in MHz, C_L in pF and I_{tot} in mA.

Physical parameters and constants:

$\varepsilon_0 = 8{,}854 \cdot 10^{-14}$ F/cm
$\varepsilon'_{Si} = 11{,}7$
$\varepsilon'_{ox} = 3{,}9$
$\varepsilon_{Si} = 1{,}036$ pF/cm
$\varepsilon_{ox} = 0{,}345$ pf/cm
$v_{sat} = 10^7$ cm/s

Typical parameters of a 0,35 um CMOS technology:

$t_{ox} = 7$ nm
$L_{min} = 0{,}35$ µm

nMOS

$U_{GS0n} = 0{,}55$ V
$K_n = 100$ µA/V2
$1/\lambda = v_{En} \cdot L$
$v_{En} = 4$ V/µm

pMOS

$U_{GS0p} = -0{,}55$ V
$K_p = -40$ µA/V2
$1/\lambda = v_{Ep} \cdot L$
$v_{Ep} = 8$ V/µm

$C_{ox} = \varepsilon_{ox}/t_{ox} = 4{,}93$ fF/µm^2 (for $t_{ox} = 7$ nm)
$g_{m,sat} = WC_{ox}\, v_{sat}$

$I_D = K_n(W/L) \cdot (U_{GS} - U_{GS0})^2 (1 + \lambda \cdot U_{DS})$
$C_{gs} = (2/3) WLC_{ox}$
$f_T = \mathrm{gm}/(2\pi\, C_{gs})$