The course **Analog and mixed-signal integrated circuits** follows the textbook 'Analog Design Essentials' (author Willy M. C. Sansen, Springer, 2006)
Academic year 2011/2012

2. block:
    - Chapter 5: sl. 05.47 – 05.59
    - Chapter 6: sl. 06.1 – 06.47 (no bipolars, no noise analysis)
    - Chapter 7: sl. 07.1 – 07.32 (no bipolars)
    - Chapter 8: sl. 08.1 – 08.14 (no bipolars)
    - Chapter 15: sl. 15.1 – 15.55 (no bipolars)

Typical questions:

Chapter 5:

1. For a 3-stage amplifier, explain how to choose the compensation capacitances C_c and C_D (related to the load capacitance C_L and non-dominant pole frequencies). Find I_{DS1}, I_{DS2}, I_{DS3}, C_c and C_D to obtain GBW = 40 MHz for C_L = 2 pF. Calculate the total current consumption.

Chapter 6:

1. Draw the schematic of a 2-stage Miller OTA that has PMOS transistors in the differential input stage. Draw the small-signal equivalent circuit. Calculate the voltage gain of the first and second stage A_{V1} and A_{V2}, bandwidth BW and GBW if the output is loaded by C_L = 2 pF and GBW = 10 MHz. Estimate the parasitic capacitance C_{n1} at the input of the second stage (for a rough estimate assume that for a transistor $C_{gs} = C_{gd} = C_{db}$).
2. How do you calculate the slew rate SR of a 2-stage Miller OTA when the slew rate depends on the internal activity of the amplifier? Calculate SR/GBW.
3. How do you calculate the slew rate SR of a 2-stage Miller OTA when the slew rate depends on the external capacitive load C_L?

Chapter 7:

1. Draw the schematic of a single-stage CMOS OTA. Write down the expression for the dominant pole and the expression for the non-dominant pole. The capacitance that defines the non-dominant pole is the sum of which parasitic capacitances?
2. Draw the schematic of a single-stage telescopic CMOS OTA. Does the use of the cascodes change the GBW of the amplifier? Does the use of the cascodes change the current consumption of the amplifier? How many bias voltages we have to define additionally to the power supply voltages VDD and VSS?
3. Draw the schematic of a single-stage symmetrical CMOS OTA (the simplest possible circuit) loaded by C_L. Calculate the voltage gain A_{V0}, bandwidth BW and GBW. Which capacitance defines the frequency of the non-dominant pole? What is the frequency of the non-dominant pole? What is the largest possible value of the current factor B? Which voltage ($V_{GS} - V_T$) should be chosen for the transistors in the current mirror $1:B$?
4. Draw the schematic of a single-stage symmetrical CMOS OTA with the cascodes.
5. Draw the schematic of a symmetrical Miller CMOS OTA (2-stage amplifier) in a configuration that allows suppression of the positive zero.

6. Draw the schematic of a folded cascode CMOS OTA loaded by C_L. What is the gain, bandwidth and *GBW* of this amplifier? What is the frequency of the non-dominant pole?
7. What are the advantages of the folded cascode CMOS OTA (sl. 07.27, 07.29, 07.30)? What is the drawback of this circuit (sl. 07.25)?

Chapter 8:

1. Draw the schematic of a simple fully differential CMOS OTA with a CMFB amplifier.

Chapter 15:

1. Calculate the mismatch of a simple differential pair caused by the spreading of the load resistance ΔR_L.
2. What is the relative spreading of the output current of the current mirror?
3. What is the CMRR (common-mode rejection ratio)? Derive the expression for the CMRR for a simple differential pair. (sl. 15.18)

Physical parameters and constants:

$\varepsilon_0 = 8{,}854 \cdot 10^{-14}$ F/cm
$\varepsilon'_{Si} = 11{,}7$
$\varepsilon'_{ox} = 3{,}9$
$\varepsilon_{Si} = 1{,}036$ pF/cm
$\varepsilon_{ox} = 0{,}345$ pf/cm
$v_{sat} = 10^7$ cm/s

Typical parameters of a 0,35 um CMOS technology:

$t_{ox} = 7$ nm
$L_{min} = 0{,}35$ µm

nMOS

$U_{GS0n} = 0{,}55$ V
$K_n = 100$ µA/V2
$1/\lambda = v_{En} \cdot L$
$v_{En} = 4$ V/µm

pMOS

$U_{GS0p} = -0{,}55$ V
$K_p = -40$ µA/V2
$1/\lambda = v_{Ep} \cdot L$
$v_{Ep} = 8$ V/µm

$$I_D = K_{n,p} \frac{W}{L} \cdot (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 4{,}93\ \mathrm{fF/\mu m^2}$ for t_{ox} = 7 nm, i.e. L_{min} = 0,35 µm

$g_{m,sat} = WC_{ox}v_{sat}$

$$C_{gs} = \frac{2}{3}WLC_{ox}$$

$$f_T = \frac{g_m}{2\pi C_{gs}}$$

$f_T = \frac{1}{L} \cdot \frac{1{,}35}{1+2{,}8 \cdot 10^4 \frac{L}{V_{GS}-V_T}}$ where L is in 'cm' and f_T in 'MHz'