Course: Analog and mixed-signal integrated circuits
Midterm exam, 01.12.2011.

1. Draw a technology cross-section of a PMOS transistor processed on the p-type Si substrate (also draw the substrate contact).
   (2 points)

2. Draw and design a simple one-stage amplifier with an NMOS transistor under the following conditions:
   a. Set the drain current to $I_D = 20\ \mu A$ and the dynamic output resistance to be 200 kΩ. Knowing that the amplifier is not designed for RF (radio frequency) applications, choose suitable V_{GS} and calculate W and L (if you need the voltage V_{DS}, you may assume that V_{DS} is at the boundary between the triode and saturation region).
   b. Calculate the transconductance g_m and the low-frequency voltage gain A_V assuming that an active load is connected at the drain of the NMOS transistor and that its dynamic output resistance is equal to the dynamic output resistance r_{dN} of the NMOS transistor (draw the small-signal dynamic equivalent circuit before calculating the gain).
   (7 points)

3. Draw a diode-connected NMOS transistor and derive the expression for the output dynamic resistance between the drain and source contacts (draw the small-signal dynamic equivalent circuit before the calculation).
   (2 points)

4. Calculate the low-frequency voltage gain $A_{V0} = u_{iz}/u_{ul}$ for a circuit in Fig. 1 under the assumption that for typical transistor dimensions the dynamic output resistance $r_d >> 1/g_m$ (draw the small-signal dynamic equivalent circuit before the calculation). Express the voltage gain using the transistor parameters (W, L, V_{GS0}, ...). Which condition has to be met for the transistor *T1* to be in the saturation, and under which condition *T2* is in saturation?
   (4 points)

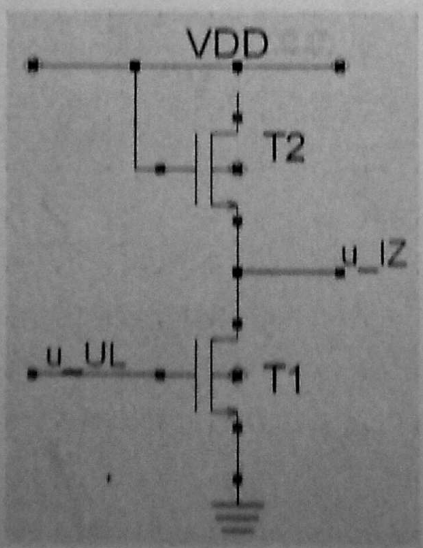

Figure 1. NMOS amplifier.

5. Calculate the low-frequency voltage gain $A_{V0} = u_{iz}/u_{ul}$ for a circuit in Fig. 2, bandwidth BW and GBW (draw the small-signal equivalent circuit). Assume that the output dynamic resistance r_{IDC} of the current source I_{DC} is equal to the output resistance r_d of the NMOS transistor T_1. Draw the amplitude and phase Bode diagram. If the output u_{iz} is loaded by C_L, under which conditions the characteristic pole frequency of C_{gs} will be equal to the pole introduced by C_L?
(8 points)

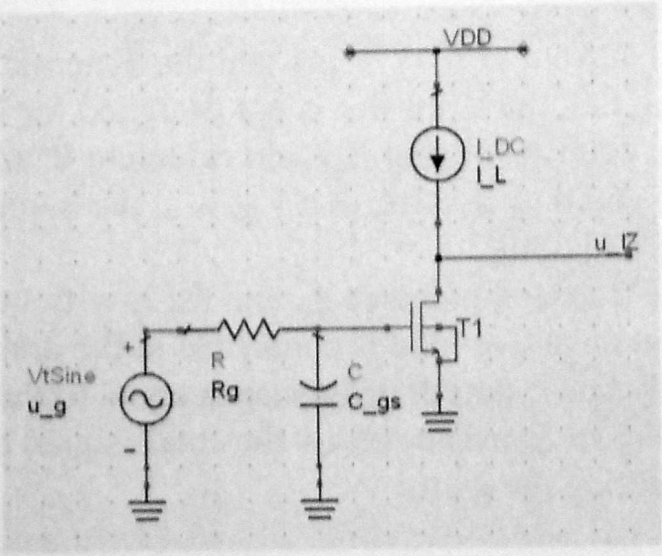

Figure 2. Amplifier (C_{gs} is a part of the transistor).

6. Draw a basic schematic of a differential amplifier by using PMOS transistors in the input differential stage and a current mirror as an active load. Calculate the gain A_{V0}, bandwidth BW and GBW of the circuit if the output is loaded by C_L?
(4 points)

7. For a given $GBW = 75$ MHz and $C_L = 5$ pF, calculate the compensation capacitance C_c and the transconductance of the input transistors g_{m1} and of the output transistor in the second stage g_{m2} to ensure stable operation. What is the phase margin for a stable operation of a two-stage operational amplifier and how it is ensured? Calculate I_{D1} and I_{D2}. Calculate the figure of merit FOM = $(GBW \cdot C_L)/I_{tot}$. Estimate the capacitance C_{gs} of the output transistor T_2.
(8 points)

Course: Analog and mixed-signal integrated circuits
Final exam, 26.01.2012.

1. Draw the schematic of a 2-stage Miller OTA that has PMOS transistors in the differential input stage. Draw the small-signal equivalent circuit. Calculate the low-frequency voltage gain of the first and second stage A_{V01} and A_{V02}, bandwidth BW and GBW. If the output is loaded by $C_L = 2$ pF and $GBW = 25$ MHz, determine f_{nd}, C_c, g_{m1}, g_{m6} (the transconductance of the output stage). Estimate the parasitic capacitance C_{n1} at the input of the second stage; it is not necessary to determine the numerical value of this parasitic capacitance (for a rough estimate assume that for a transistor $C_{gs} = C_{gd} = C_{db}$).
   (8 points)

2. Derive the expression of the ratio SR/GBW of a 2-stage Miller OTA when the slew rate depends on the internal activity of the amplifier. Which $V_{GS} - V_T$ should you choose to get high slew rate?
   (2 points)

3. Draw the schematic of a single-stage telescopic CMOS OTA loaded by C_L. Does the use of the cascodes change the GBW of the amplifier? What is the low-frequency gain of the cascade? Does the use of the cascodes change the current consumption of the amplifier? How many bias voltages we have to define additionally to the power supply voltages VDD and VSS?
   (4 points)

4. Draw the schematic of a single-stage symmetrical CMOS OTA loaded by C_L. Calculate the voltage gain A_{V0}, bandwidth BW and GBW. Which capacitance defines the frequency of the non-dominant pole and what is the frequency of the non-dominant pole? How is the value of the current factor B determined? Which voltage ($V_{GS} - V_T$) should be chosen for the transistors in the current mirror '$1:B$'?
   (8 points)

5. Draw the schematic of a symmetrical Miller CMOS OTA (2-stage amplifier) in a configuration that allows suppression of the positive zero.
   (2 points)

6. Draw the schematic of a folded cascode CMOS OTA loaded by C_L. What is the gain, bandwidth and GBW of this amplifier? What is the output resistance at the output node (where C_L is connected)? What is the frequency of the non-dominant pole and which parasitic capacitance determines this frequency? Specify the advantages of the folded cascade CMOS OTA and its disadvantage.
   (7 points)

7. Draw the schematic of a simple fully differential CMOS OTA with a CMFB amplifier.
   (2 points)

8. Calculate the input mismatch-offset voltage of a simple differential pair caused by the spreading of the load resistance ΔR_L.
   (2 points)