01. veljače 2013.

Kolegij **Analogni i analogno-digitalni integrirani sklopovi** slijedi knjigu 'Analog Design Essentials' (autor Willy M. C. Sansen, Springer, 2006)
Akademska godina 2012./2013.

POPIS PRIJEĐENOG GRADIVA

2. Blok predavanja:
    - Chapter 6: sl. 06.30 – 06.47
    - Chapter 7: sl. 07.1 – 07.32 (NE bipolarni tranzistori i BiCMOS)
    - Chapter 8: sl. 08.1 – 08.16
    - Chapter 11: sl. 11. 1 – 11.15
    - Chapter 15: sl. 15.1 – 15.55
    - Chapter 4: sl. 4.1 – 4.31
    - Chapter 20: sl. 20.1 – 20.44

Tipična pitanja:

Chapter 6:

1. Draw the schematic of a 2-stage Miller OTA that has PMOS transistors in the differential input stage. Draw the small-signal equivalent circuit. Calculate the voltage gain of the first and second stage A_{V1} and A_{V2}, bandwidth *BW* and *GBW* if the output is loaded by C_L = 2 pF and *GBW* = 10 MHz. Estimate the parasitic capacitance C_{n1} at the input of the second stage (for a rough estimate assume that for a transistor $C_{gs} = C_{gd} = C_{db}$).
2. How do you calculate the slew rate *SR* of a 2-stage Miller OTA when the slew rate depends on the internal activity of the amplifier? Calculate *SR/GBW*.
3. How do you calculate the slew rate *SR* of a 2-stage Miller OTA when the slew rate depends on the external capacitive load C_L?

Chapter 7:

1. Draw the schematic of a single-stage CMOS OTA. Write down the expression for the dominant pole and the expression for the non-dominant pole. The capacitance that defines the non-dominant pole is the sum of which parasitic capacitances?
2. Draw the schematic of a single-stage telescopic CMOS OTA. Does the use of the cascodes change the *GBW* of the amplifier? Does the use of the cascodes change the current consumption of the amplifier? How many bias voltages we have to define additionally to the power supply voltages *VDD* and *VSS*?
3. Draw the schematic of a single-stage symmetrical CMOS OTA (the simplest possible circuit) loaded by C_L. Calculate the voltage gain A_{V0}, bandwidth *BW* and *GBW*. Which capacitance defines the frequency of the non-dominant pole? What is the frequency of the non-dominant pole? What is the largest possible value of the current factor *B*? Which voltage ($V_{GS} - V_T$) should be chosen for the transistors in the current mirror *1:B*?
4. Draw the schematic of a single-stage symmetrical CMOS OTA with the cascodes.
5. Draw the schematic of a symmetrical Miller CMOS OTA (2-stage amplifier) in a configuration that allows suppression of the positive zero.

6. Draw the schematic of a folded cascode CMOS OTA loaded by C_L. What is the gain, bandwidth and *GBW* of this amplifier? What is the frequency of the non-dominant pole?
7. What are the advantages of the folded cascode CMOS OTA (sl. 07.27, 07.29, 07.30)? What is the drawback of this circuit (sl. 07.25)?

Chapter 8:

1. Draw the schematic of a simple fully differential CMOS OTA with a CMFB amplifier.
2. What are the requirements of the common-mode amplifier with respect to the differential amplifier in a fully-differential amplifier?
3. In the case of two consecutively connected fully-differential amplifiers, what is the load capacitance of the first amplifier for the common mode signal and what is the load capacitance for the differential signal? Draw the equivalent circuit used to calculate these two load capacitances.
4. Draw a simple fully-differential amplifier with MOS transistors working in the linear region (consisting of only 6 transistors).

Chapter 11:

1. Draw a simple input stage of a rail-to-rail amplifier (consisting of 2 NMOS transistors, 2 PMOS transistors and 2 current sources). What is the issue related to the transconductance g_m for this simple input structure with respect to the common mode input range?
2. Draw the input stage of a rail-to-rail amplifier that improves the variation of the transconductance g_m over the common mode input range.

Chapter 15:

1. Calculate the mismatch of a simple differential pair caused by the spreading of the load resistance ΔR_L.
2. What is the relative spreading of the output current of the current mirror?
3. What is the CMRR (common-mode rejection ratio)? Derive the expression for the CMRR for a simple differential pair. (sl. 15.18)

Chapter 4:

1. Napisati izraz za gustoću snage otpornika (za bijeli šum) i nacrtati nadomjesni sklop otpornika koji uključuje i izvor šuma. U kojim jedinicama se tipično izražava šum (dvije varijante)? Koliki je bijeli šum otpornika od 1 kΩ?
2. Gustoća sange šuma dva paralelna otpornika R_1 i R_2 (u ovom sklopu nema izvora napajanja). Nacrtati nadomjesni sklop koji uključuje izvore šuma i izračunati ekvivalentni šum paralelne kombinacije. (Napomena: zbrajati doprinose snaga)
3. Na izvor istosmjernog napona od 2 V i unutarnjeg otpora R_u od 1 kΩ priključen je otpornik R_T od 1 kΩ. Nacrtati nadomjesnu električnu shemu za proračun šuma i izračunati ekvivalentni šum (gustoću snage šuma ili efektivni napon šuma) u čvoru između otpornika R_u i R_T .
4. Na izvor istosmjerne struje od 1 mA i velikog unutarnjeg otpora priključena je serijska kombinacija otpornika R_1=1 kΩ i R_2=1 kΩ. Nacrtati nadomjesnu električnu shemu za proračun šuma i izračunati ekvivalentni šum (gustoću snage šuma ili efektivni napon šuma) u čvoru između otpornika R_1 i R_2.
5. Nacrtati spektar šuma RC filtra i izračunati ukupnu snagu šuma RC filtra ako je R=1 kΩ i C=10 pF.

6. Napisati izraz za 1/f šum otpornika. Kolika je tipična vrijednost konstante KF_R za silicij?
7. Kako se računa šum diode? Koji su doprinosi šumu diode? Nacrtati nadomjesni sklop diode koji uključuje i izvor šuma. Kako izgleda ukupan spektar šuma za diodu (označiti karakteristične vrijednosti: razinu bijelog šuma i jednu karakterističnu točku za 1/f šum).
8. Nacrtati dinamički nadomjesni sklop MOSFET-a za proračun šuma i koliko iznosi ekvivalentni ulazni napon šuma kada se u obzir uzimaju doprinosi bijelog šuma (nije potrebno u obzir uzeti doprinos otpora podloge)?
9. Kako se računa 1/f šum MOSFET-a? Ovisi li 1/f šum MOSFET-a o statičkoj radnoj točki? Ovisi li bijeli šum MOSFET-a o statičkoj radnoj točki?
10. Kako se može utjecati na i smanjiti bijeli šum MOSFET-a, a što treba učiniti da se smanji 1/f šum MOSFET-a?
11. Kako se računa ekvivalentni ulazni šum MOSFET-a M1 opterećenog aktivnim opterećenjem M2? Što se može učiniti da se smanji utjecaj šuma aktivnog opterećenja M2? Koristi li se isti postupak za smanjenje šuma aktivnog opterećenja za bijeli šum i za 1/f šum? (sl. 04.28 i 04.29)
12. Kako se definira faktor šuma pojačala?

Chapter 20:

1. Draw a schematic of the binary weighted resistor DAC. What are the typical issues related to this type of DAC?
2. Draw a schematic of the R-2R DAC. What are the typical issues related to this type of DAC?
3. Draw a schematic of the 4-bit current steering DAC. What are the typical issues related to this type of DAC? What is the advantage and disadvantage of using the thermometer code for the control of current sources?
4. Draw a schematic of the dual-slope ADC. What are the typical issues related to this type of ADC?
5. Draw a schematic of the 5-bit charge redistribution ADC. What are the typical issues related to this type of ADC?

Fizikalni parametri i konstante:

$\varepsilon_0 = 8{,}854 \cdot 10^{-14}$ F/cm
$\varepsilon'_{Si} = 11{,}7$
$\varepsilon'_{ox} = 3{,}9$
$\varepsilon_{Si} = 1{,}036$ pF/cm
$\varepsilon_{ox} = 0{,}345$ pf/cm
$v_{sat} = 10^7$ cm/s

Typical parameters of a 0,35 um CMOS technology:

$t_{ox} = 7$ nm
$L_{min} = 0{,}35$ μm

nMOS

U_{GS0n} = 0,55 V
K_n = 100 μA/V2
$1/\lambda = v_{En} \cdot L$
v_{En} = 4 V/μm

pMOS

U_{GS0p} = -0,55 V
K_p = -40 μA/V2
$1/\lambda = v_{Ep} \cdot L$
v_{Ep} = 8 V/μm

$C_{ox} = \varepsilon_{ox}/t_{ox}$ = 4,93 fF/μm^2 (for t_{ox} = 7 nm)
$g_{m,sat} = WC_{ox}\, v_{sat}$

$I_D = K_n(W/L)\cdot(U_{GS}-U_{GS0})^2(1+\lambda\cdot U_{DS})$
$C_{gs} = (2/3)WLC_{ox}$
$f_T = gm/(2\pi\, C_{gs})$

Konstante za proračun šuma:

KF_{RSi} = 2·10^{-21} S·cm^2
KF_{Rpoly} = 2·10^{-20} S·cm^2
KF_D = 10^{-21} A·cm^2
$KF_{F,nMOS}$ = 4·10^{-31} C^2/cm^2
$KF_{F,pMOS}$ = 10^{-32} C^2/cm^2
$KF_{F,JFET}$ = 10^{-33} C^2/cm^2

Jednadžbe za proračun šuma:

$$\overline{dv_R^{\,2}} = 4kTRdf$$

$$\overline{dv_{Rf}^{\,2}} = V_R^{\,2}\,\frac{KF_R R}{A_R}\,\frac{df}{f}$$

$$\overline{di_D^{\,2}} = 2qI_D df$$

$$\overline{di_{Df}^{\,2}} = I_D\,\frac{KF_D}{A_D}\,\frac{df}{f}$$

$$\overline{di_{DS}^{\,2}} = \frac{4kT}{R_{ch}}\,df$$

$$\overline{dv_{ieq}^{\,2}} = \frac{KF_F}{WL\cdot C_{ox}^{\,2}}\,\frac{df}{f}$$