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DIGITAL LEARNING CONTENT

CHAPTER-4

SEQUENTIAL CIRCUITS

4.1: Sequential circuits:

The circuits which are dependent on clock cycles and output depends on present as well as past inputs to generate any output, are known as **Sequential Circuits.**

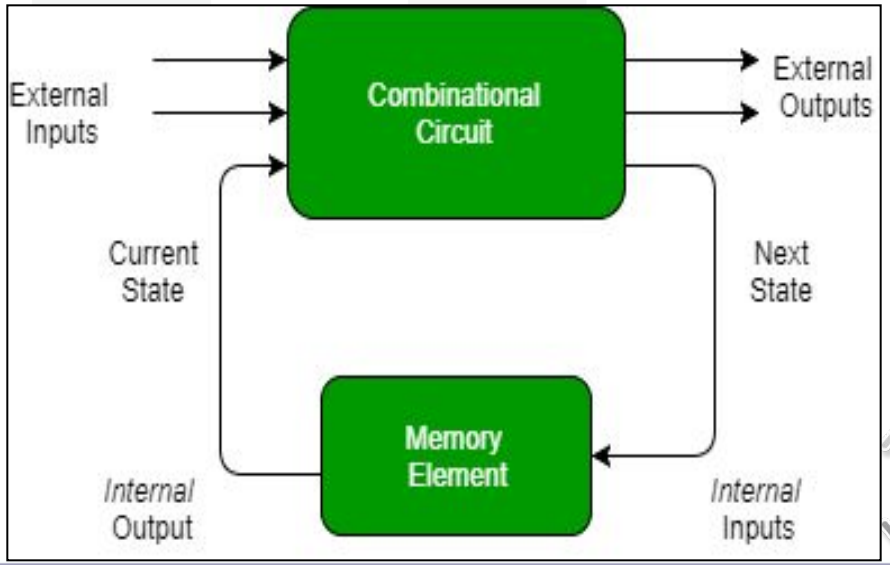


Image source https://media.geeksforgeeks.org/wp-content/uploads/1111-1.png

Difference between combinational & sequential circuits

PARAMETER FOR COMPARISON	COMBINATIONAL CIRCUIT	SEQUENTIAL CIRCUIT
Basic	The output depends only on the present state of the inputs.	The output depends on both the present input and past state output.
Storage capability	Does not store data.	Can store data.
Example	Adders, encoders, multiplexer, etcetera.	Flip-flop and latches, Counters, etc.,
Clock	Circuits do not rely on the clock.	Clock is utilized for triggering functions.
Feedback	No feedback is there.	Feedback is required.

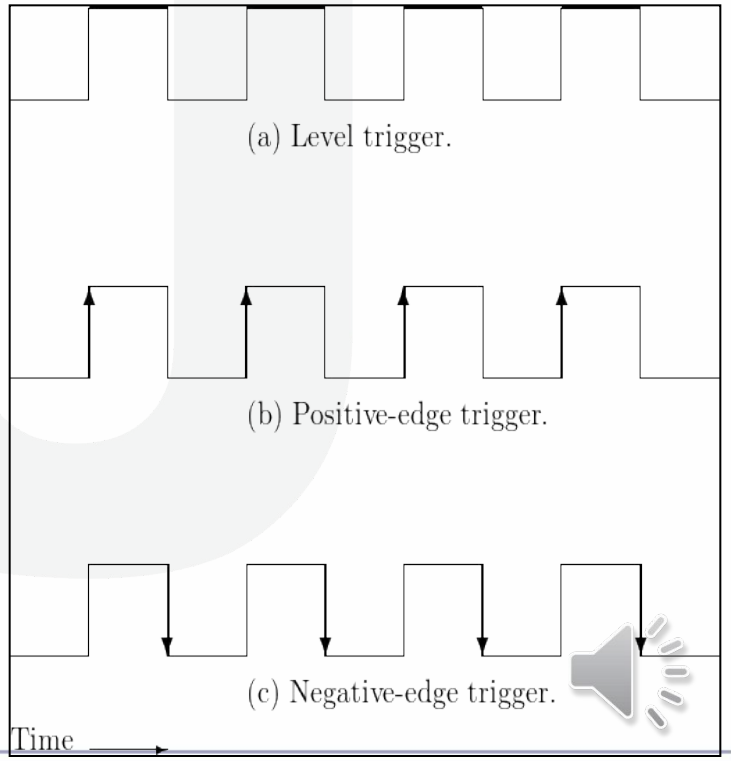
Image source https://www.allaboutcircuits.com/technical-articles/an-introduction-to-digital-signal-processing/

Type of sequential circuits

- **There are two types of sequential circuits**.
  - Asynchronous sequential circuits
  - Synchronous sequential circuits
- If some or all outputs of a sequential circuits do not change on occurrence of transition of active clock cycle, then the circuit is known as Asynchronous sequential circuits. So, the output is not synchronous with clock cycle.
- If some or all outputs of a sequential circuits change on occurrence of transition of active clock cycle, then the circuit is known as Synchronous sequential circuits.

4.2: Clock and Triggering

- **Clock signal is a square wave that alternates between 0 and 1**.
- Triggering: When any sequential circuit works on the input and generate a new input after some excitation/signal is applied. This is called triggered.
- Types of triggering:
  - Level Triggering
    - Positive level triggering & Negative Level Triggering
  - Edge Triggering



•Image source https://hob.cs.sonoma.edu/IntroCompOrg-x64/book173x.png

4.2: Clock and Triggering (Continue..)

- Level Triggering: If the sequential circuit is operated with the the clock signal is at the level 1 or level 0.
- If the sequential circuit is operated with the clock signal when it is in Logic High, then that type of triggering is known as **Positive level triggering.**
- If the sequential circuit is operated with the clock signal when it is in **Logic Low**, then that type of triggering is known as **Negative level triggering.**
- [https://www.tutorialspoint.com/digital_circuits/digital_circuits_sequential_circuits.htm]

4.2: Clock and Triggering (Continue..)

- Edge Triggering: If the sequential circuit is operated with the clock signal transitions either from Logic Low to Logic High or Logic High to Logic Low.
- If the sequential circuit is operated with the clock signal that is transitioning from Logic Low to Logic High, then that type of triggering is known as **Positive edge triggering**.
- If the sequential circuit is operated with the clock signal that is transitioning from Logic High to Logic Low, then that type of triggering is known as **Negative edge triggering**.

- [https://www.tutorialspoint.com/digital_circuits/digi... Image source https://hhb.cs.sonoma.edu/IntroCompOrg-x64/book173x.png

4.3: Flip-Flop

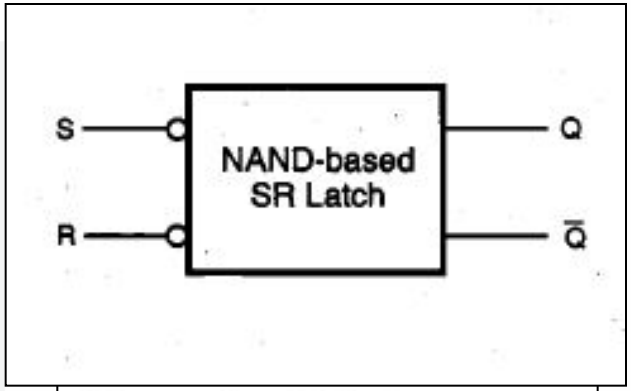
- **Flip-flop** is a binary storage device. It can store 1 bit of memory.
- It can have value “1” or “0” i.e. “HIGH” or “LOW”.
- Flip-flop remains in any of the above state for indefinite time until it is directed by an input signal to change its state.
- It stores data.
- It is also known as bi-stable multivibrator.
- Flip-flop can be un-clocked(transparent/Asynchronous) or clocked (Synchronous).
- Un-clocked flip-flop is known as Latch.

4.4: Latch

- Asynchronous flip-flop is known as Latch.

4.4.1: R-S Latch (Active Low):

- R and S means Reset and Set respectively.
- Q_{n+1} and Q_{n+1}' are the outputs which are



Inputs		Outputs		Comment
S	R	Q_{n+1}	Q_{n+1}'	
0	0	1	1	Invalid
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q_n	Q_n'	No change

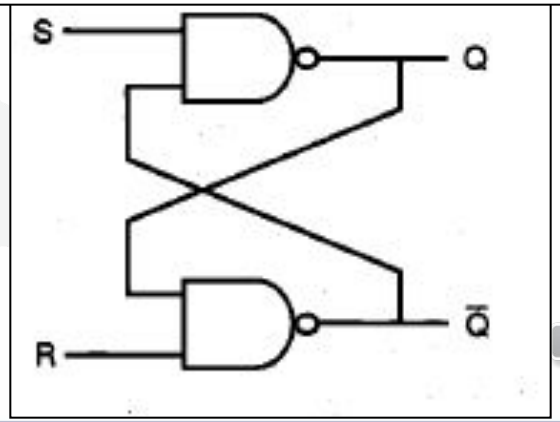


Image source: https://i.imgur.com/JRuPALB.png

4.4: Latch (Continue..)

- Asynchronous flip-flop is known as Latch.

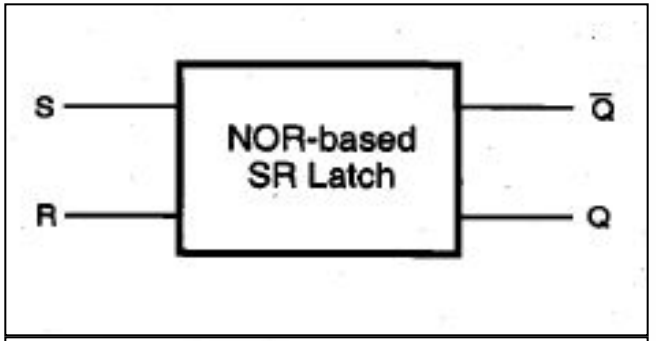
4.4.2: R-S Latch (Active high):

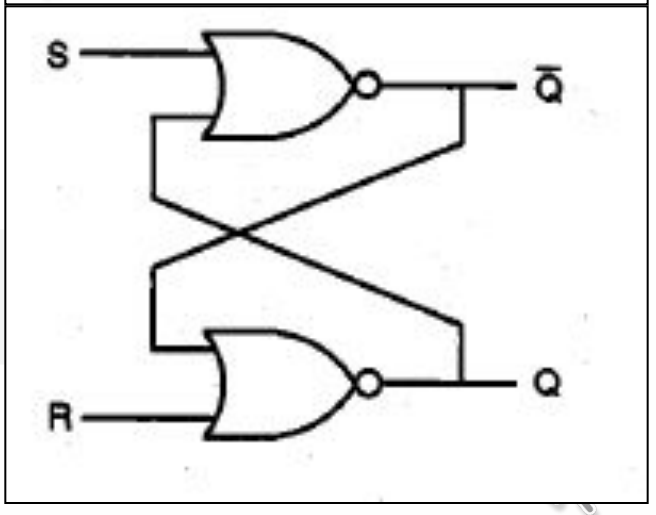
- R and S means Reset and Set respectively.
- Q_{n+1} and Q_{n+1}' are the outputs which are complements of each other.

The condition when Qn+1 and Qn+1 ' are same, it is known as "Race-Around"condition.

- **same, it is**

Inputs		Outputs		Comment
S	R	Q_{n+1}	Q_{n+1}'	
0	0	Q_n	Q_n'	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Invalid





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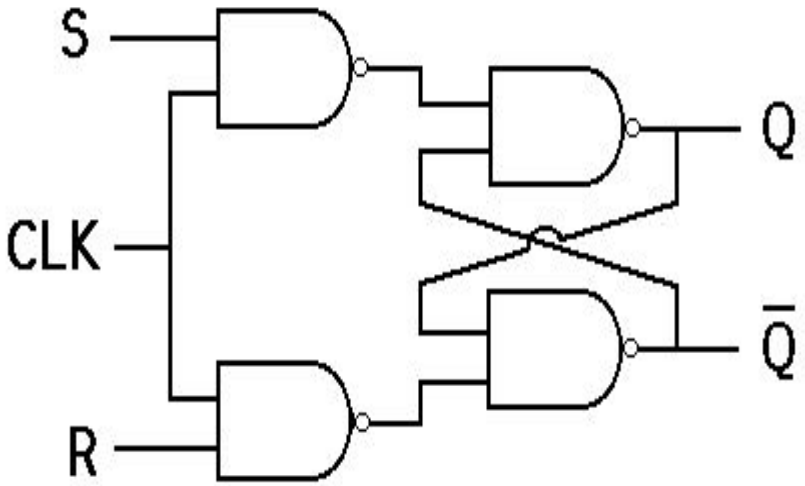
4.5.1: R-S Flip-Flops (Using NAND gates)

- The SR (Set-Reset) flip-flop is one of the simplest sequential circuits and consists of two gates connected.
- The output of each gate is connected to one of the inputs of the other gate.
- The circuit has two active low inputs marked S & R, as well as two outputs, Q & Q'.

Clk	Inputs		Outputs		Comment
	S	R	Q_{n+1}	Q_{n+1}'	
x	0	0	Q_n	Q_n'	No change
↑	0	0	Q_n	Q_n'	Invalid
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	0	0	Invalid



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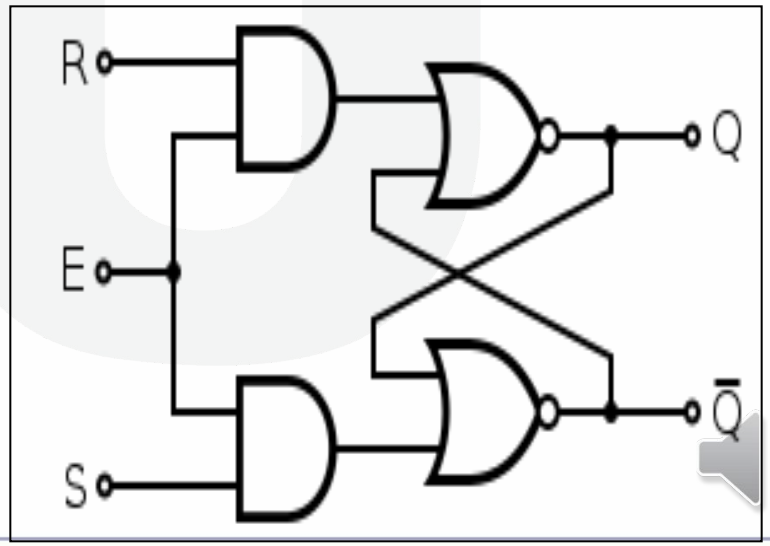
4.5.2: R-S Flip-Flops (Using NOR gates)

- The SR (Set-Reset) flip-flop is one of the simplest sequential circuits and consists of two gates connected.
- The output of each gate is connected to one of the inputs of the other gate.
- The circuit has two active low inputs marked S & R, as well as two outputs, Q & Q'.
- .

Clk	Inputs		Outputs		Comment
	S	R	Q_{n+1}	Q_{n+1}'	
x	0	0	Q_n	Q_n'	No change
↑	0	0	Q_n	Q_n'	Invalid
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	0	0	Invalid



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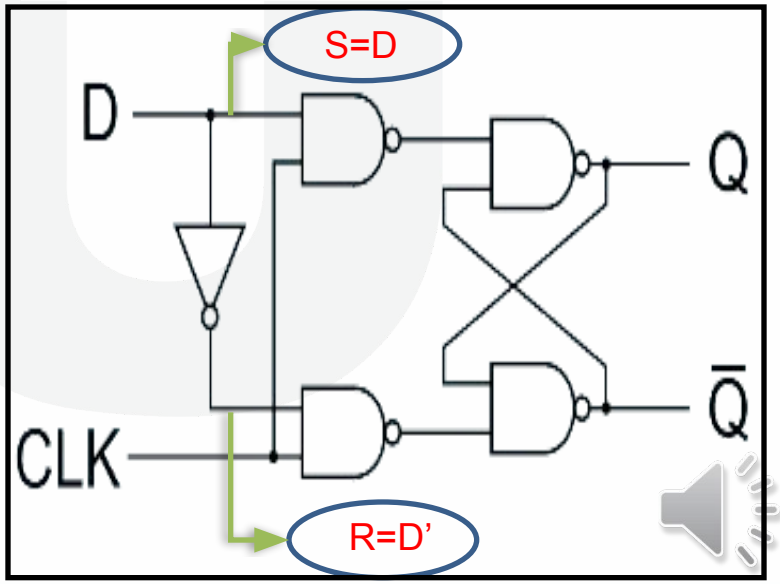
4.6: D Flip-Flop

- The D flip-flop is modification in S-R flip-flop.
- One inverter is connected between S & R. So that both R and S can not be same at a time. It eliminates “Race around” condition.
- The circuit has one input marked D, as well as two outputs, Q & Q’.
- It is also known as ‘Data flip-flop’ or ‘Delay

Clk	D	Outputs		Comment
		Q_{n+1}	Q_{n+1}'	
↑	0	0	1	Reset
↑	1	1	0	Set



Clk	D	Inputs		Outputs		Comment
		S	R	Q_{n+1}	Q_{n+1}'	
↑	0	0	1	0	1	Reset
↑	1	1	0	1	0	Set

•Image source: https://electronicsforu.com/wp-contents/uploads/2017/08/d-flip-flop.png

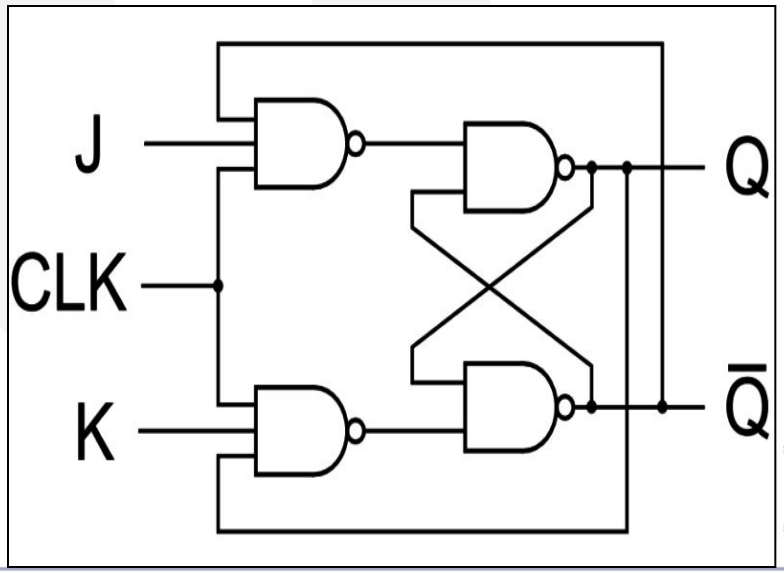
4.7: J-K Flip-Flop

- The output of each gate is connected to one of the inputs of the other gate.
- The circuit has two active low inputs marked J & K, as well as two outputs, Q & Q'.

It is the solution of Race around condition occurred in R-S Flip-Flop

- It is the solution of Race around condition occurred in R-S Flip-Flop.

Clk	Inputs		Outputs		Comment
	J	K	Q_{n+1}	Q_{n+1}'	
x	0	0	Q_n	Q_n'	No change
↑	0	0	Q_n	Q_n'	No change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	Q_n'	Q_n	Toggle



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4.8: T Flip-Flop

- The circuit has one input T. It is nothing but J and K shorted and marked as T. It has two outputs, Q & Q'.
- This flip-flop provides two possibilities of output. One is "No-change" and the other one is "Toggle".
- T=J=K

Clk	T	Inputs		Outputs		Comment
		J	K	Q_{n+1}	Q_{n+1}'	
x	0	0	0	Q_n	Q_n'	No change
↑	0	0	0	Q_n	Q_n'	No change
↑	1	1	1	Q_n'	Q_n	Toggle

Clk	T	Outputs		Comment
		Q_{n+1}	Q_{n+1}'	
x	0	Q_n	Q_n'	No change
↑	0	Q_n	Q_n'	No change
↑	1	Q_n'	Q_n	Toggle

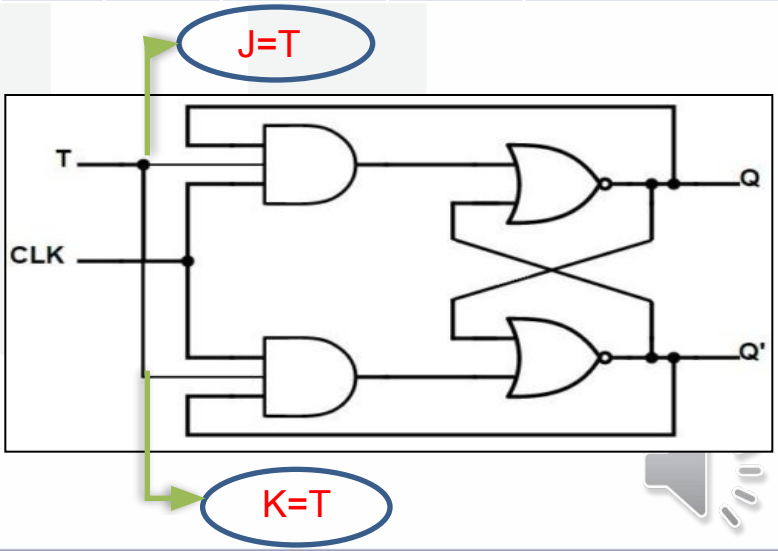


Image source: https://www.electronicsforu.com/wp-contents/uploads/2019/04/t-flip-flop-1-500x266.jpg

4.9: Excitation table of flip flops

- Truth table of flip-flop gives Next state based on inputs, whereas excitation table means to first mention present state and next state, then find out the suitable input conditions which leads to the given next state.

4.9.1: Excitation table of S-R flip flop

- Here, Truth table and excitation table of SR flip-flop is shown.
  - Take first case in Excitation table, Qn=0 and Qn+1=0.
  - Now find the same condition in truth table when Qn=0 and Qn+1=0. It is possible when S=R=0 and S=0 and R=1.
  - It means in both cases S=0 and R can be 0 or 1. So, we write as S=0 and R=X in excitation table.
  - Similarly, we can solve other

Inputs		Outputs	
		Present State	Next State
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	invalid	
1	1	invalid	

Truth Table of SR Flip-Flop

Outputs		Inputs	
Present State	Next State		
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation Table of SR Flip-Flop

Image source: https://www.electronicsforu.com/wp-contents/uploads/2019/04/t-flip-flop-1-500x266.jpg

4.9.2: Excitation table of J-K flip flop

- Here, Truth table and excitation table of JK flip-flop is shown.
  - Take first case in Excitation table, Qn=0 and Qn+1=0.
  - Now find the same condition in truth table when Qn=0 and Qn+1=0. It is possible when J=K=0 and J=0 and K=1.
  - It means in both cases J=0 and K can be 0 or 1. So, we write as J=0 and K=X in excitation table.
  - Similarly, we can solve other

Inputs		Outputs	
		Present State	Next State
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table of JK Flip-Flop

Outputs		Inputs	
Present State	Next State		
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table of JK Flip-Flop

Image source: https://www.electronicsforu.com/wp-contents/uploads/2019/04/t-flip-flop-1-500x266.jpg

4.9.2: Excitation table of D flip flop

- Here, Truth table and excitation table of D flip-flop is shown.
  - Take first case in Excitation table, Qn=0 and Qn+1=0.
  - Now find the same condition in truth table when Qn=0 and Qn+1=0. It is possible when D=0.
  - Similarly, Qn+1=1 is only possible when D=1.

Input	Outputs	
	Present State	Next State
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Truth Table of D Flip-Flop

Outputs		Input
Present State	Next State	
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation Table of D Flip-Flop

Image source: https://www.electronicsforu.com/wp-contents/uploads/2019/04/t-flip-flop-1-500x266.jpg

4.9.2: Excitation table of T flip flop

- Here, Truth table and excitation table of T flip-flop is shown.
  - Take first case in Excitation table, Qn=0 and Qn+1=0.
  - Now find the same condition in truth table when Qn=0 and Qn+1=0. It is possible when T=0.
  - Similarly, we can solve other cases.

Input	Outputs	
	Present State	Next State
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table of T Flip-Flop

Outputs		Input
Present State	Next State	
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table of T Flip-Flop

Image source: https://www.electronicsforu.com/wp-contents/uploads/2019/04/t-flip-flop-1-500x266.jpg

4.10: Characteristics equation of flipflops

- For finding the characteristic equation, first we need to re-arrange truth table of the flip –flop.
- It must consider the present state Qn also as input along with input terminals and the next state Qn+1 as output.
- Prepare k-map for the output.
- Reducing k-map will lead to the characteristic equation of the respective flip-flop.
- Next slides will include re-arranged truth-table, k map and reduced equation for the respective flip-flop.

4.10.1: Characteristics equation of R-S flip flop

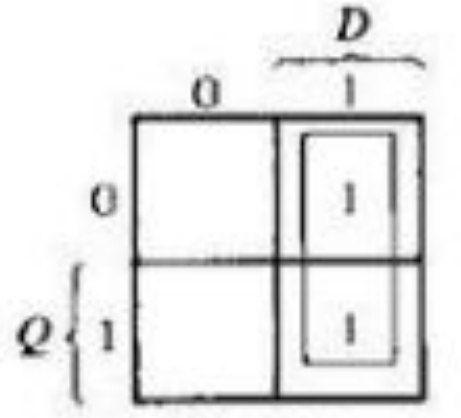
Inputs			Output	Remarks
S	R	Q_n (Present State)	Q_{n+1} (Next State)	States and Conditions
0	0	X	Q_n	Hold State condition S = R = 0
0	1	X	0	Reset state condition S = 0 , R = 1
1	0	X	1	Set state condition S = 1 , R = 0
1	1	X	Indeterminate	Indeterminate state condition S = R = 1

$$Q_{n+1} = (SR + SR') (Q_n + Q'_n) + Q_n (S'R' + SR')$$

$$Q_{n+1} = S + Q_nR'$$

4.10.2: Characteristics equation of D flip flop

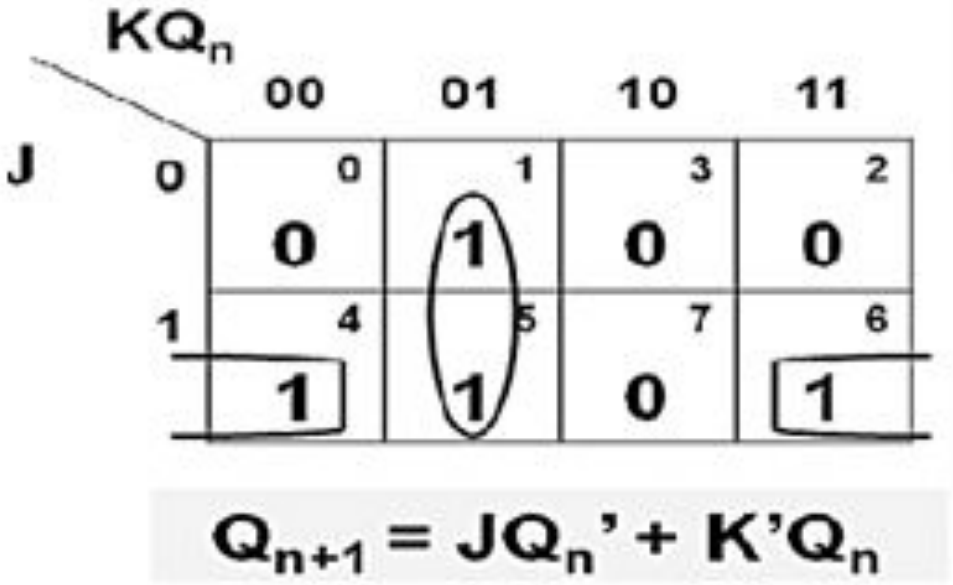
Inputs		Output
D	Q_n (Present State)	Q_{n+1} (Next State)
0	0	0
0	1	1
1	0	0
1	1	1



$Q_{n+1}=D$

4.10.3: Characteristics equation of JK flip flop

Inputs			Output
J	K	Q_n (Present State)	Q_{n+1} (Next State)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



$$Q_{n+1} = JQ_n' + K'Q_n$$

4.10.4: Characteristics equation of T flip flop

Inputs		Output
T	Q_n (Present State)	Q_{n+1} (Next State)
0	0	0
0	1	1
1	0	1
1	1	0

T\Qn	Qn’	Qn
T’	0	1
T	1	0

$$Q_{n+1}=TQn'+T'Qn$$

4.11: Conversion among flip-flops

- Follow these **steps** for converting one flip-flop to the other.
- Consider the **characteristic table** of desired flip-flop.
- Fill the excitation values inputs of given flip-flop for each combination of present state and next state.
- Get the simplified expressions for each excitation input. If necessary, use Kmaps for simplifying.
- Draw the circuit diagram of desired flip-flop according to the simplified expressions using given flip-flop and necessary logic gates.
- In this ppt, two conversions are shown, other conversion can be carried out similarly.

4.11: Conversion among flip-flops (Continue..)

- The **excitation table** for all flip-flops is shown below.

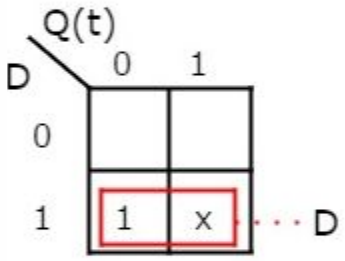
Present State	Next State	SR flip-flop inputs		D flip-flop input	JK flip-flop inputs		T flip-flop input
Qt	Qt+1	S	R	D	J	K	T
0	0	0	x	0	0	x	0
0	1	1	0	1	1	x	1
1	0	0	1	0	x	1	1
1	1	x	0	1	x	0	0

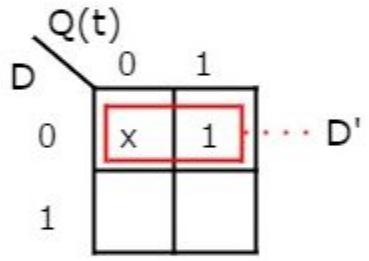
- Now using this table and the steps mentioned, we will do the conversion between flip-flops.

4.11.1: SR to D Flip flop conversion

- We know that SR flip-flop has two inputs S & R. So, write down the excitation values of SR flip-flop for each combination of present state and next state values. (Use the prior knowledge of Characteristic table of Flip-Flops.
- The table shows the characteristic tal[illegible] K-Map for S K-Map for R [illegible]on

D flip-flop input	Present State	Next State	SR flip-flop inputs	
D	**Q**t	**Q**t+1	**S**	**R**
0	0	0	0	x
0	1	0	0	1
1	0	1	1	0
1	1	1	x	0

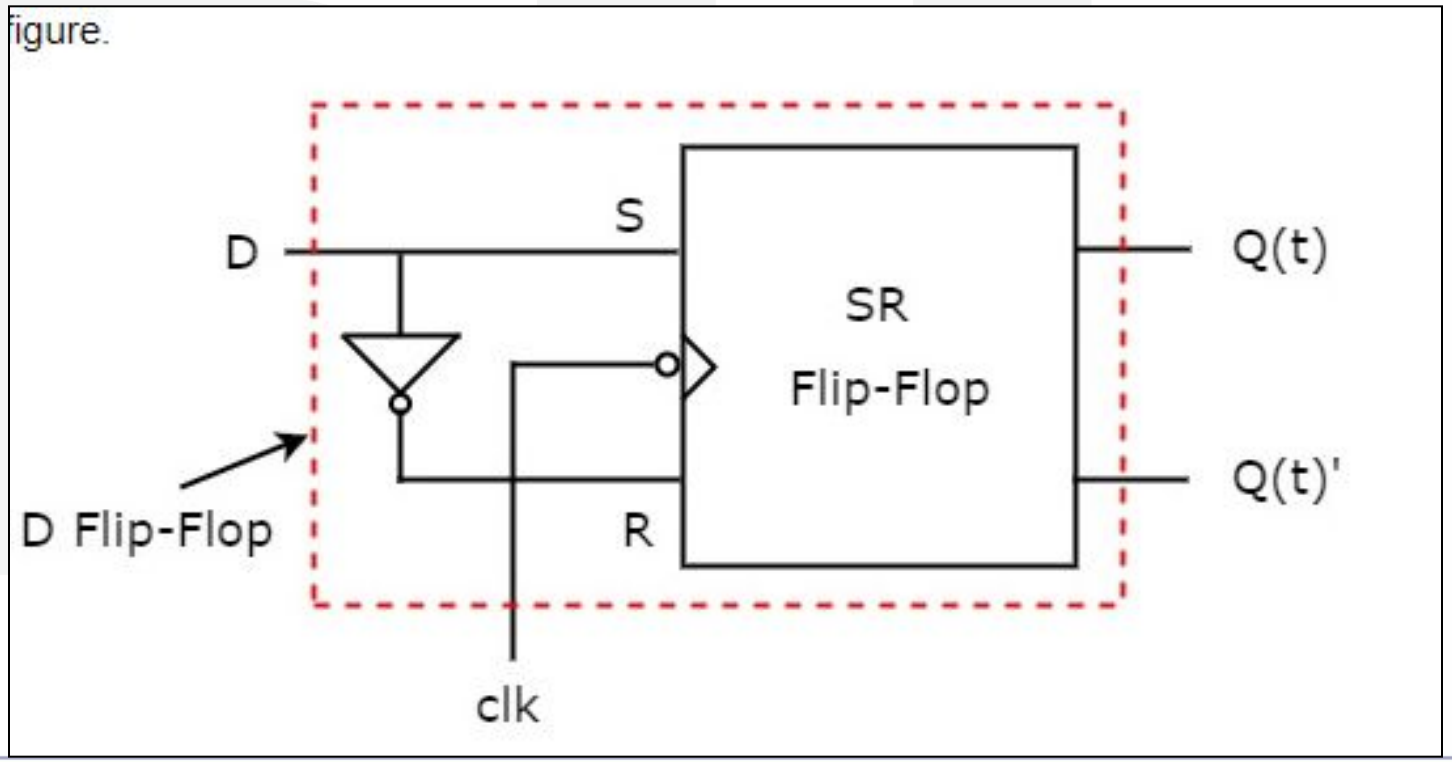




S=D and R=D'

From above expressions, we can design the circuit diagram of D Flip-Flop (Shown in next slide)

4.11.1: SR to D Flip flop conversion (Continue..)



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4.11.2: D to T Flip flop conversion

- We know that D flip-flop has single input D. So, write down the excitation values of D flip-flop for each combination of present state and next state values.
- The following table shows the characteristic table of T flip-flop along with the **excitation input** of D flip-flop. From the above table, we can directly write

T flip-flop input	Present State	Next State	D flip-flop input
T	**Q**tt	**Q**t+1	**D**
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

□ $D=T \oplus Q(t)$, from this equation the circuit can be designed as follows.

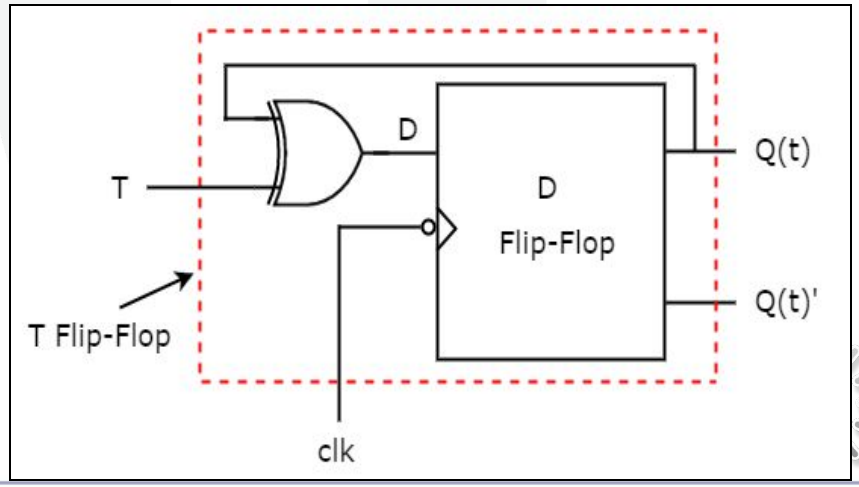

Image source: https://www.tutorialspoint.com/digital_circuits/images/circuit_diagram_of_t_flip_flop.jpg

4.12: Applications of flip flops

- These are the various types of flip-flops being used in digital electronic circuits and the applications of Flip-flops are as specified below.
  - Counters
  - Frequency Dividers
  - Shift Registers
  - Storage Registers

4.13: Shift Registers

- One flip-flop can store one-bit of data.
- To store multiple bits of information, we require multiple flip-flops. The group of flip-flops, which are used to store the binary data is known as register.
- If the register is capable of shifting bits either towards right hand side or towards left hand side is known as shift register.
- An ‘N’ bit shift register contains ‘N’ flip-flops.
- Following are the four types of shift registers based on applying inputs and accessing of outputs.
  - Serial In – Serial Out shift register
  - Serial In – Parallel Out shift register
  - Parallel In – Serial Out shift register
  - Parallel In – Parallel Out shift register

4.13.1: Serial In Serial Out (SISO) Shift Registers

- The shift register, which allows serial input and produces serial output is known as Serial In – Serial Out SISO shift register.
- The block diagram of 3-bit SISO shift register is shown in the figure.
- IT consists of three D flip-flops, which are cascaded.
- All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.
- In this shift register, we can send the bits serially from the input of left most D flip-flop. (Serial-input)
- For every positive edge of clock, the data shifts from one stage to the next. So, we can receive the bits serially from the output of right most D flip-flop. (Serial-output)

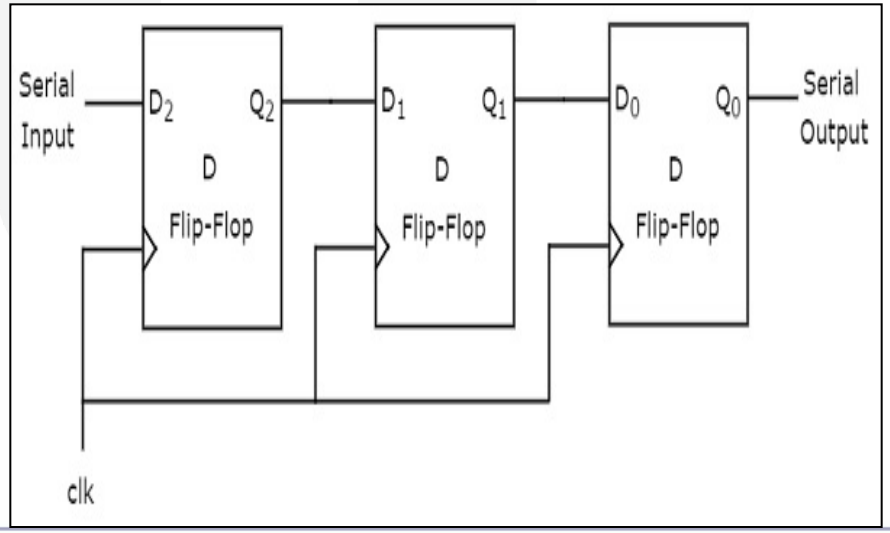

Image source: Google

4.13.2: Serial In Parallel Out (SIPO) Shift Registers

- The shift register, which allows serial input and produces parallel output is known as Serial In – Parallel Out SIPO shift register. The block diagram of 3-bit SIPO shift register is shown in the figure.
- It consists of three D flip-flops, which are cascaded.
- All these flip-flops are synchronous with each other since, the same clock is applied to each one.
- In this shift register, we can send the bits serially from the input of left most D flip-flop (serial input).
- For every positive edge of clock, the data shifts from one stage to the next. In this case, we can access the outputs of each D flip-flop in parallel (Parallel Output).

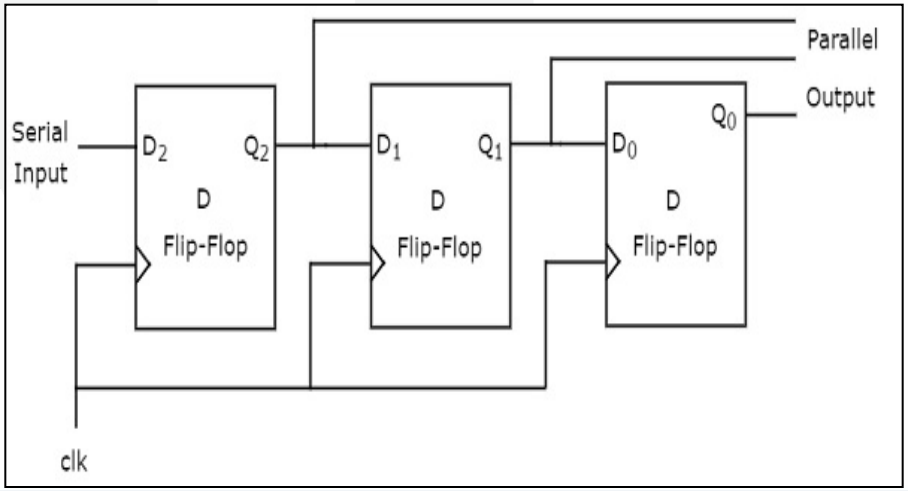

Image source: Google

4.13.3: Parallel In Serial Out (PISO) Shift Registers

- The shift register, which allows parallel input and produces serial output is known as Parallel In – Serial Out (PISO) shift register. The **block diagram** of 3-bit PISO shift register is shown here. IT consists of three D flip-flops, which are cascaded.
- All these flip-flops are synchronous with each other since, the same clock is applied to each one.
- In this shift register, we can apply the parallel inputs to each D flip-flop by making Preset Enable to 1.
- For every positive edge of clock signal, the data shifts from one stage to the next. So, we will get the serial output from the right most D flip-flop.

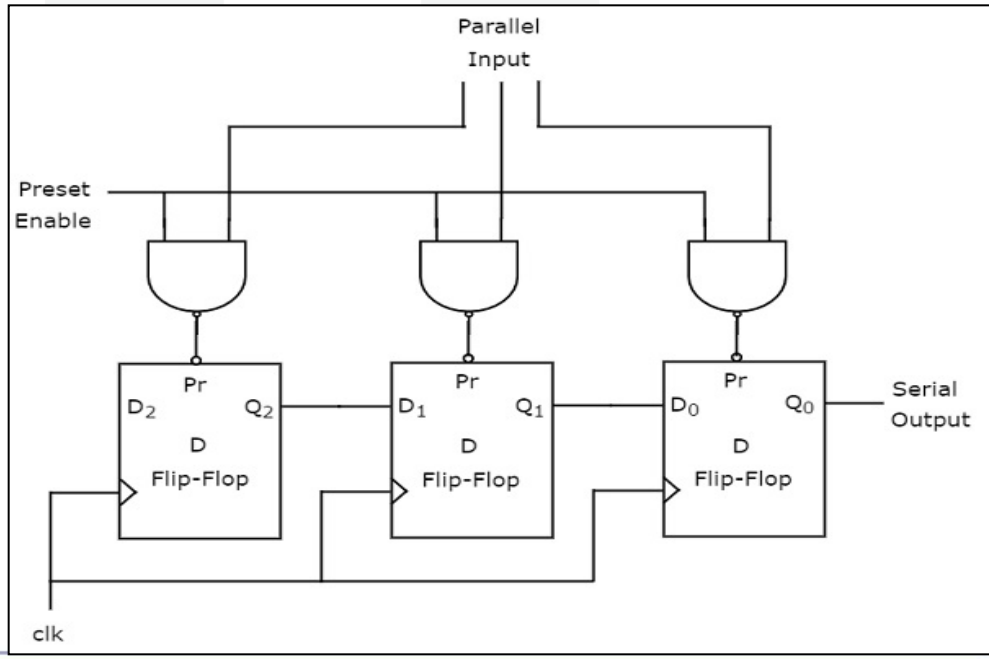

Image source: Google

4.13.4: Parallel In Parallel Out (PIPO) Shift Registers

- The shift register, which allows parallel input and produces parallel output is known as Parallel In – Parallel Out (PIPO) shift register.
- The PIPO shift register is the simplest of the four configurations. It has only three connections, the parallel input (PI) which determines what enters the flip-flop, the parallel output (PO) and the sequencing clock signal (Clk).
- Similar to the SISO shift register, this type of register also acts as a temporary storage device or as a time delay device, with the amount of time delay being varied by the frequency of the clock pulses.

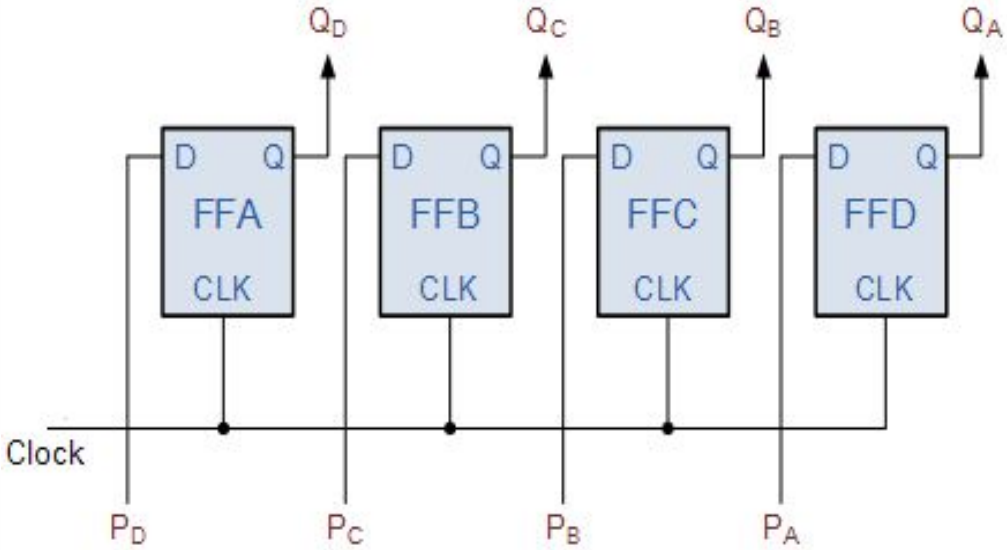

Image source: Google

4.14: Application of Shift registers

- Shift registers can be used in Parallel to serial converter, Serial to parallel converter, sequence generator, etc.,

4.15: Counters

- An ‘N’ bit binary counter consists of ‘N’ T flip-flops. If the counter counts from 0 to $2^N - 1$, then it is called as binary **up counter**. Similarly, if the counter counts down from $2^N - 1$ to 0, then it is called as binary **down counter**.
- There are two **types of counters** based on the flip-flops that are connected in synchronous or not.
  - Asynchronous counters
  - Synchronous counters

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4.15: Counters (Difference between Synchronous and asynchronous counters))

SYNCHRONOUS COUNTER	SYNCHRONOUS COUNTER
In synchronous counter, all flip flops are triggered with same clock simultaneously.	In asynchronous counter, different flip flops are triggered with different clock, not simultaneously.
Synchronous Counter is faster than asynchronous counter in operation.	Asynchronous Counter is slower than synchronous counter in operation.
It is also called Parallel Counter.	It is also called Serial Counter.
Synchronous Counter designing as well implementation are complex due to increasing the number of states.	Asynchronous Counter designing as well as implementation is very easy.
Synchronous Counter will operate in any desired count sequence.	Asynchronous Counter will operate only in fixed count sequence (UP/DOWN).
Synchronous Counter examples are: Ring counter, Johnson counter.	Asynchronous Counter examples are: Ripple UP counter, Ripple DOWN counter.
Propagation delay is less.	There is high propagation delay.

4.15.1: Asynchronous Counters

- If the flip-flops do not receive the same clock signal, then that counter is called as Asynchronous counter.
- The clock is applied only to first flip-flop. The remaining flip-flops receive the clock signal from output of its previous stage flip-flop.
- Therefore, the outputs of all flip-flops do not affect at the same time.
- Asynchronous counters are further divided among two main categories.
  - Asynchronous Binary up counter
  - Asynchronous Binary down counter
- N-bit counter will require N number of flip-flops for the implementation.
- N-bit counter will count total 2^N states. i.e. 0 to 2^N -1.

4.15.1.1: Asynchronous Binary Up Counters

No of negative edge of Clock	Q_2 MSB	Q_1	Q_0 LSB
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

- An ‘N’ bit Asynchronous binary up counter consists of ‘N’ T flip-flops. It counts from 0 to 2^{N-1}.
- The block diagram of 3-bit Asynchronous binary up counter is shown in the figure.

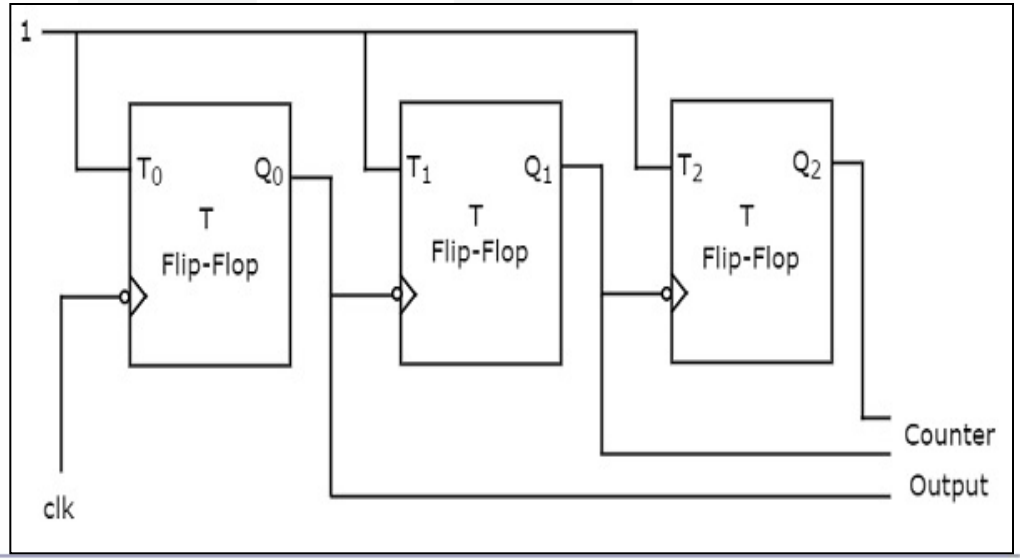

Image source: Google

4.15.1.2: Asynchronous Binary Down Counters

No of negative edge of Clock	Q_2 MSB	Q_1	Q_0 LSB
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1

- An ‘N’ bit Asynchronous binary dowwn counter consists of ‘N’ T flip-flops. It counts from 2^{N-1} to 0.
- The block diagram of 3-bit Asynchronous binary down counter is shown in the figure.

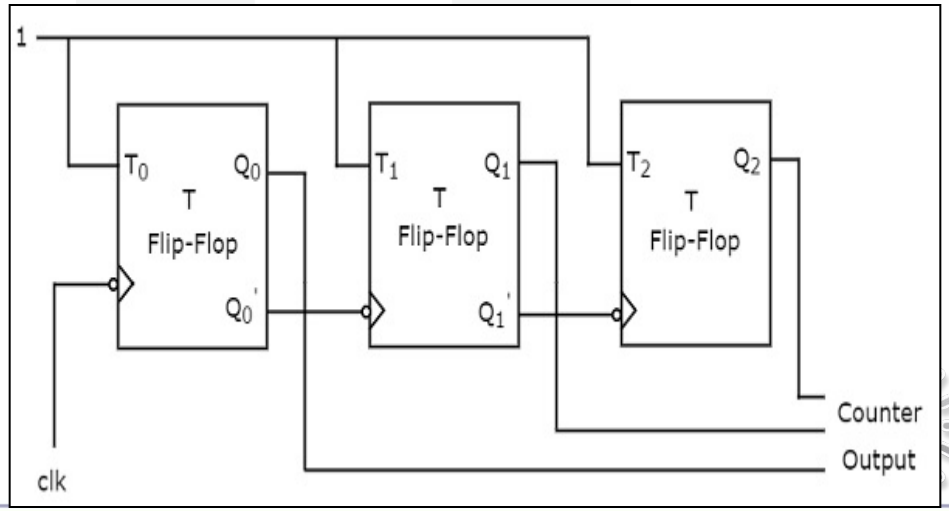

Image source: Google

4.15.2: Synchronous Counters

- If all the flip-flops receive the same clock signal, then that counter is called as Synchronous counter.
- Therefore, the outputs of all the flip-flop affect at the same time.
- There are two types of counter synchronous counters.
  - Synchronous binary up counters
  - Synchronous binary down counters
- N-bit counter will require N number of flip-flops for the implementation.
- N-bit counter will count total 2^N states. i.e. 0 to 2^N -1.

4.15.2.1: Synchronous Binary Up Counters

- The clock pulses are fed directly to each of the J-K flip-flops and both the J and K inputs are tied together, but only in the first flip-flop, FFA are they connected to logic “1” which makes the flip-flop toggle on every clock pulse.
- This counter counts sequentially on every clock pulse the resulting outputs counts from 0 (0000) to 15 (1111). Therefore, it is known as a 4-bit Synchronous Up Counter.

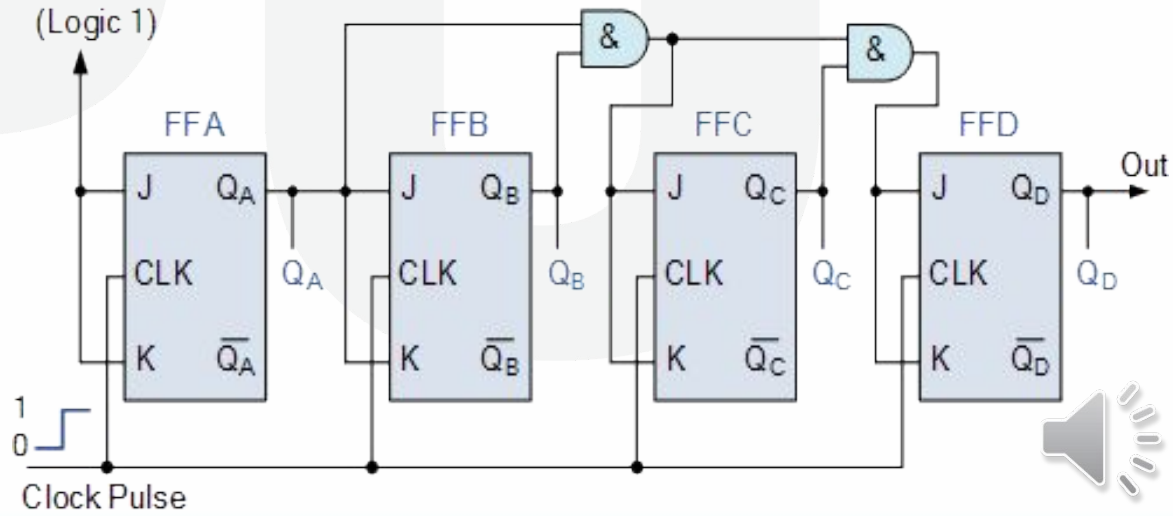

Image source: Google

4.15.2.1: Synchronous Binary Up Counters (Continue)

No of Clock pulse	Q_D MSB	Q_C	Q_B	Q_A LSB
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1

No of Clock pulse	Q_D MSB	Q_C	Q_B	Q_A LSB
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

4.15.2.1: Synchronous Binary Up Counters (Continue)

- Figure shows the timing diagram of synchronous binary up counter.
- Similarly, timing diagram of other counters can also be drawn.

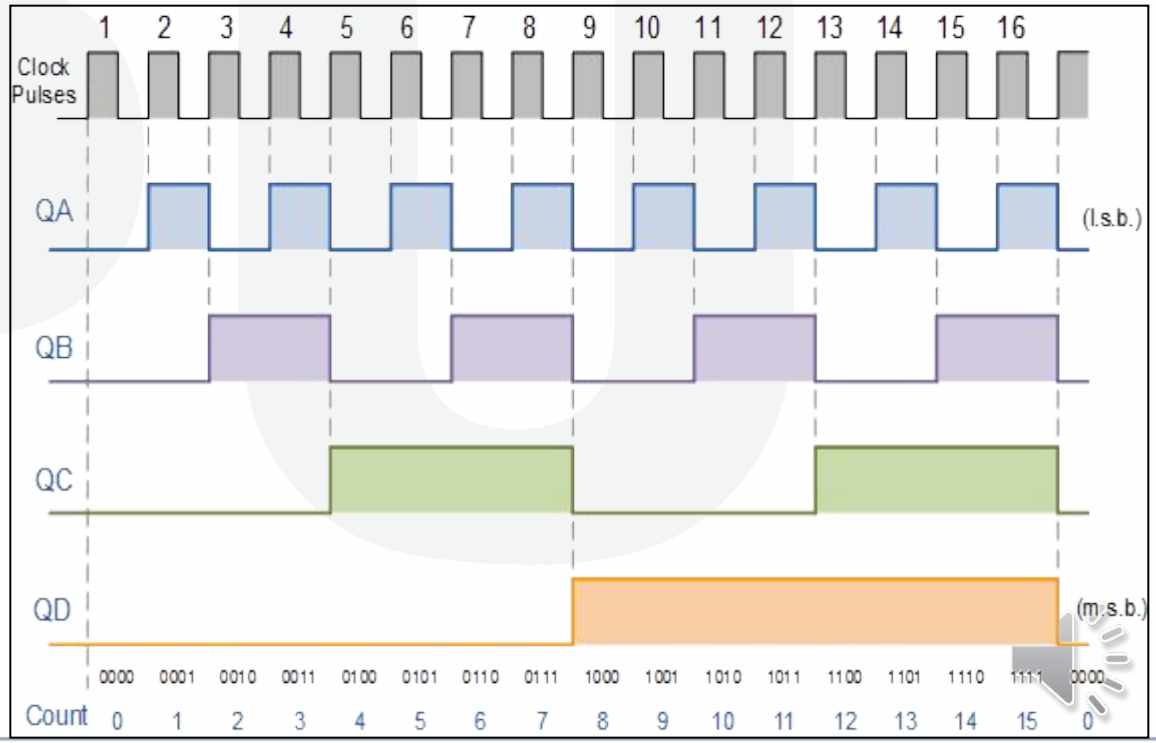

Image source: Google

4.15.2.2: Synchronous Binary down Counters

- AND gates are connected to the Q output of the flip-flops as shown to produce a waveform timing diagram the reverse of the above.
- This counter counts sequentially on every clock pulse the resulting outputs counts from 15 (1111) to 0 (0000). Therefore, it is known as a 4-bit Synchronous down Counter.

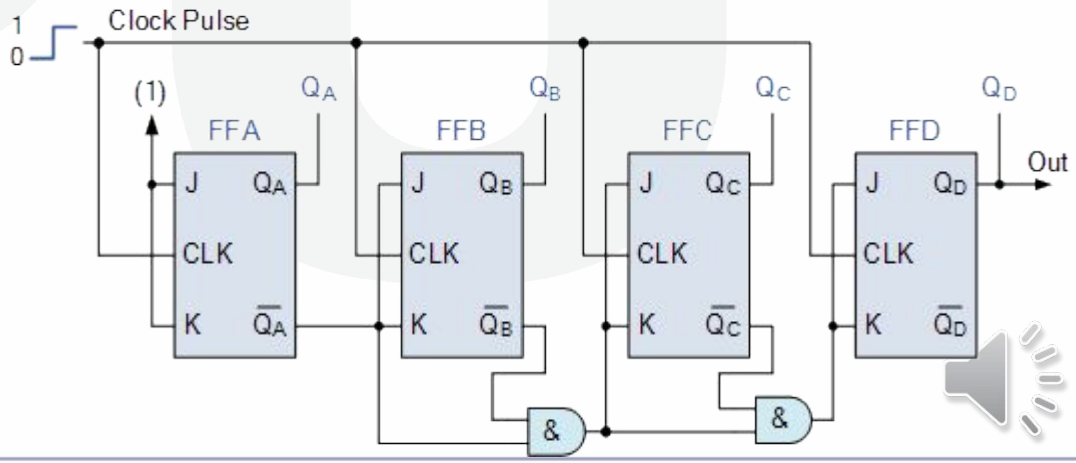

Image source: Google

4.15.2.2: Synchronous Binary down Counters (Continue)

No of Clock pulse	Q_D MSB	Q_C	Q_B	Q_A LSB
15	1	1	1	1
14	1	1	1	0
13	1	1	1	1
12	1	1	1	0
11	1	0	0	1
10	1	0	0	0
9	1	0	0	1
8	1	0	0	0

No of Clock pulse	Q_D MSB	Q_C	Q_B	Q_A LSB
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

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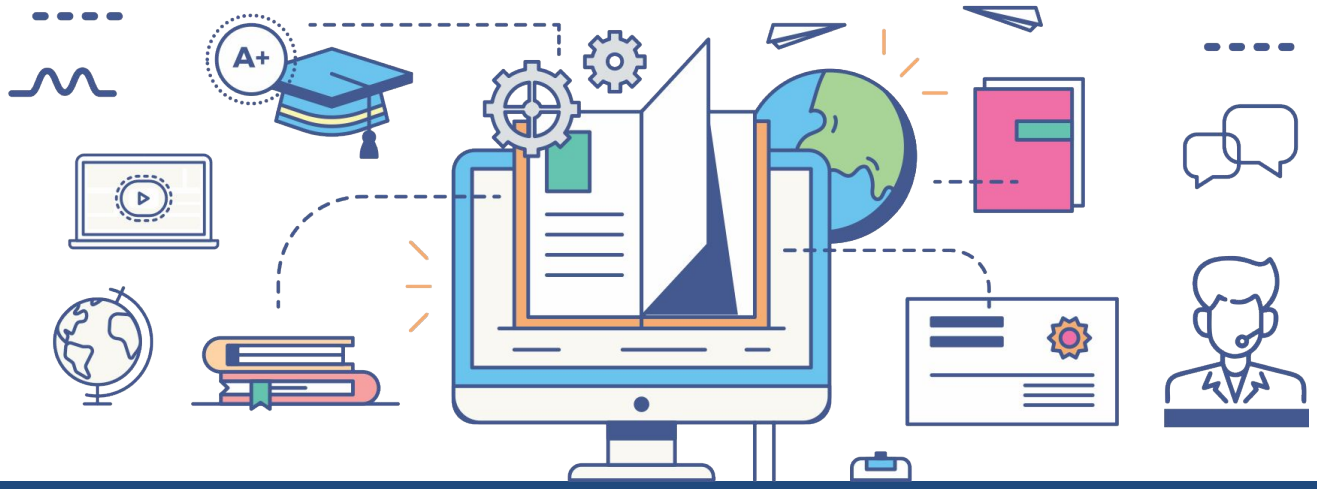

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