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Digital Electronics (203105201)

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CHAPTER-6

Semiconductor Memories And Programmable Logic Devices

Classification and characteristics of memories

There are two types of memories that are used in digital systems.

Random-access memory (RAM): Perform both the write and read operations. A memory device that maintains its data permanently (or until the device is reprogrammed). Non-volatile: It maintains its data even without power supply. Used to store programs such as the BIOS, data such as look tables.

Read-only memory (ROM): Perform only the read operation. A memory device that can be read and written. Volatile, it loses its data when the power supply is switched-off when the supply is switched-on it contains random data.

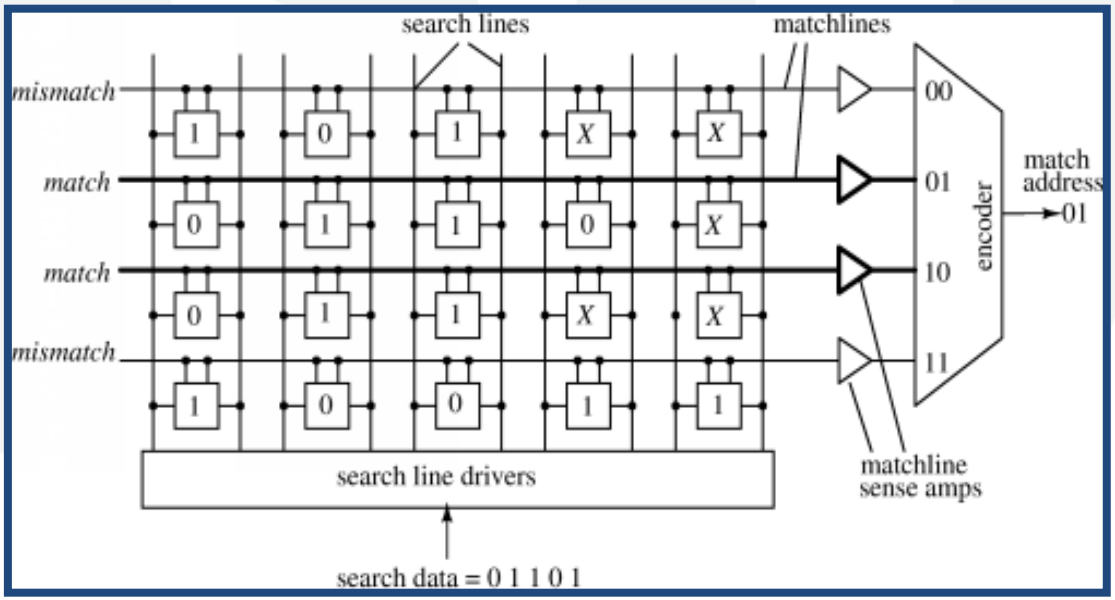
Static RAM (SRAM): The basic element of a static RAM cell is the D-Latch. Data remains stored in the cell until it is intentionally modified. SRAM is fast.

Dynamic RAM: DRAM stores the binary information in the form of electric charges on capacitors. High density, high capacity, low cost, low speed, low power consumption.

Content addressable memory (CAM)

Content-addressable memory (CAM): is a special type of computer memory used in certain very-high-speed searching applications.

CAM is frequently used in networking devices where it speeds forwarding information base and routing table operations.



Introduction of PLD

Programmable logic device (or PLD) is a general name for a digital integrated circuit capable of being programmed to provide a variety of different logic functions. In this section we will discuss several types of combinational PLDs, and later we will discuss sequential PLDs. Simple combinational PLDs are capable of realizing from 2 to 10 functions of 4 to 16 variables with a single integrated circuit. More complex PLDs may contain thousands of gates and flip-flops. Thus, a single PLD can replace a large number of integrated circuits, and this leads to lower cost designs. When a digital system is designed using a PLD.

Programmable Logic Array: A programmable logic array (PLA) performs the same basic function as a ROM. A PLA with n inputs and m outputs can realize m functions of n variables. The internal organization of the PLA is different from that of the ROM. The decoder is replaced with an AND array which realizes selected product terms of the input variables.

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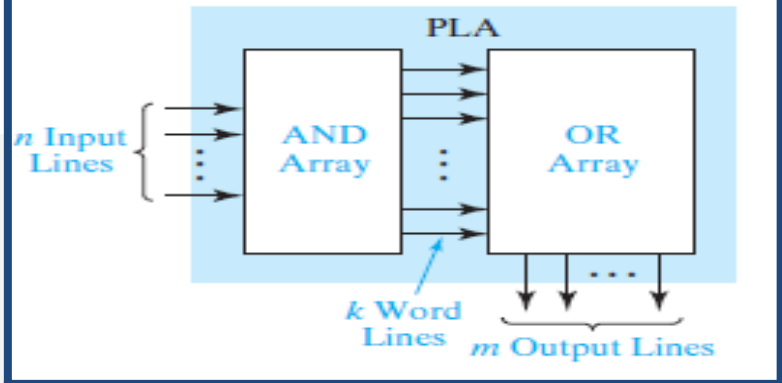
Introduction of PLD

Programmable Array Logic: The PAL (programmable array logic) is a special case of the programmable logic array in which the AND array is programmable and the OR array is fixed.

The basic structure of the PAL is the same as the PLA because only the AND array is programmable, the PAL is less expensive than the more general PLA, and the PAL is easier to program. For this reason, logic designers frequently use PALs to replace individual logic gates when several logic functions must be realized. The symbol represents an input buffer which is logically equivalent to A buffer is used because each PAL input must drive many AND gate inputs.



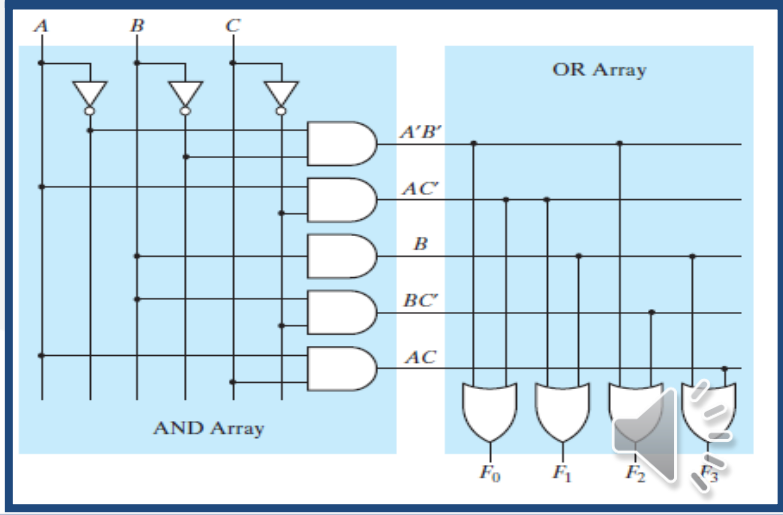
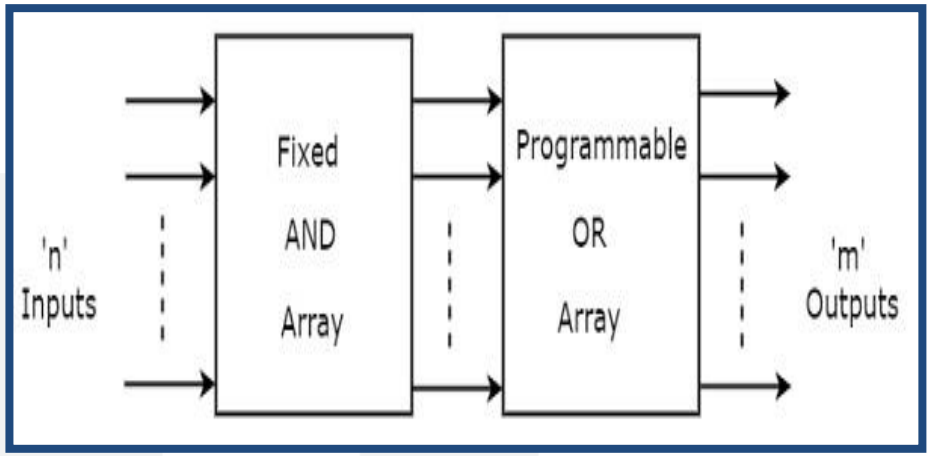


Image source Google

ROM as a PLD

Read Only Memory ROM is a memory device, which stores the binary information permanently. That means, we can't change that stored information by any means later. If the ROM has programmable feature, then it is called as Programmable ROM PROM.

The user has the flexibility to program the binary information electrically once by using PROM programmer. PROM is a programmable logic device that has fixed AND array & Programmable OR array. The block diagram of PROM is shown in the following figure.



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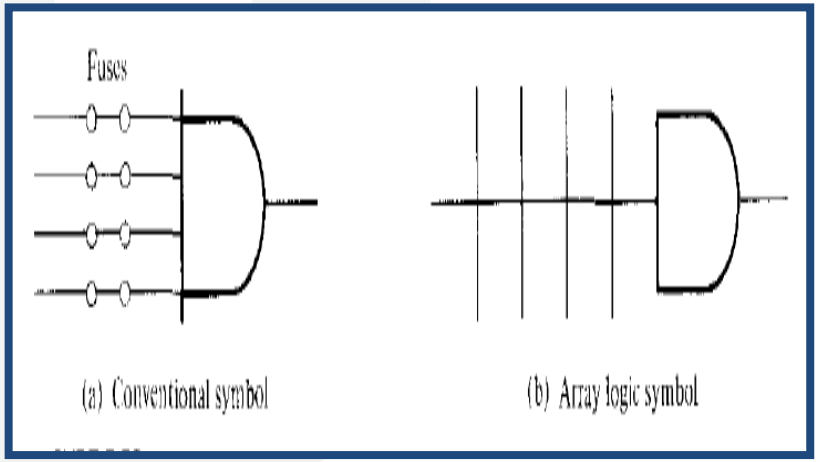
Programmable array logic

Programmable logic devices have hundreds of gates interconnected through hundreds of electronic fuses. It is sometimes convenient to draw the internal logic of such devices in a compact form referred to as array logic. The conventional symbol is drawn with multiple lines showing the fuses connected to the inputs of the gate.

Each input has a buffer and an inverter gate. Note that the two gates are shown with one composite graphic symbol with normal and complement outputs. There are four sections in the unit, each being composed of a three wide AND-OR array.



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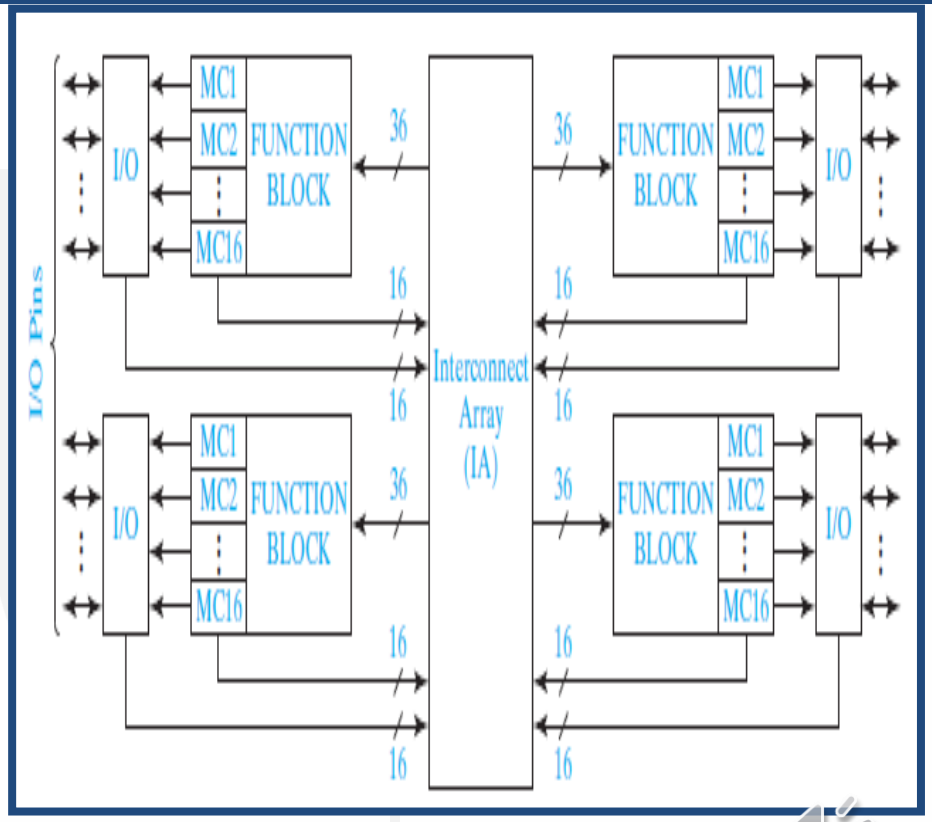
Complex Programmable logic devices (CPLDS)

Integrated circuit technology continues to improve, more and more gates can be placed on a single chip. This has allowed the development of complex programmable logic devices (CPLDs). Instead of a single PAL or PLA on a chip, many PALs or PLAs can be placed on a single CPLD chip and interconnected. When storage elements such as flip-flops are also included on the same IC. A small digital system can be implemented with a single CPLD.



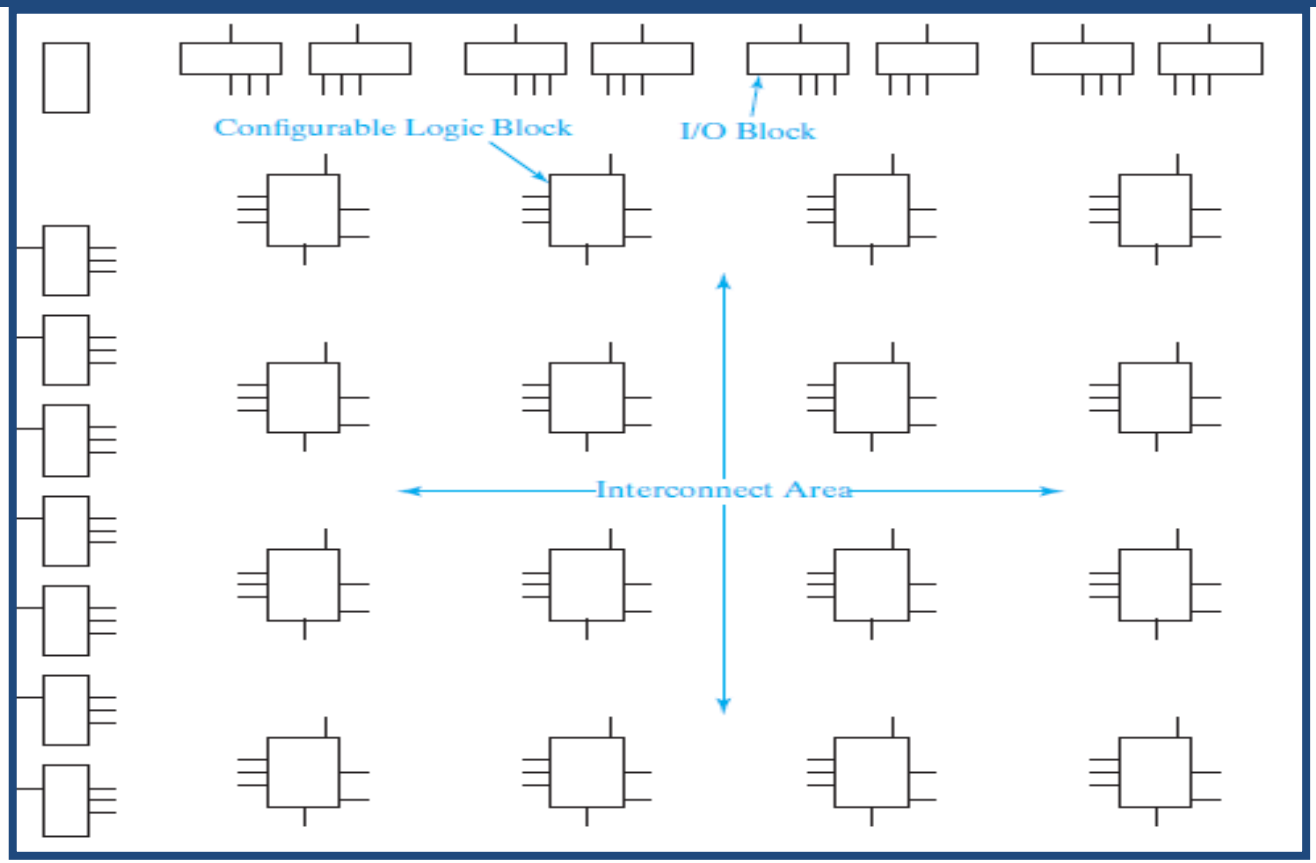
Field Programmable Gate Array (FPGA)

The use of field-programmable gate arrays (FPGAs) in combinational logic design. An FPGA is an IC that contains an array of identical logic cells with programmable interconnections. The user can program the functions realized by each logic cell and the connections between the cells.

The interior of the FPGA consists of an array of logic cells, also called configurable logic blocks (CLBs). The array of CLBs is surrounded by a ring of input-output interface blocks. These I/O blocks connect the CLB signals to IC pins. The space between the CLBs is used to route connections between the CLB outputs and inputs.

This CLB contains two function generators, two flip-flops, and various multiplexers for routing signals within the CLB. Each function generator has four inputs and can implement any function of up to four variables. The function generators are implemented as lookup tables (LUTs).

Field Programmable Gate Array (FPGA)



Layout of a Typical FPGA

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