

# Fast and simple space vector modulation method for multilevel converters

ISSN 1755-4535

Received on 26th February 2019

Revised 11th September 2019

Accepted on 2nd October 2019

E-First on 4th November 2019

doi: 10.1049/iet-pel.2019.0264

www.ietdl.org

 Haitao Zhang<sup>1</sup> ✉, Yongqing Meng<sup>1</sup>, Lianhui Ning<sup>1</sup>, Yichao Zou<sup>1</sup>, Xiuli Wang<sup>1</sup>, Xifan Wang<sup>1</sup>
<sup>1</sup>School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, Shaanxi, People's Republic of China

✉ E-mail: htzhangee@gmail.com

**Abstract:** This study proposes a simplified space vector pulse-width modulation (SVPWM) method for multilevel converters. To avoid unnecessary coordination transformations, firstly, a further derivation is conducted on the basis of the 60° coordinate transformation. Then, all the nearest three vectors (NTVs), duty cycles and optimal switching sequence within one switching period can be identified through a simple comparison of three-phase modulation waves. To further reduce the switching frequency, detailed steps to achieve the minimum number of transitions among different NTVs are constructed. Combined with the optimal switching sequence within one switching period, the minimum number of transitions within a fundamental period can be achieved easily. Finally, a thorough discussion is conducted to simplify the procedure further and the flowchart for the proposed SVPWM is also presented. Compared with the previous methods, the proposed method does not require any iterative calculation or coordinate transformation. To the best of the authors' knowledge, the calculation amount is reduced by almost seven times compared with the methods proposed. In addition, the switching frequency and total harmonic distortions remain at the same level without any deterioration. Finally, the simulation and experiment for modular multilevel converter are performed to verify the correctness and efficiency of the proposed method.

## 1 Introduction

Since the introduction of multilevel converter topologies, including neutral point-clamped (NPC) inverter [1, 2], flying capacitor inverter [3] and modular multilevel converter (MMC) [4, 5], they have been applied to many areas successfully such as wind turbine, motor driving and direct-current (DC) distribution system due to their numerous advantages such as lower harmonic, lower voltage stress, high power quality and common voltage. Compared with high voltage direct current transmission system, the voltage level for wind turbine, motor driving and DC distribution system is relatively low such that the nearest level modulation is not applicable. Instead, the pulse-width modulation (PWM) proves to be more suitable for medium/low-voltage multilevel converters.

As for PWM, two major modulation strategies, sinusoidal pulse-width modulation (SPWM) and space vector pulse-width modulation (SVPWM), have their own merits and demerits, respectively [6]. Based on the voltage-second balance, SPWM can achieve the desired voltage with a simple comparison between the sinusoidal modulation signal and the triangle carrier signal. Compared to SPWM, the SVPWM features more degrees of freedom, better harmonic performance and higher DC voltage utilisation, hence it is preferred in many cases such as fault-tolerant operation [7, 8], over-modulation operation [9] and capacitor voltage balancing [10–12]. However, due to the existence of redundant space vectors and switching sequences, its implementation procedure is rather complex, especially for multilevel converters. For the purpose of simplifying this procedure, various methods have been put forward [13–30].

The SPWM equivalence method [13–17] uses SPWM to achieve SVPWM by adding a common mode voltage to the modulation waves. However, for different modulation modes (including continuous and discontinuous modulation) and different switching sequences, the different common mode voltages are required. In addition, for some special demand such as capacitor voltage balancing under various conditions, the corresponding common mode voltages are hard to deduce. The hexagons division method [18–20] divides the high-level number space vector diagram (SVD) into low-level number SVD, and then implements the SVPWM for high-level number with the help of SVPWM for

low-level number. Although this method possesses all the freedoms of the conventional SVPWM methods, it requires look-up tables and costs more storage space. What is more, the storage space and computational time will increase apparently with the level number of converters, making it is unsuitable for converters with hundreds of level number. To reduce the requirement for storage space and speed up computation, a coordinate transformation-based method is proposed in 60° and 90° coordinates, respectively [21–25]. Different from the previous methods, the coordinate transformation-based method can locate the nearest three vectors (NTVs) quickly through one coordinate transformation and inverse coordinate transformation. What is more, the calculation burden is relatively small and remains unchanged regardless of the level number of converters and modulation index, which is meaningful and very important and widely used in [26, 29, 30].

Apart from the NTVs detection, the optimal switching sequence to achieve the minimum switching frequency, including the optimal switching sequence within one switching period and the transitions among different NTVs, is another important aspect. To acquire the optimal switching sequence within one switching period, a method called minimum change detector (MCD) is proposed in [25]. However, as MCD needs to calculate the difference between the old vector and all the available redundant new vectors to determine the next vector every segment, the computation burden is relatively large and increases with the number of redundant vectors. To resolve this problem, another 90° coordinate transformation is introduced in [28], decreasing the complexity and calculation amount to some extent. While coordinate transformation can simplify the whole procedure of SVPWM of multilevel converters and retains the computation burden at a low level regardless of the level number of converters, the procedure to realise the minimum transitions among different NTVs still needs further study.

In addition to the methods above, Dekka *et al.* [31] use modulation signals in the *abc*-axis to implement SVPWM. However, it does not give mathematical proof and detailed steps to achieve the minimum switching frequency. Bai *et al.* [27] mimic the sampling mode of carrier phase-shifted SPWM to achieve SVPWM. To be more specific, it regroups the whole system into numerous two-level submodules, samples the modulation signals for submodules evenly in one sampling period and applies the two-

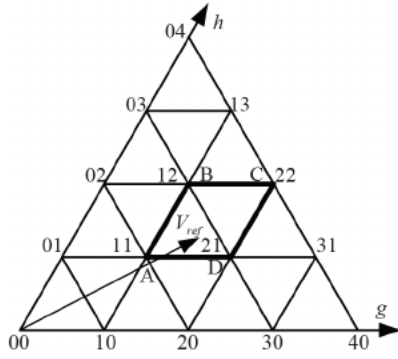


Fig. 1 Sixty-degree SVD

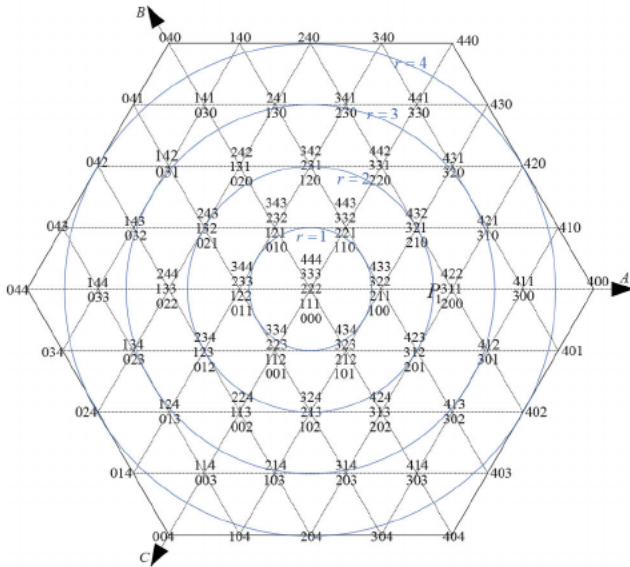


Fig. 2 Five-level SVD

level SVPWM to each submodule. Moreover, a generalised method is proposed in [32] to make full use of all the degrees of freedom at the cost of complex calculations.

For the purpose of implementing the multilevel SVPWM explicitly and reducing the calculation, with the aid of 60° coordinate transformation, a simple but efficient method requiring neither coordinate transformation nor iterative calculation is proposed. With a simple comparison of three-phase modulation waves, all the NTVs, duty cycle calculation and the optimal switching sequence can be obtained efficiently. What is more, based on the principles [33, 34] for better harmonic profile and minimum transition numbers, a novel strategy to achieve the minimum number of transitions among different NTVs is introduced. To illustrate the method clearly, a brief review of 60° coordinate transformation and SVD properties is given in Section 2. Then the detailed derivation procedure for NTVs and duty cycle is presented and the NTVs and duty cycles for different conditions are listed in Section 3. The strategy to achieve the minimum number of transitions among different NTVs (namely, the identification of the initial space vector) and the rule of the optimal switching sequence determination are put forward in Section 4. A further discussion and explanation are given in Section 5. For verifying the correctness and effectiveness of the proposed method, simulations and comparisons are presented in Section 5. At the end of this paper, the conclusion is drawn and future work is discussed.

## 2 Review of 60° coordinate transformation method and SVD properties

### 2.1 Sixty-degree coordinate transformation and reference vector location

The reference vector location in SVPWM is equivalent to the identification of the NTVs. According to Piao and Hung [14], the

degree coordinate can be transformed to 60° coordinate by (1) and (2):

$$V_i = N \cdot m_i \quad (i = a, b, c) \quad (1)$$

$$\begin{bmatrix} V_g \\ V_h \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2)$$

where  $m_i (i = a, b, c)$ ,  $N$ ,  $V_i (i = a, b, c)$  and  $V_j (j = g, h)$  are three-phase modulation waves, level number of converters, phase voltage in 120° and 60° coordinates, respectively. Taking the five-level converter, for example, part of 60° coordinates is depicted in Fig. 1.

If the reference vector lies as shown above, then the NTVs can be identified by (3) and (4):

$$\begin{aligned} V_A &= [\text{int}(V_g), \text{int}(V_h)]^T \\ V_B &= [\text{int}(V_g), \text{int}(V_h) + 1]^T \\ V_C &= [\text{int}(V_g) + 1, \text{int}(V_h) + 1]^T \\ V_D &= [\text{int}(V_g) + 1, \text{int}(V_h)]^T \end{aligned} \quad (3)$$

$$V_{\text{ref}} \in \begin{cases} \Delta ABD & \text{if } (V_g + V_h) \leq (\text{int}(V_g) + \text{int}(V_h) + 1) \\ \Delta CBD & \text{if } (V_g + V_h) \geq (\text{int}(V_g) + \text{int}(V_h) + 1) \end{cases} \quad (4)$$

where  $\text{int}(x)$  is a function that returns the largest integer no bigger than  $x$ . Supposing that the modulation triangle has been identified, and then space vectors can be retransformed from 60° coordinate to 120° coordinate by (5) as noted in [14]:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 0 & 1 & 1 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_g \\ V_h \\ k \end{bmatrix} \quad (5)$$

where  $k$  is a free variable and an integer, guaranteeing all the space vectors are in the range of  $[0, N]$ . In other words,  $0 \leq V_a, V_b, V_c \leq N$  always holds.

Although the coordinate transformation method is simple and explicit, two coordinate transformations are inevitable in each switching period. What is more, the optimal switching sequence to achieve the minimum number of transitions within a fundamental period requires additional calculations [25, 28], which increases the computation amount apparently.

### 2.2 SVD properties

Taking the five-level SVD as an example. As shown in Fig. 2, the multilevel SVD is divided by the blue circles evenly and space vectors are listed decreasingly from top to bottom.

As we can see, the biggest element of the smallest space vector for each vertex is decided by where the vertex lies and vice versa. For example, vertex  $P_1$  lies within the blue circles  $r = 2$  and  $r = 3$ , then the smallest space vector corresponding to vertex  $P_1$  are  $[2, 0, 0]$  and the biggest element of  $[2, 0, 0]$  is 2. Conversely, if the biggest elements of the smallest space vector for one vertex are 2, then it is surely that this vertex lies within the blue circles  $r = 2$  and  $r = 3$ . This conclusion is useful for locating the vertex through its corresponding space vector.

## 3 NTVs determination and duty cycle calculation

In order to reduce the number of unnecessary coordinate transformation, substituting (2) into (3) and replacing  $V_g$  and  $V_h$  with  $V_a, V_b$ , and  $V_c$ , (3) can be rewritten as

$$\begin{aligned}
V_A &= [\text{int}(V_a - V_b), \text{int}(V_b - V_c)]^T \\
V_B &= [\text{int}(V_a - V_b), \text{int}(V_b - V_c) + 1]^T \\
V_C &= [\text{int}(V_a - V_b) + 1, \text{int}(V_b - V_c) + 1]^T \\
V_D &= [\text{int}(V_a - V_b) + 1, \text{int}(V_b - V_c)]^T
\end{aligned} \quad (6)$$

Subsequently, transferring the space vectors in  $60^\circ$  coordinates expressed in (6) to  $120^\circ$  coordinates with (5) and setting  $k$  as  $\text{int}(V_c)$ , (6) can be further expressed by

$$\begin{aligned}
V_A &= \begin{bmatrix} \text{int}(V_a - V_b) + \text{int}(V_b - V_c) + \text{int}(V_c) \\ \text{int}(V_b - V_c) + \text{int}(V_c) \\ \text{int}(V_c) \end{bmatrix} \\
V_B &= \begin{bmatrix} \text{int}(V_a - V_b) + \text{int}(V_b - V_c) + \text{int}(V_c) + 1 \\ \text{int}(V_b - V_c) + \text{int}(V_c) + 1 \\ \text{int}(V_c) \end{bmatrix} \\
V_C &= \begin{bmatrix} \text{int}(V_a - V_b) + \text{int}(V_b - V_c) + \text{int}(V_c) + 2 \\ \text{int}(V_b - V_c) + \text{int}(V_c) + 1 \\ \text{int}(V_c) \end{bmatrix} \\
V_D &= \begin{bmatrix} \text{int}(V_a - V_b) + \text{int}(V_b - V_c) + \text{int}(V_c) + 1 \\ \text{int}(V_b - V_c) + \text{int}(V_c) \\ \text{int}(V_c) \end{bmatrix}
\end{aligned} \quad (7)$$

Similarly, substituting (2) into (4) and replacing  $V_g$  and  $V_h$  with  $V_a$ ,  $V_b$ , and  $V_c$  (4) can be expressed in  $120^\circ$  coordinate as

$$V_{\text{ref}} \in \begin{cases} \Delta ABD & \text{if } (V_a - V_c) \leq (\text{int}(V_a - V_b) + \text{int}(V_b - V_c) + 1) \\ \Delta CBD & \text{if } (V_a - V_c) \geq (\text{int}(V_a - V_b) + \text{int}(V_b - V_c) + 1) \end{cases} \quad (8)$$

Since the function  $\text{int}(x)$  has properties as (9), the final results of (7) and (8) depend on the relative size of  $V_i - \text{int}(V_i)$  ( $i = a, b, c$ ):

$$\text{int}(x_1 - x_2) = \begin{cases} \text{int}(x_1) - \text{int}(x_2) & \text{if } x_1 - \text{int}(x_1) \geq x_2 - \text{int}(x_2) \\ \text{int}(x_1) - \text{int}(x_2) - 1 & \text{if } x_1 - \text{int}(x_1) < x_2 - \text{int}(x_2) \end{cases} \quad (9)$$

Without loss of generality, one condition as (10) is discussed here in detail and the other conditions can be done similarly:

$$V_b - \text{int}(V_b) > V_a - \text{int}(V_a) > V_c - \text{int}(V_c) \quad (10)$$

As (10) holds, then (7) and the right part of (8) can be further simplified as (11) and (12):

$$\begin{aligned}
V_A &= [\text{int}(V_a) - 1, \text{int}(V_b), \text{int}(V_c)]^T \\
V_B &= [\text{int}(V_a), \text{int}(V_b) + 1, \text{int}(V_c)]^T \\
V_C &= [\text{int}(V_a) + 1, \text{int}(V_b) + 1, \text{int}(V_c)]^T \\
V_D &= [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T
\end{aligned} \quad (11)$$

$$\text{int}(V_a - V_b) + \text{int}(V_b - V_c) + 1 = \text{int}(V_a) - \text{int}(V_c) \quad (12)$$

Having

$$V_a - \text{int}(V_a) > V_c - \text{int}(V_c)$$

then

$$V_a - V_c > \text{int}(V_a) - \text{int}(V_c)$$

this means

$$V_a - V_c > \text{int}(V_a - V_b) - \text{int}(V_b - V_c) + 1 \quad (13)$$

Combining (8), (11) and (13), the NTVs are selected as (14):

$$\begin{aligned}
V_B &= [\text{int}(V_a), \text{int}(V_b) + 1, \text{int}(V_c)]^T \\
V_C &= [\text{int}(V_a) + 1, \text{int}(V_b) + 1, \text{int}(V_c)]^T \\
V_D &= [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T
\end{aligned} \quad (14)$$

All the available redundant space vectors can be generated as (15). As redundant space vector selection is not the focus of this paper, we will not discuss this topic in detail here:

$$\begin{aligned}
V_B &= [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T + r[1, 1, 1]^T \\
V_C &= [\text{int}(V_a), \text{int}(V_b) + 1, \text{int}(V_c)]^T + s[1, 1, 1]^T \\
V_D &= [\text{int}(V_a) + 1, \text{int}(V_b) + 1, \text{int}(V_c)]^T + t[1, 1, 1]^T \\
r, s, t &\in \mathbf{Z}, 0 \leq V_{kj} \quad (i = B, C, D; j = 1, 2, 3) \leq N
\end{aligned} \quad (15)$$

The duty cycle for each space vector can be deduced by solving (16) and (17):

$$V_B D_B + V_C D_C + V_D D_D = V_{\text{ref}} \quad (16)$$

$$D_B + D_C + D_D = 1 \quad (17)$$

If new variables are defined as

$$\begin{aligned}
V'_a &= V_a - \text{int}(V_a) \\
V'_b &= V_b - \text{int}(V_b) \\
V'_c &= V_c - \text{int}(V_c)
\end{aligned} \quad (18)$$

substituting space vectors in (15) into (16) and solving (16) and (17), then the duty cycles for each space vector can be expressed by (19):

$$\begin{aligned}
D_B &= 1 - D_C - D_D \\
D_C &= V'_b - V'_a \\
D_D &= V'_a - V'_c
\end{aligned} \quad (19)$$

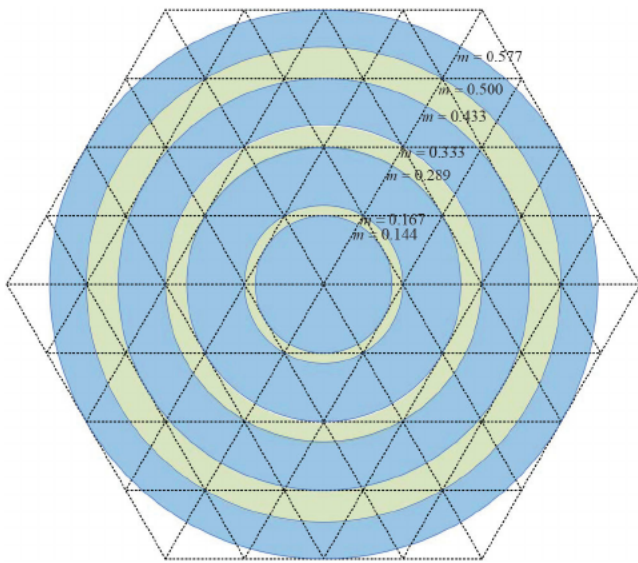
If we set  $[\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T$  as  $V_1$  and arrange the nearest three space vectors increasingly from top to bottom, then all the NTVs and duty cycles for different conditions can be listed as Table 1. From Table 1 we know that the NTVs for different conditions all include space vector  $V_1$ . Besides, the optimal switching sequence to achieve the minimum number of transitions within one switching period can also be determined at the same time when the NTVs are identified. Actually, the relative size of  $V'_i$  ( $i = a, b, c$ ) can not only determine NTVs and duty cycles, but also determines the optimal switching sequence to achieve the minimum number of transitions within a switching period, which will be discussed later.

#### 4 Identification of initial space vector and optimal switching sequence

Apart from the detection of NTVs, the determination of the optimal switching sequence within one switching period and duty cycle calculation, another important thing is to identify the initial space vector for every switching sequence, which also has an influence on the final switching frequency [34]. If the minimum number of transitions within one fundamental period (or switching frequency) is set as a target, then the transitions among different modulation triangles should be minimised at the same time [34]. To minimise the switching frequency (or the number of transitions within one fundamental period), different strategies are adopted in previous literatures. However, their results are not completely identical. Taking a five-level SVD as an example, the multilevel SVD, as shown in Fig. 3, is divided by the modulation index into seven

**Table 1** NTVs and duty cycle for different conditions

Relative size among $V'_i$	$V'_a > V'_b > V'_c$	$V'_a > V'_c > V'_b$	$V'_b > V'_a > V'_c$
NTVs	$V_1 = [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T$ $V_2 = [\text{int}(V_a) + 1, \text{int}(V_b), \text{int}(V_c)]^T$ $V_3 = [\text{int}(V_a) + 1, \text{int}(V_b) + 1, \text{int}(V_c)]^T$	$V_1 = [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T$ $V_2 = [\text{int}(V_a) + 1, \text{int}(V_b), \text{int}(V_c)]^T$ $V_3 = [\text{int}(V_a) + 1, \text{int}(V_b), \text{int}(V_c) + 1]^T$	$V_1 = [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T$ $V_2 = [\text{int}(V_a), \text{int}(V_b) + 1, \text{int}(V_c)]^T$ $V_3 = [\text{int}(V_a) + 1, \text{int}(V_b) + 1, \text{int}(V_c)]^T$
duty cycle	$D_1 = 1 - D_2 - D_3$ $D_2 = V'_a - V'_b$ $D_3 = V'_b - V'_c$	$D_1 = 1 - D_2 - D_3$ $D_2 = V'_a - V'_c$ $D_3 = V'_c - V'_b$	$D_1 = 1 - D_2 - D_3$ $D_2 = V'_b - V'_a$ $D_3 = V'_a - V'_c$
relative size among $V'_i$	$V'_b > V'_c > V'_a$	$V'_c > V'_a > V'_b$	$V'_c > V'_b > V'_a$
NTVs	$V_1 = [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T$ $V_2 = [\text{int}(V_a), \text{int}(V_b) + 1, \text{int}(V_c)]^T$ $V_3 = [\text{int}(V_a), \text{int}(V_b) + 1, \text{int}(V_c) + 1]^T$	$V_1 = [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T$ $V_2 = [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c) + 1]^T$ $V_3 = [\text{int}(V_a) + 1, \text{int}(V_b), \text{int}(V_c) + 1]^T$	$V_1 = [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T$ $V_2 = [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c) + 1]^T$ $V_3 = [\text{int}(V_a), \text{int}(V_b) + 1, \text{int}(V_c) + 1]^T$
duty cycle	$D_1 = 1 - D_2 - D_3$ $D_2 = V'_b - V'_c$ $D_3 = V'_c - V'_a$	$D_1 = 1 - D_2 - D_3$ $D_2 = V'_c - V'_a$ $D_3 = V'_a - V'_b$	$D_1 = 1 - D_2 - D_3$ $D_2 = V'_c - V'_b$ $D_3 = V'_b - V'_a$

**Fig. 3** Classification of SVD by modulation index**Table 2** Rule of optimal switching sequence within a switching cycle

Initial space vector	Switching sequence
$V_0 = V_1$	$V_1 \rightarrow V_2 \rightarrow V_3$
$V_0 = V_2$	$V_2 \rightarrow V_3 \rightarrow V_1 + [1, 1, 1]$
$V_0 = V_3$	$V_3 \rightarrow V_1 + [1, 1, 1] \rightarrow V_2 + [1, 1, 1]$

parts marked in yellow and blue. If the modulation circle is in the blue modulation area, then the results from the methods used in [28, 32] are identical. However, if the modulation circle lies within the yellow modulation area, then the method in [28] will bring in extra transitions and increase the switching frequency to some extent. All of those things will be verified in Section 6 later.

According to the analysis in [34], to achieve the minimum number of transitions among different modulation triangles, the space vectors, whose vertex lies within the area where the reference vector (or the modulation circle) locates, should be selected as the initial space vector. Combining with the SVD properties described in Section 2, the detailed steps to select the initial space vector are constructed as follows.

Supposing the modulation index and NTVs are  $m$  and  $V_b$ ,  $V_2$  and  $V_3$  respectively, then the initial space vector can be selected through the following steps:

(i) Normalising the space vector  $V_i$  ( $i = 1, 2, 3$ ) through (20):

$$V_i = V_i - \min(V_i(1), V_i(2), V_i(3)) \cdot [1, 1, 1]^T \quad (i = 1, 2, 3) \quad (20)$$

where  $\min(V_i(j))$  ( $i, j = 1, 2, 3$ ) returns the smallest element of the space vector  $V_i$  ( $i = 1, 2, 3$ ).

(ii) Selecting the space vector satisfying (21) as the potential initial space vector:

$$\text{int}(\sqrt{3} \cdot N \cdot m) = \max(V_i(1), V_i(2), V_i(3)) \quad (i = 1, 2, 3) \quad (21)$$

where  $N$  is the level number of converters and  $m$  is the modulation index.

(iii) If the number of potential initial space vectors is one, then it should be selected as the initial vector automatically. However, if there are two space vectors satisfying (19), then the space vector with a lower duty cycle should be selected as the initial space vector [34].

After the identification of the NTVs, duty cycles and the initial space vector, the optimal switching sequence within a switching period can be determined easily. With the purpose of minimising the number of transitions within every switching period and  $V_1, V_2, V_3$  defined as in Table 1, the switching sequence for different conditions and initial space vectors is listed in Table 2.

## 5 Further discussion of multilevel SVPWM

### 5.1 Further discussions of the computation time

As one of this manuscript's contributions is reducing the computation amount and time of multilevel SVPWM, here we explain how this improvement is achieved exactly from the theoretical aspect. To clarify this problem clearly, we firstly choose methods proposed in [28, 32] for comparison which are, respectively, the simplest and fastest SVPWM methods for multilevel converters by far to the best of our knowledge [28, 32].

In general, the SVPWM method for multilevel converters includes three steps: NTVs identification, duty cycle calculation and optimal switching sequence determination. Among the calculation or determination of these three parts, various operations are needed. However, the most time-consuming operation includes the coordinate transformation, trigonometric function calculation and iterative operation. To compare the calculation amount of these three methods, a summary of the time-consuming operation needed in each step of different methods is presented in Table 3, where ✓ and –, respectively, indicate whether the corresponding operation is needed or not. Taking the blue table cells as an example, the first and second ‘–’ mean that the NTVs determination of the method proposed in [32] does not need coordinate transformation and trigonometric function calculation, respectively. In contrast, the last ‘✓’ means



that the NTVs determination of the method proposed in [32] requires iterative calculation.

As shown above, the method proposed in [28, 32] requires coordinate transformation, trig-function calculation and iterative operation in different steps, resulting in a big calculation amount. In addition, due to the existence of the iterative operation, the calculation amount of [32] increases with the higher level number of converters. In contrast, the proposed method requires none of these operations, including coordination transformation, trig-function calculation and iterative operation. Therefore, the calculation amount of the proposed method is reduced apparently compared with the previous literature related and we will verify this conclusion again by experiments later.

## 5.2 Further simplification of the process of multilevel SVPWM

Although several complicated coordinate transformations are replaced by a simple comparison of  $V'_i$  ( $i = a, b, c$ ) to deduce the NTVs and switching sequence, two more maps, Tables 1 and 2, are still needed. Actually, the NTVs and switching sequence within a switching cycle can be obtained without these two maps.

As shown in Table 1, although NTVs for various conditions are different, they all have vector  $[\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T$ . According to Table 2, with  $V_1$  as initial space vector, the optimal switching sequence can be determined depending on the relative size of  $V'_i$  ( $i = a, b, c$ ). The principle can be described as follows: the bigger the  $V'_i$  ( $i = a, b, c$ ) is, the former of its corresponding phase is in the switching sequence. For example, if  $V'_a > V'_b > V'_c$ , then the corresponding switching sequence of the three phase is  $A \rightarrow B \rightarrow C$ . On the other hand, if  $V'_b > V'_c > V'_a$ , its switching sequence is  $B \rightarrow C \rightarrow A$ . Once the switching sequence has been decided, the NTVs can also be deduced. For example, if  $V'_a > V'_b > V'_c$ , then the switching sequence will be  $A \rightarrow B \rightarrow C$ . With the initial space vector as  $V_1 = [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T$ , the NTVs can be deduced as

$$\begin{aligned} V_1 &= [\text{int}(V_a), \text{int}(V_b), \text{int}(V_c)]^T \\ V_2 &= [\text{int}(V_a) + 1, \text{int}(V_b), \text{int}(V_c)]^T \\ V_3 &= [\text{int}(V_a) + 1, \text{int}(V_b) + 1, \text{int}(V_c)]^T \end{aligned}$$

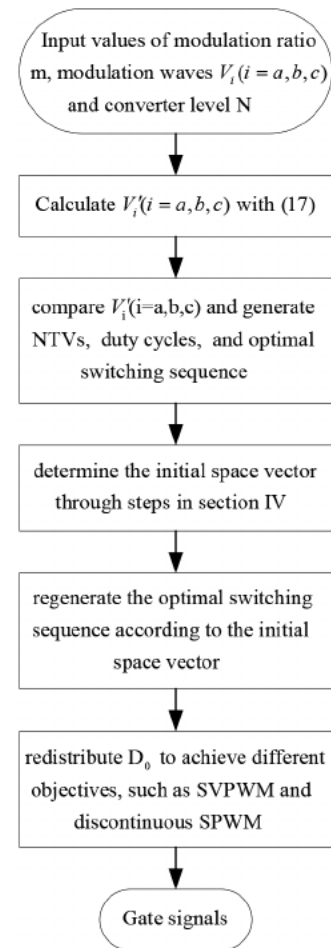
Then, with duty cycles calculated by (17) and initial space vector identified through the steps in Section 4, the actual switching sequence can be revised according to the initial space vector and the actual gate signals can be generated. In fact, through the distribution of the duty cycle for the initial space vector, various modulation strategies, such as continuous and discontinuous SPWM and SVPWM, can be obtained easily. As this procedure is simple and can be found in related books, it is omitted here. The flowchart for the proposed method is presented in Fig. 4, where  $D_0$  represents the corresponding duty cycle of the initial space vector.

## 6 Simulation and experimental results

In this section, MMC is taken as an example to verify the correctness and efficiency of the proposed method. For the sake of fairness, only the method that can achieve all the objectives can be selected as the comparison objects. These objectives include locating the NTVs, calculating the duty cycles, determining the optimal switching sequence within one switching period, selecting the initial space vector for every switching sequence, generating all the available switching states and fully using the degrees of freedom. As a result, the methods proposed in [28, 32] are used here as the comparison objects due to the reasons noted in Section 1. Since the DC voltage balancing strategy is not the focus of this paper and can be implemented on the base of the results of this paper, to further eliminate interference, capacitors are replaced by ideal DC-voltage source, which is a common practice used in [28, 32]. Further, the level number of converters and modulation index are labelled as  $N$  and  $m$ , respectively.

**Table 3** Time-consuming operation required in each step of different methods

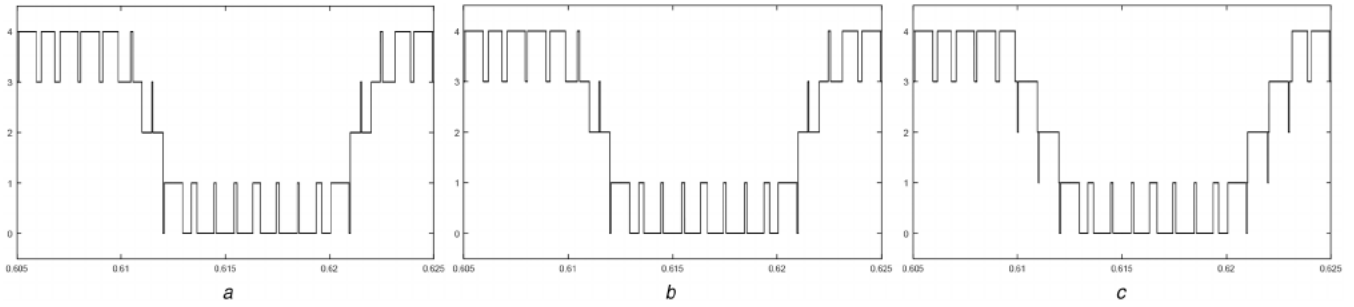
Steps in SVPWM method	Coordinate transformation	Trig-function calculation	Iterative operation
NTVs determination in this paper	—	—	—
NTVs determination in [32]	—	—	✓
NTVs determination in [28]	✓	—	—
duty-cycle calculation in this paper	—	—	—
duty-cycle calculation in [32]	—	✓	—
duty-cycle calculation in [28]	—	✓	—
switching sequence in this paper	—	—	—
switching sequence in [32]	—	—	—
switching sequence in [28]	✓	—	—



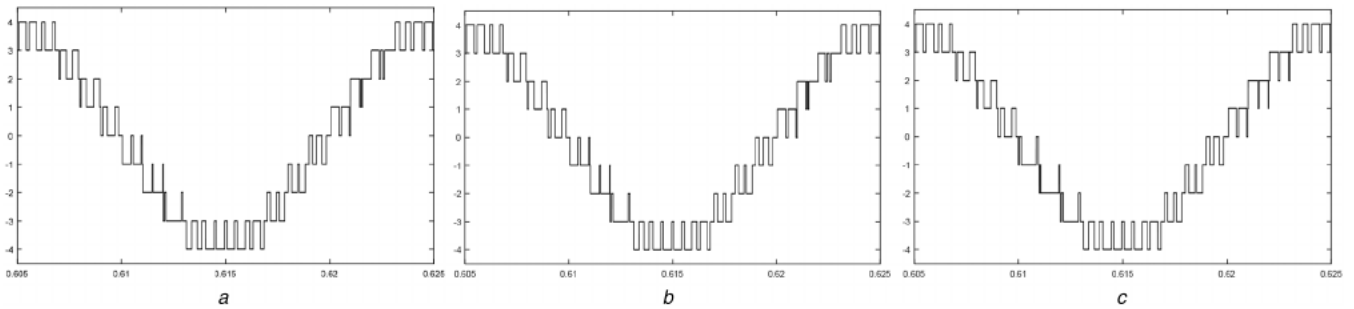
**Fig. 4** Flowchart for the proposed SVPWM method

### 6.1 Output phase-voltage and line-to-line voltage

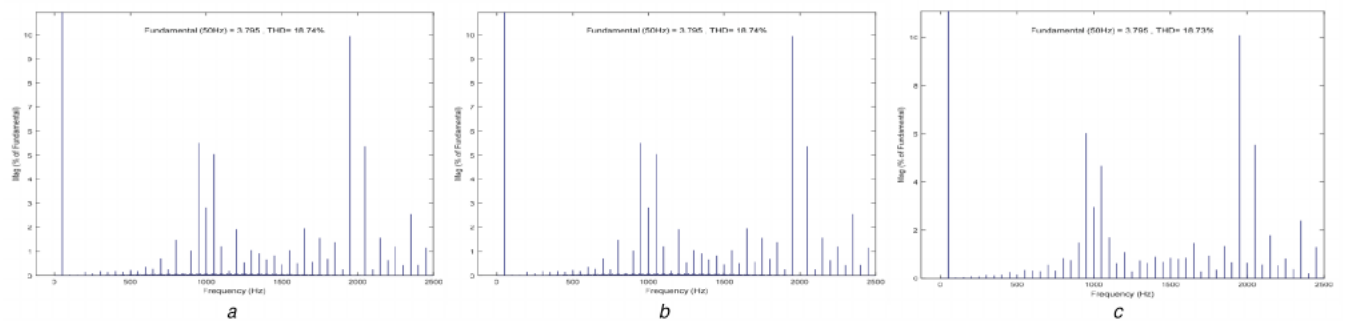
Setting  $N = 5$  and  $m = 0.55$ , Figs. 5a–c show the output voltages of phase-A upper arm obtained by the methods proposed in this paper and in [28, 32], respectively. As we can see, Figs. 5a and b are completely identical in every switching period. In other words, the NTVs determination, duty cycle distribution and switching sequence generation in every switching period are always consistent for the methods proposed in this paper and in [32], verifying the correctness of the proposed simplified method.



**Fig. 5** Upper arm output voltage waveforms of different SVPWM methods  
(a) Method in this paper, (b) Method in [32], (c) Method in [28]



**Fig. 6** Output line voltage waveforms of different SVPWM methods  
(a) Method in this paper, (b) Method in [32], (c) Method in [28]



**Fig. 7** THD analysis results of output line voltages of different methods  
(a) THDs of the line voltage in Figs. 6a, (b) THDs of the line voltage in Fig. 6b, (c) THDs of the line voltage in Fig. 6c

**Table 4** THD of output line voltage for different methods and modulation index

Modulation method, THD, %	Proposed method	Method in [32]	Method in [28]
$m = 0.55$	18.74	18.74	18.73
$m = 0.45$	20.66	20.66	20.64
$m = 0.35$	26.08	26.08	26.01
$m = 0.30$	27.27	27.27	27.23
$m = 0.25$	37.24	37.24	37.23
$m = 0.20$	43.21	43.21	43.15
$m = 0.15$	50.74	50.74	50.71

Fig. 5c is a little different from the output voltages shown in Figs. 5a and b during part of the switching periods, which is caused by their different selection strategies of the initial space vector in every switching period for different conditions. However, the NTVs determination and duty cycle distribution in every switching period for these three methods are always identical. The different selection of the initial space vector in every switching period will also influence the switching frequency and harmonic content and distribution, which will be analysed later. Fig. 6 demonstrates the corresponding output line voltages. Similarly, Figs. 6a and b are always the same while the line voltage shown in Fig. 6c is little different.

## 6.2 Comparison of THDs and switching frequency of different modulation indices and different methods

To evaluate the harmonic performance of the output voltages obtained from the proposed method and from [28, 32], the THDs of the line voltages shown in Fig. 6 are measured through the 'Powergui FFT Analysis Tool' in Matlab/Simulink. To eliminate the random error, the output line voltage of several fundamental periods is analysed through 'Powergui FFT Analysis Tool' to measure the THD. The corresponding Fourier analysis results are presented in Fig. 7 and the weighted harmonics with respect to the fundamental content is described by histograms. With respect to Figs. 7a–c, their fundamental contents are all equal. In addition, the harmonic distribution is almost identical both at the high- and low-frequency ranges and harmonic contents are almost identical with a difference  $<0.1\%$ , which is caused by the selection of the initial space vector. It is worth to note that although the initial space vector selection strategy used in [28] can reduce the THDs to some extent, it will also increase the switching frequency in some conditions.

Apart from the Fourier analysis demonstrated in Fig. 7, the THDs of output line voltage for different modulation index obtained from three different methods are presented in Table 4. As can be seen, the THDs for the method proposed and method in [32] are completely identical. In contrast, the THDs for the method proposed and the method in [28] are almost identical with difference  $<0.1\%$ .

**Table 5** Switching frequency of one arm for different methods and modulation index

Modulation method, Hz	Proposed method	Method in [32]	Method in [28]
$m = 0.55$	1150	1150	1150
$m = 0.45$	1150	1150	1200
$m = 0.35$	1100	1100	1100
$m = 0.30$	1100	1100	1150
$m = 0.25$	1050	1050	1050
$m = 0.20$	1050	1050	1050
$m = 0.15$	1050	1050	1100

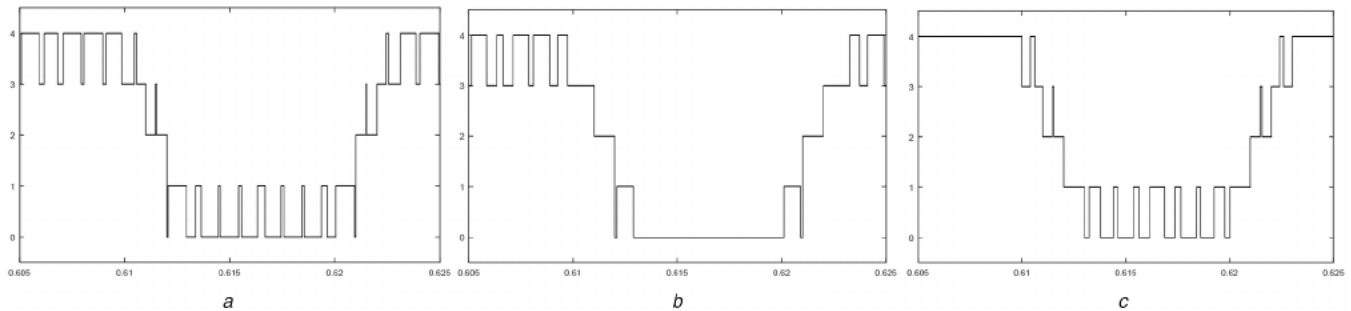
**Fig. 8** Output voltage waveforms of SVPWM and DSPWM methods  
(a) SVPWM, (b) DSPWM1, (c) DSPWM2**a****b****Fig. 9** Photograph of the experimental system and device  
(a) AppSIM, (b) TMS320F28335

Table 5 shows the comparison of switching frequency of one arm for different modulation indices using different methods.

The switching frequency is counted by the 'Counter block' in Matlab/Simulink library. To be more specific, the number of rising edges of the output voltage of arms in 1 s is counted through the 'Counter block' to measure the switching frequency. When the modulation circle lies in the modulation area marked in blue shown in Fig. 3, the switching frequency obtained from three different methods is identical. In contrast, when the modulation circle lies in the modulation area marked in yellow, the switching frequency

obtained from the method in [28] is a little higher than the switching frequency obtained from the method proposed in this paper and in [32] as noted in Section 6. In other words, the initial space vector selection strategy used in [28] cannot guarantee the minimum switching frequency all the time.

Tables 4 and 5 here validate the conclusion that the proposed SVPWM method for multilevel converter can efficiently simplify the procedure without any deterioration of THD and switching frequency, and even some improvement in some conditions.

### 6.3 Implementation of discontinuous SPWM

Compared to the continuous SPWM, the discontinuous SPWM is another important modulation strategy due to its reduced switching frequency and unchanged output line-voltage waves. With the duty cycle deduced in (17) and Table 1, proper distribution of  $D_0$  can result in two discontinuous SPMWs shown in Figs. 8b and c. For comparison, Fig. 8a shows the output voltage waves of continuous SPWM. As we can see, the discontinuous SPWM1 and SPWM2 can both reduce one transition for one phase per switching period and decrease the switching frequency apparently while keeping the output line-voltage unchanged.

### 6.4 Experimental results

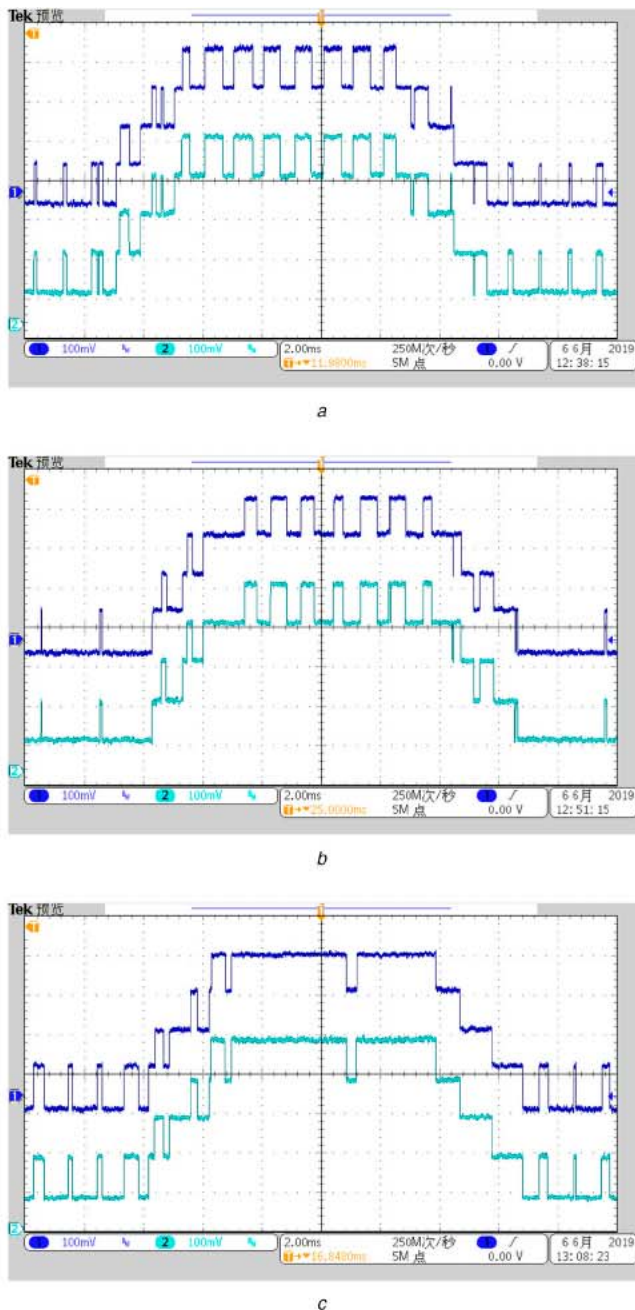
To verify the correctness and efficiency of the proposed SVPWM method, experiments are conducted through the in-loop simulation platform AppSIM shown in Fig. 9a and 32-bit floating-point Digital Signal Processor (DSP)-TMS320F28335 shown in Fig. 9b.

To verify the correctness of the proposed method, the output waveforms of the proposed method and the method proposed in [32] are compared in Fig. 10. Figs. 10a–c demonstrate the output voltage waveforms of SVPWM, discontinuous SPWM1 (DSPWM1) and DSPWM2, respectively. The upper one is obtained from the proposed method while the lower one is gained from the method proposed in [32]. As we can see, the output waveforms obtained from these two methods are completely identical, which verify the correctness of the proposed method. In addition, compared SVPWM, DSPWM1 and DSPWM2 can reduce one transition for one phase per switching period and thus further reduce the switching frequency obviously.

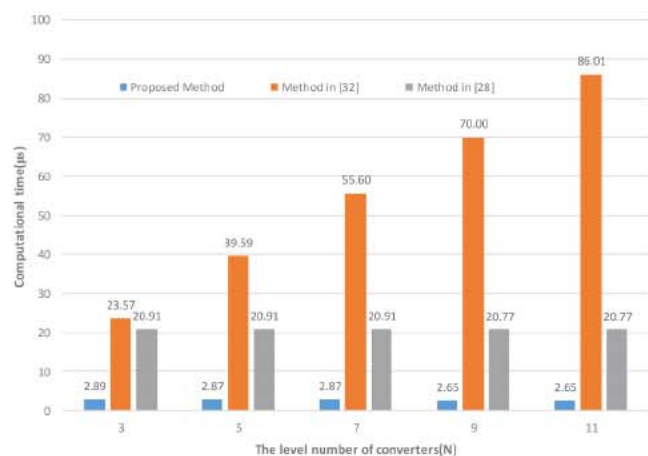
### 6.5 Comparison of real-time implementation

The computation times for three methods, the proposed method in this paper and the method in [28, 32], are compared in Fig. 11 with





**Fig. 10** Experimental results of the output voltage waveforms  
(a) SVPWM, (b) DSPWM1, (c) DSPWM2



**Fig. 11** Computational time for different modulation methods

$m = 0.55$ . It is worth to note that all the computation times in Fig. 11 only contain the time to complete the algorithm calculation, including locating the NTVs, calculating the duty cycles and determining the optimal switching sequence. The time to write on General Purpose Input/Output (GPIO) and generate actual pulse is not included here. In addition, the whole computation process does not use the function library provided by the DSP.

As we can see, the computation time for the proposed method is about  $2.86 \mu\text{s}$ . Especially, it remains nearly unchanged regardless of the level number of converters. In contrast, the computation time for three-level converter with the method in [28] is about  $20.91 \mu\text{s}$ . The computation time for the three-level converter with the method in [32] is about  $23.5 \mu\text{s}$  and the time increases with the increase of level number of converters. From the result of the comparison we can see that the computation time is reduced by almost seven times at least. All in all, the proposed method reduces the computation time and increases the efficiency apparently.

## 7 Conclusion

This paper proposes an efficient and simple SVPWM method for multilevel converters. On the basis of  $60^\circ$  coordinate transformation, the proposed method can locate the NTVs, calculate duty cycles and determine the optimal switching sequence by only one simple comparison of three-phase modulation waves while requiring no coordinate transformation or iterative computation. What is more, the proposed method is applicable to all multilevel converters regardless of the concrete topologies and the calculation amount is independent of the level number of converters. Simulation and experimental results show that the proposed method is capable of generating all the available switching states and switching sequence without loss of any degrees of freedom. The optimal switching sequence within one switching period and proposed steps to guide the transitions among different NTVs can also be used to achieve the minimum number of transitions within a fundamental period. Moreover, compared with the existing method [28, 32], the proposed method can speed up the procedure at least seven times, increasing the efficiency apparently.

## 8 References

- [1] Nabae, A., Takahashi, I., Akagi, H.: 'A new neutral-point-clamped PWM inverter', *IEEE Trans. Ind. Appl.*, 1981, **1A-17**, pp. 518–523
- [2] Dekka, A., Narimani, M.: 'Capacitor voltage balancing and current control of a five-level nested neutral-point-clamped converter', *IEEE Trans. Power Electron.*, 2018, **33**, pp. 10169–10177
- [3] Arazm, S., Vahedi, H., Al-Haddad, K.: 'Space vector modulation technique on single phase sensor-less PUC5 inverter and voltage balancing at flying capacitor'. IECON 2018 – 44th Annual Conf. of the IEEE Industrial Electronics Society, Washington, DC, USA, 2018, pp. 4504–4509
- [4] Hagiwara, M., Akagi, H.: 'Control and experiment of pulse width-modulated modular multilevel converters', *IEEE Trans. Power Electron.*, 2009, **24**, pp. 1737–1746
- [5] Lin, H., Zhu, L., Yin, T., *et al.*: 'An optimal-path SVPWM algorithm with mutual DC voltages balancing capacity for three-module cascaded multilevel converter'. 2018 IEEE Int. Power Electronics and Application Conf. and Exposition (PEAC), Shenzhen, China, 2018, pp. 1–5
- [6] Yao, W., Hu, H., Lu, Z.: 'Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter', *IEEE Trans. Power Electron.*, 2008, **23**, pp. 45–51
- [7] Aleenejad, M., Mahmoudi, H., Jafarishadeh, S., *et al.*: 'Fault-tolerant space vector modulation for modular multilevel converters with bypassed faulty submodules', *IEEE Trans. Ind. Electron.*, 2019, **66**, pp. 2463–2473
- [8] Aleenejad, M., Iman-Eini, H., Farhangi, S.: 'Modified space vector modulation for fault-tolerant operation of multilevel cascaded H-bridge inverters', *IET Power Electron.*, 2013, **6**, pp. 742–751
- [9] Jana, K.C., Biswas, S.K., Chowdhury, S.K.: 'Performance evaluation of a simple and general space vector pulse-width modulation-based M-level inverter including over-modulation operation', *IET Power Electron.*, 2013, **6**, pp. 809–817
- [10] Li, W., Hu, J., Hu, S., *et al.*: 'Capacitor voltage balance control of five-level modular composited converter with hybrid space vector modulation', *IEEE Trans. Power Electron.*, 2018, **33**, pp. 5629–5640
- [11] Jiao, Y., Lee, F.C., Lu, S.: 'Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction', *IEEE Trans. Power Electron.*, 2014, **29**, pp. 5579–5591
- [12] Amini, J.: 'An effortless space-vector-based modulation for N-level flying capacitor multilevel inverter with capacitor voltage balancing capability', *IEEE Trans. Power Electron.*, 2014, **29**, pp. 6188–6195



- [13] Fei, W.: 'Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters', *IEEE Trans. Ind. Appl.*, 2002, **38**, pp. 500–506
- [14] Piao, C., Hung, J.Y.: 'A simplified and unified space vector PWM algorithm for multi-level diode clamped VSI'. 2015 IEEE Int. Conf. on Industrial Technology (ICIT), Seville, Spain, 2015, pp. 2770–2776
- [15] Maheshwari, R., Busquets-Monge, S., Nicolas-Apruzzese, J.: 'A novel approach to generate effective carrier-based pulsewidth modulation strategies for diode-clamped multilevel DC–AC converters', *IEEE Trans. Ind. Electron.*, 2016, **63**, pp. 7243–7252
- [16] Tian, H., Li, Y.W.: 'Carrier-based stair edge PWM (SEPWM) for capacitor balancing in multilevel converters with floating capacitors', *IEEE Trans. Ind. Appl.*, 2018, **54**, pp. 3440–3452
- [17] Yu, H., Chen, B., Yao, W., *et al.*: 'Hybrid seven-level converter based on T-type converter and H-bridge cascaded under SPWM and SVM', *IEEE Trans. Power Electron.*, 2018, **33**, pp. 689–702
- [18] Yu, H., Chen, B., Yao, W., *et al.*: 'A space vector PWM scheme for multilevel inverters based on two-level space vector SPWM', *IEEE Trans. Ind. Electron.*, 2006, **53**, pp. 1631–1639
- [19] Das, S., Narayanan, G.: 'Novel switching sequences for a space-vector-modulated three-level inverter', *IEEE Trans. Ind. Electron.*, 2012, **59**, pp. 1477–1487
- [20] Ahmed, I., Borghate, V.B.: 'Simplified space vector modulation technique for seven-level cascaded H-bridge inverter', *IET Power Electron.*, 2014, **7**, pp. 604–613
- [21] Celanovic, N., Boroyevich, D.: 'A fast space-vector modulation algorithm for multilevel three-phase converters', *IEEE Trans. Ind. Appl.*, 2001, **37**, pp. 637–641
- [22] Li, J., Jiang, J., Qiao, S.: 'A space vector pulse width modulation for five-level nested neutral point piloted converter', *IEEE Trans. Power Electron.*, 2017, **32**, pp. 5991–6004
- [23] Liu, Z., Wang, Y., Tan, G., *et al.*: 'A novel SVPWM algorithm for five-level active neutral-point-clamped converter', *IEEE Trans. Power Electron.*, 2016, **31**, pp. 3859–3866
- [24] Grigoletto, F.B., Schuetz, D., Junior, L.A., *et al.*: 'Space vector modulation for packed-U-cell converters (PUC)'. IECON 2018 – 44th Annual Conf. of the IEEE Industrial Electronics Society, Washington, DC, USA, 2018, pp. 4498–4503
- [25] Ahmed, I., Borghate, V.B., Matsa, A., *et al.*: 'Simplified space vector modulation techniques for multilevel inverters', *IEEE Trans. Power Electron.*, 2016, **31**, pp. 8483–8499
- [26] Li, C., Lu, R., Li, W., *et al.*: 'Space vector modulation for Sic & Si hybrid active neutral point clamped converter'. 2018 IEEE Int. Power Electronics and Application Conf. and Exposition (PEAC), Shenzhen, China, 2018, pp. 1–6
- [27] Bai, Z., Chen, H., Ma, H.: 'Implementation of space vector modulation (SVM) for modular multilevel converter based on submodule regroup'. 2018 IEEE Int. Power Electronics and Application Conf. and Exposition (PEAC), Shenzhen, China, 2018, pp. 1–6
- [28] Deng, Y., Wang, Y., Teo, K.H., *et al.*: 'A simplified space vector modulation scheme for multilevel converters', *IEEE Trans. Power Electron.*, 2016, **31**, pp. 1873–1886
- [29] Lin, H., Shu, Z., He, X., *et al.*: 'ND SVPWM with DC voltage balancing and vector smooth transition algorithm for a cascaded multilevel converter', *IEEE Trans. Ind. Electron.*, 2018, **65**, pp. 3837–3847
- [30] Ariff, E.A.R.E., Dordevic, O., Jones, M.: 'A space vector PWM technique for a three-level symmetrical six-phase drive', *IEEE Trans. Ind. Electron.*, 2017, **64**, pp. 8396–8405
- [31] Dekka, A., Wu, B., Zargari, N.R., *et al.*: 'A space-vector PWM-based voltage-balancing approach with reduced current sensors for modular multilevel converter', *IEEE Trans. Ind. Electron.*, 2016, **63**, pp. 2734–2745
- [32] Deng, Y., Teo, K.H., Duan, C., *et al.*: 'A fast and generalized space vector modulation scheme for multilevel inverters', *IEEE Trans. Power Electron.*, 2014, **29**, pp. 5204–5217
- [33] Fukuda, S., Iwaji, Y.: 'A single-chip microprocessor-based PWM technique for sinusoidal inverters'. 1988 IEEE Industry Application Society Annual Meeting, Pittsburgh, PA, USA, 1988, pp. 921–926
- [34] McGrath, B.P., Holmes, D.G., Lipo, T.: 'Optimized space vector switching sequences for multilevel inverters', *IEEE Trans. Power Electron.*, 2003, **18**, pp. 1293–1301