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ARQUITETURA DE COMPUTADORES

AC1 – AVALIAÇÃO SOMATIVA 01

01.) PROJETAR um circuito binário com portas lógicas capaz de produzir as seguintes saídas.

	abcd	saidas	s2	s1	s0
0	0000	2	0	1	0
1	0001	1	0	0	1
2	0010	1	0	0	1
3	0011	1	0	0	1
4	0100	4	1	0	0
5	0101	2	0	1	0
6	0110	1	0	0	1
7	0111	1	0	0	1

	abcd	saidas	s2	s1	s0
8	1000	4	1	0	0
9	1001	4	1	0	0
10	1010	2	0	1	0
11	1011	1	0	0	1
12	1100	4	1	0	0
13	1101	4	1	0	0
14	1110	4	1	0	0
15	1111	2	0	1	0

s2	00	01	11	10		s1	00	01	11	10		s0	00	01	11	10
ab\cd						ab\cd						ab\cd				
00	0	0	0	0		00	1	0	0	0		00	0	1	1	1
01	1	0	0	0		01	0	1	0	0		01	0	0	1	1
11	1	1	0	1		11	0	0	1	0		11	0	0	0	0
10	1	1	0	0		10	0	0	0	1		10	0	0	1	0

a.) SoP(4,8,9,12,13,14)
(a’.b.c’.d’)+(a.b’.c’.d’)+(a.b’.c’.d)+(a.b.c’.d’)+(a.b.c’.d)+(a.b.c.d’)

b.) PoS(1,2,3,4,6,7,8,9,11,12,13,14)

c.) SoP(1,2,3,6,7,11)
(a’.b’.c’.d)+(a’.b’.c.d’)+ (a’.b’.c.d)+(a’.b.c.d’)+ (a’.b.c.d)+(a.b’.c.d)

d.) (14,12) = (a.b.d’)
(4,12) = (b.c’.d’)
(8,9,12,13) = (a.c’)
S2 = (a.c’)+(a.b.d’)+(b.c’.d’)

e.) 0 = (a’.b’.c’.d’)
5 = (a’.b.c’.d)
15 = (a.b.c.d)
10 = (a.b’.c.d’)
s1 = (a’.b’.c’.d’)+(a’.b.c’.d)+(a.b.c.d)+(a.b’.c.d’)

f.) (11,3) = (b’.c.d)
(1,3) = (a’.b’.d)
(2,3,6,7) = (a’.c)
S0 = (a’.c)+(b’.c.d)+(a’.b’.d)

g.) (a.c’)+(a.b.d’)+(b.c’.d’)
(a.c’)+ (a.c’)+(b.d’)

h.) (a’.b’.c’.d)+(a’.b.c’.d)+(a.b.c.d)+(a.b’.c.d’)= (a’+c’)+(b’.d+b.d)+(a+c)+(b.d+b’.d’)
(a’+c’)+d+(a+c).(b.d(+)b’.d’)

i.) (a’.b’.c.d)+(a’.b’.c’.d)+(a’.b’.c.d)+(a’.b.c.d)+(a’.b.c.d’)+(a.b’.c.d)

(a’.b’).(c.d+c’.d)+(a’.c).(b’.d+b.d) +c(a’.b.d’+a.b’.d)

((a’.b’).d)+((a’.c).d)+c(a’.b.d’+a.b’.d)

(a’.b’.d)+(a’.c.d)+c(a’.b.d’+a.b’.d)=(a’.d)(b’+c)+c(a’.b.d’+a.b’.d)

(a’.d)(b’+c)+c(a’.b.d’)+(a.b’.d)