# ***Laboratory Report 4 Digital Systems***

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| Module | EE4522. Digital Systems 1 |
| Date | 09/02/2023 |
| Lab Number | 4 |
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## Introduction

In this lab using the base system from Lab 2a, we had to build a new system which has a 7-segment display part in it. The 7-segment display contains seven light-emitting diodes labelled from a to g. Using OR, AND and XOR gates we had to construct the digital system.

## Procedure

To construct this board we had to use the base system from lab 2a and then make it so that the 7-segment display creates the numbers 0,1,2 and 3 in this order. To build the 2$^{nd}$ part of the system we needed this equipment:

- Another breadboard
- 74HC08 chip
- 74HC14 chip
- 7-segment display
- 330 Ω resistors
- Extra wires

With these components it was possible to build the circuit using Schematics, photos and wire diagrams. The final design should look like figure 2.

## Results

Challenge 4.2 When circuit is finally built, we had to test whether it works. It needed to display 0, 1, 2 and 3 in this order however it didn't work at all of me. I needed to do the Boolean algebra first to (Table 1).

**Table 1:**

| x | y | a | b | c | d | e | f | g |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

After completing the truth table I needed to do Boolean algebra to be able to create the wire diagram.

A = x'•y

B = GND

C=x •x'

D=x'•y

E=y

F=(x'•y')'

G = x'

As I hadn't made the wire diagram beforehand, the wires were all over the place. So, I made out the wire diagram with the help of technicians. (Figure 1)

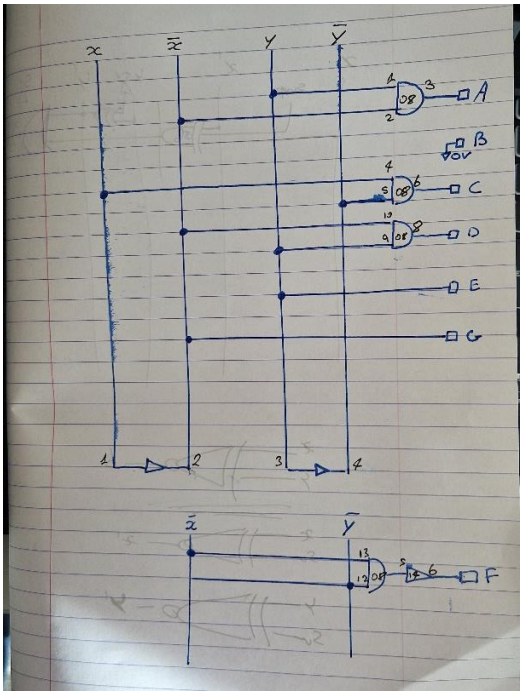
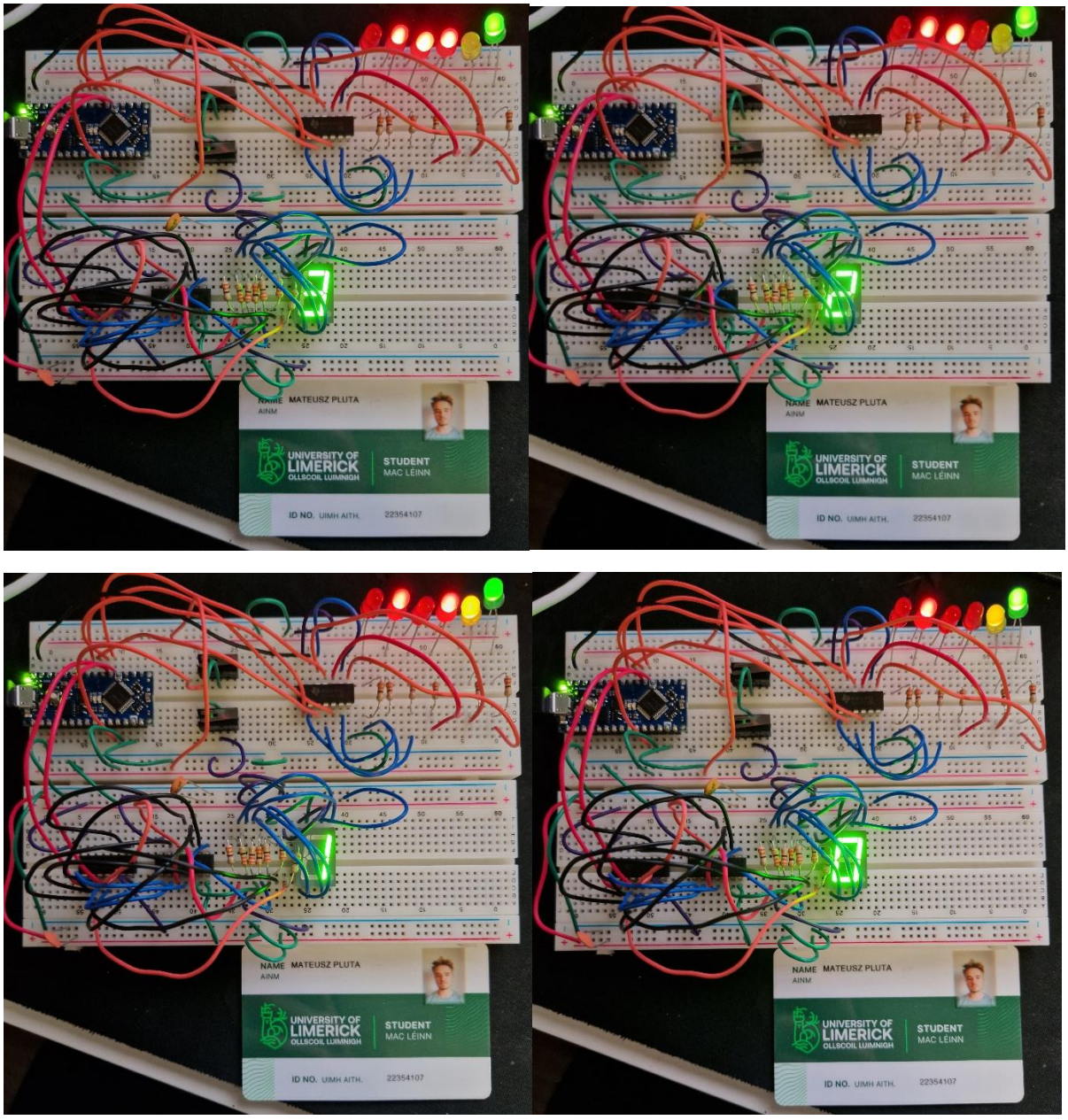



*Figure 1 Wire diagram to make 0,1,2,3.*

Challenge 4.1 I was then finally able to complete the circuit with it properly working as expected. (Figure 2,3,4,5)




Figures 2,3,4 and 5 displaying the numbers shown on the board

Challenge 4.3 – Test or fail verification table.

**Table 2**

| 7-segment display outputs | Pass or fail |
|---|---|
| 0 | Pass |
| 1 | Pass |
| 2 | Pass |
| 3 | Pass |

Challenge 4.4 We had to download the simulation model from sulis and run the simulator. The Simetrix model looks like figure 6.

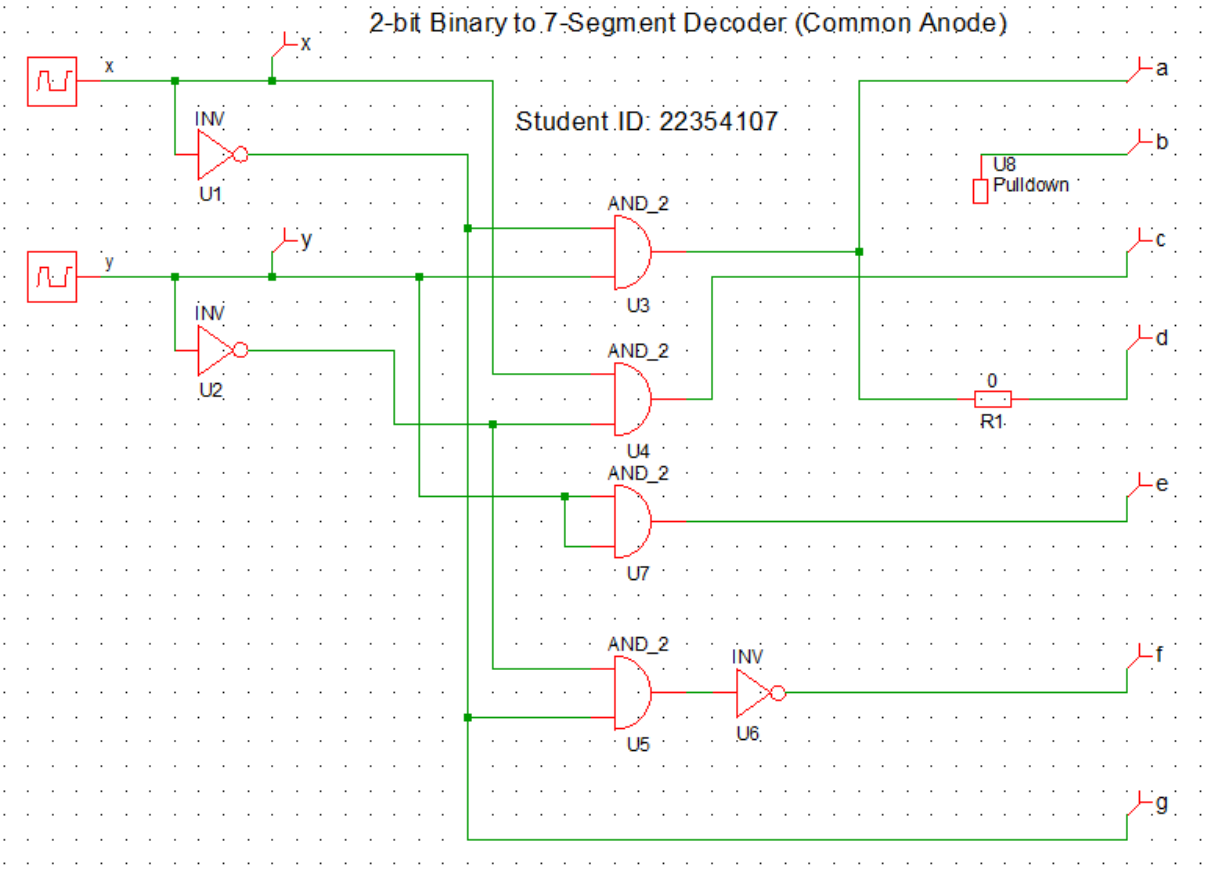



*Figure 6 Simetrix model of the circuit*

When the simulation is run, we get from x, y and from a to g plots (Figure 7). As we can see each represent a binary path just like we can see in Table 1. When the line is at the bottom it means its at 0 and when the line is at the top it means its 1.

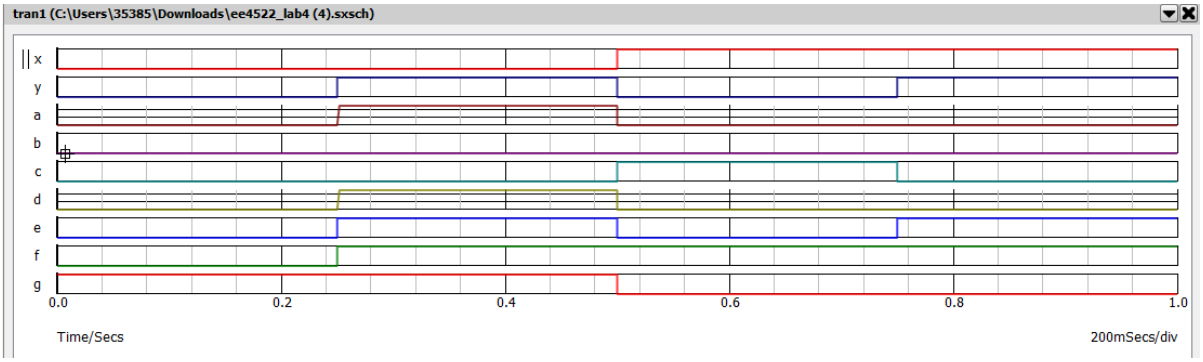



*Figure 7 Plots of x, y and a to g.*

Challenge 4.5:- We had to build an advanced circuit using an XOR gate (74HC86) and instead of the 7-segment display, displaying 0, 1, 2, 3. We needed it to display A, b, c, d as seen in figures 8,9,10 and 11.

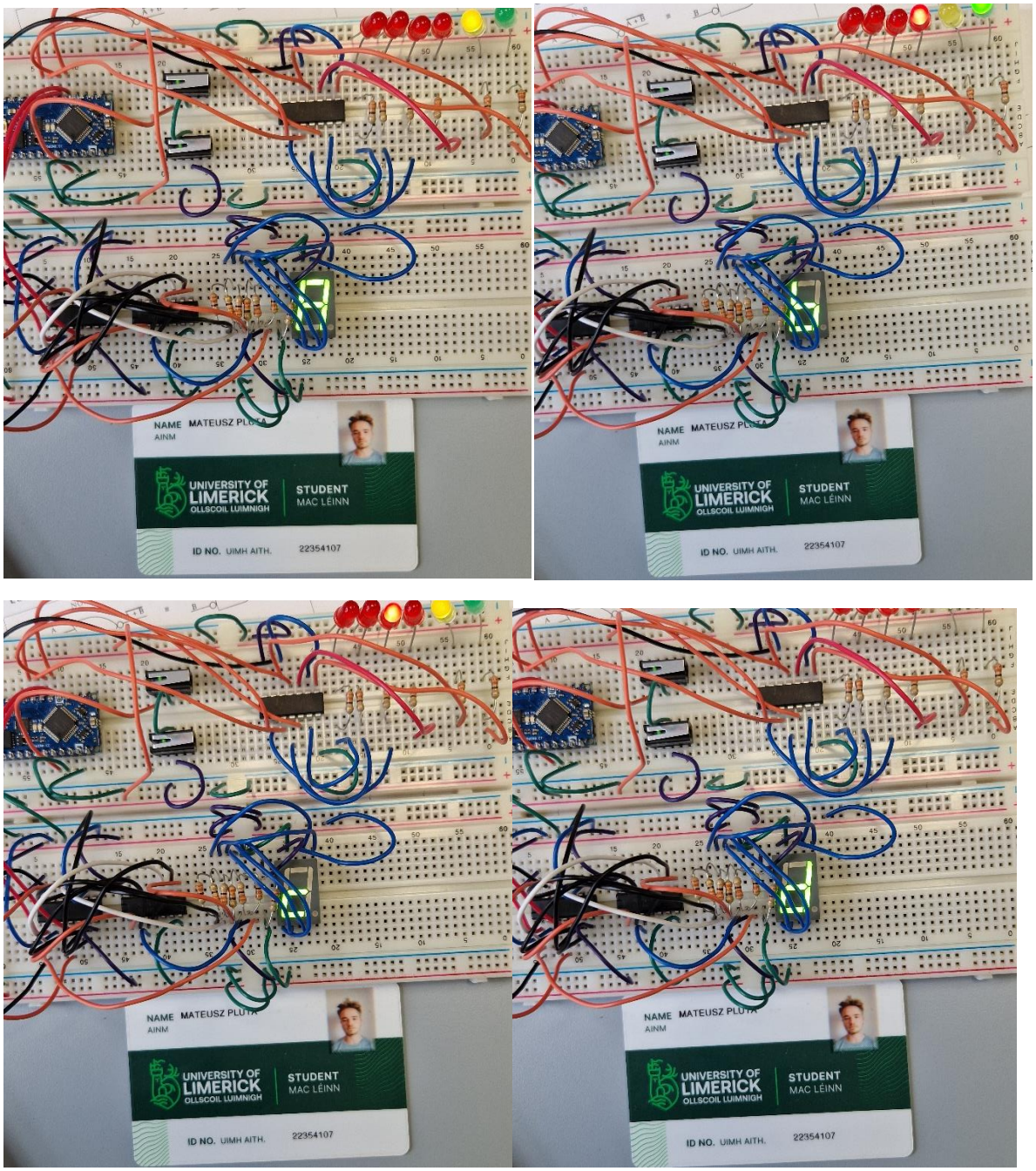



Figure 8,9,10 and 11 Pictures of advanced circuit

Once again, I needed to create another wire diagram and algebra to be able to build the circuit.

a = (x’•y’)’

b = x•y

c= x•y’

d=x’•y’

e=GND

f=x

g=GND

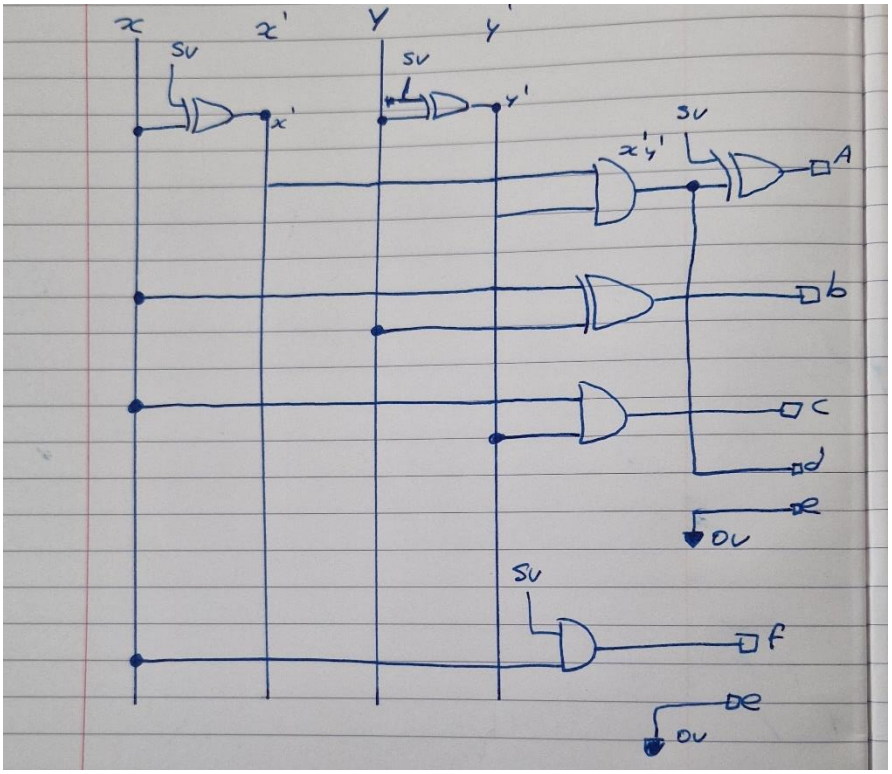



*Figure 12 The wire diagram for advanced circuit*

I have successfully been able to construct the circuit and worked perfectly when I tested it. I had trouble understanding the ‘’b’’ but the technicians assisted me greatly.

**Table 3**

| 7-segment display outputs | Pass or fail |
|---|---|
| A | Pass |
| b | Pass |
| c | Pass |
| d | Pass |

## Conclusion

In conclusion I was able to complete both circuits and understand how XOR, OR and AND gates work which was complicated at first as I didn't understand the algebra however the technicians assisted me with it. I was also able to complete every challenge without much trouble.

Declaration of authorship: "I confirm that this lab report, submitted for assessment, is my own original work".