Laboratory Report 9 Digital Systems

Module	EE4522. Digital Systems 1
Date	17/04/2023
Lab Number	9
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Introduction:

In this lab we will focus on testing and debugging the finite state machine (FSM) which is a maths model used to describe and analyse systems that exhibit a finite number of states and transition between those states. We will need to build the circuit, then test it and recording the data. Later we will use Simetrix to simulate the model and get the plots.

Procedure:

We will be required to use the following equipment to complete the circuit:

- Breadboard
- Wires
- 7 LED's
- 330Ω, 100Ω and 10kΩ resistors
- 74HC175 chip
- 74HC00
- 74HC14

Using the schematic and a wiring diagram I was able to build the FSM with easy however wiring the circuit proved to be challenging as it got very confusing considering the number of wires used. The circuit should look like figure 1.

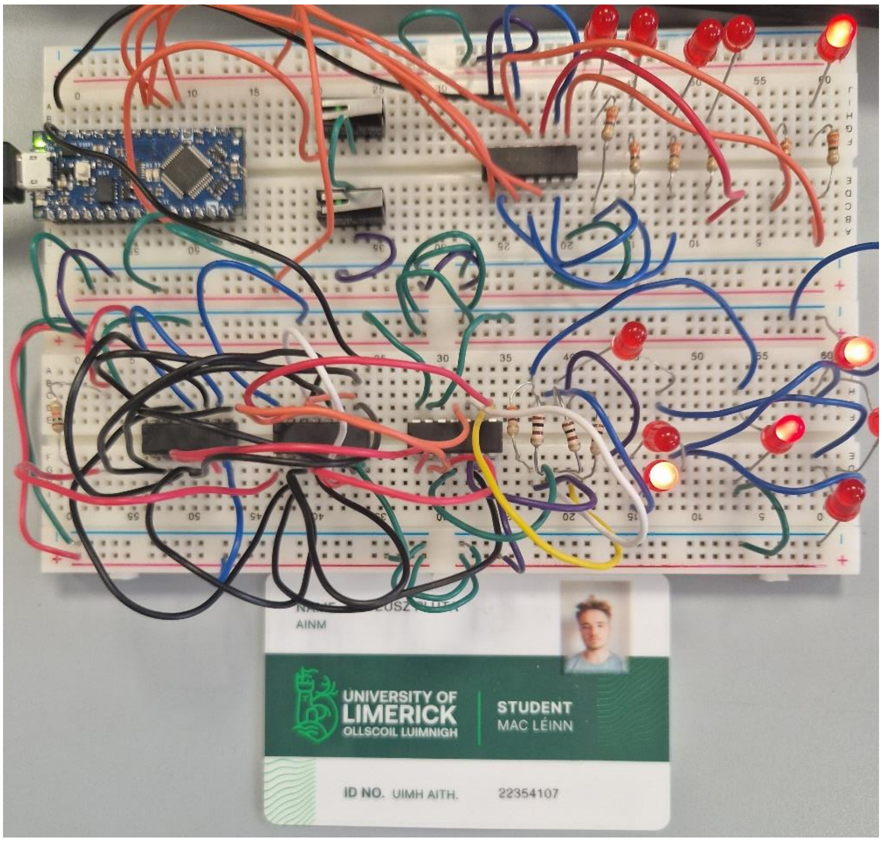


Figure 1 Photo of the circuit

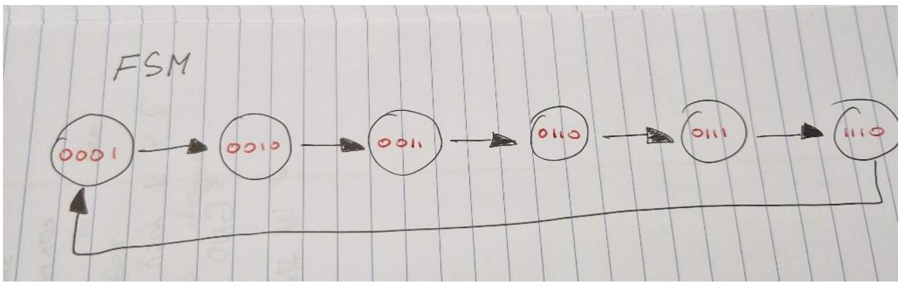
Results:

Challenge 9.1

The reason for the choice of resistors for R1 to R4 is because, in R1 resistor the current only travels to only 1 LED compared to R2, R3 and R4 where the current travels to two LED’s therefore it need more current for the LED’s to light up evenly.

Challenge 9.2

Here is a sketch of the FSM diagram.

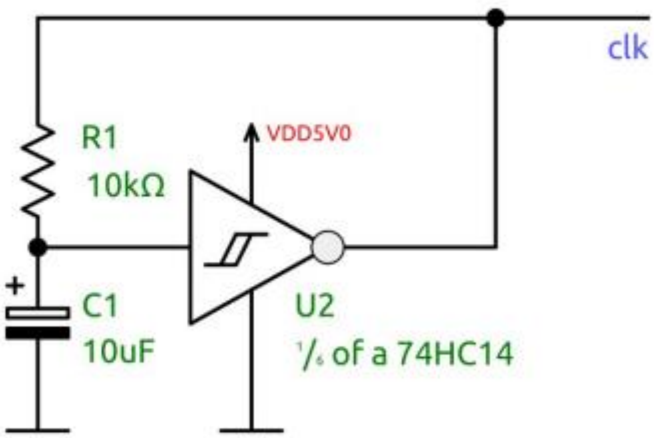


Challenge 9.3

To convert the FSM for manual clocking I need to swap the wire from Fout to counter[0] which was connected to one of my button. With a click of a button I was able to change the LED lights as shown in the truth table. However, sometimes while clicking the button the lights dident respond but that might have been a problem with my circuit.

Challenge 9.4

In this challenge we had go and create a relaxation oscillator for our circuit (Figure 2). Using the components as shown on the diagram however we have used the 30kΩ resistor and 100nF capacitor.



It took a while to build as I was struggling to get it correct however with the help of lab technicians, I was able to build it. The results are shown on figures 4 and 5. Where we can see the capacitor discharge at the end of the wave.

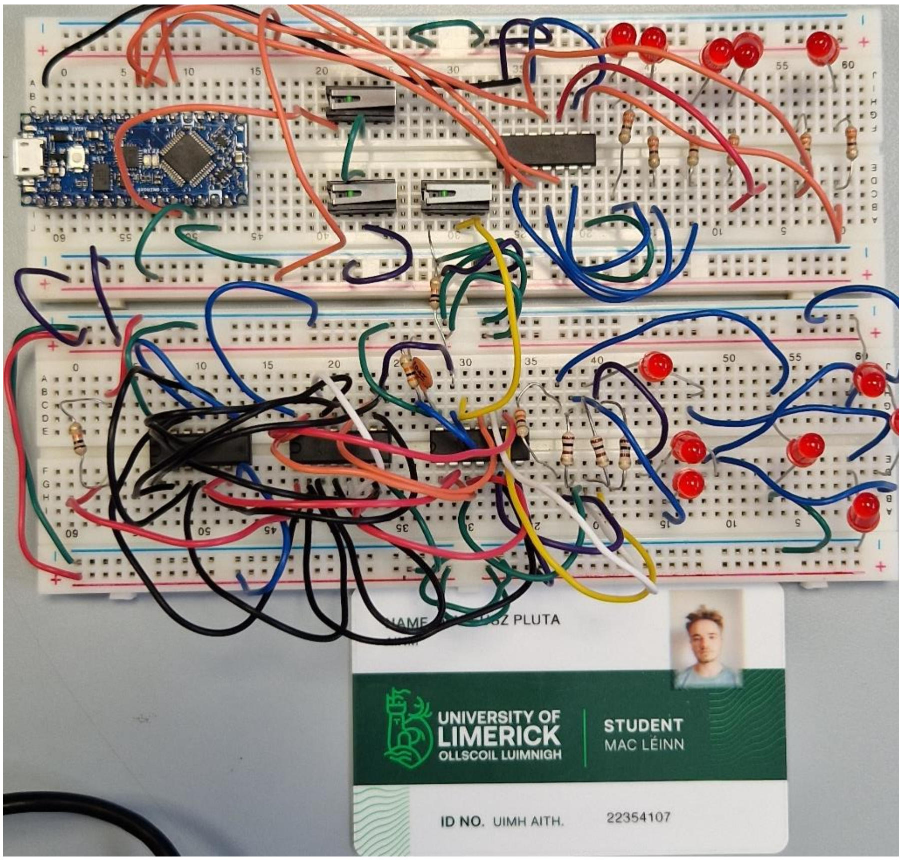
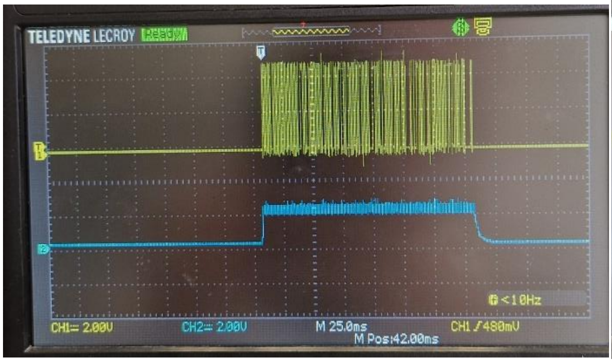
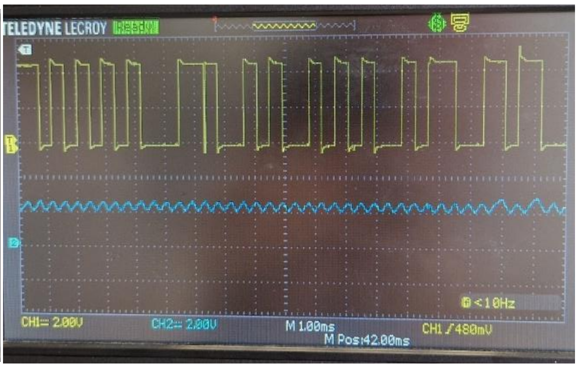


Figure 3 Photo of the relaxation oscillator in the circuit



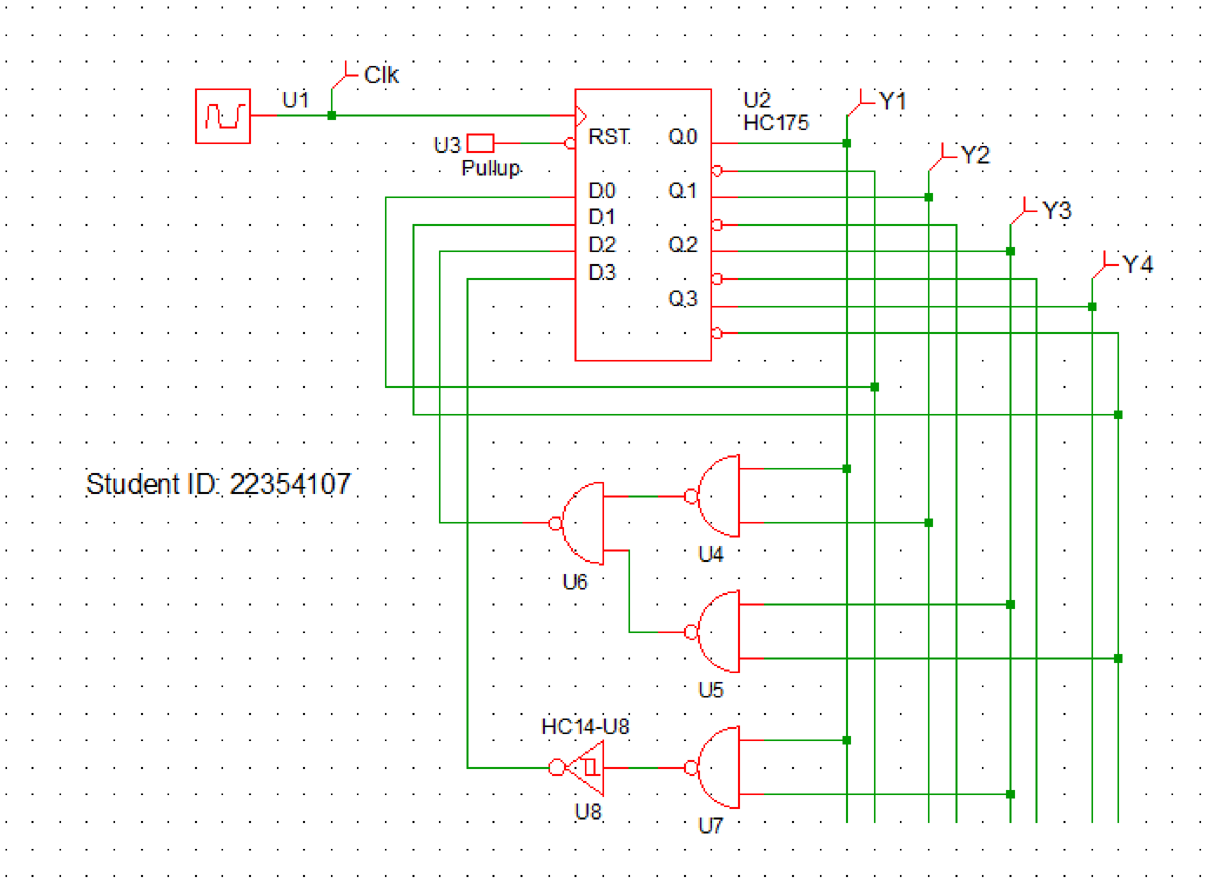


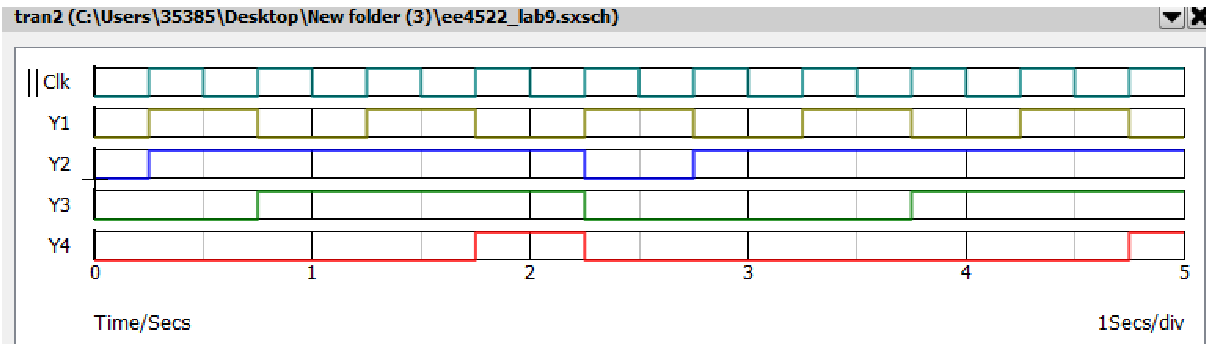
Figures 4 and 5. Scope photos of the results from the oscillator.

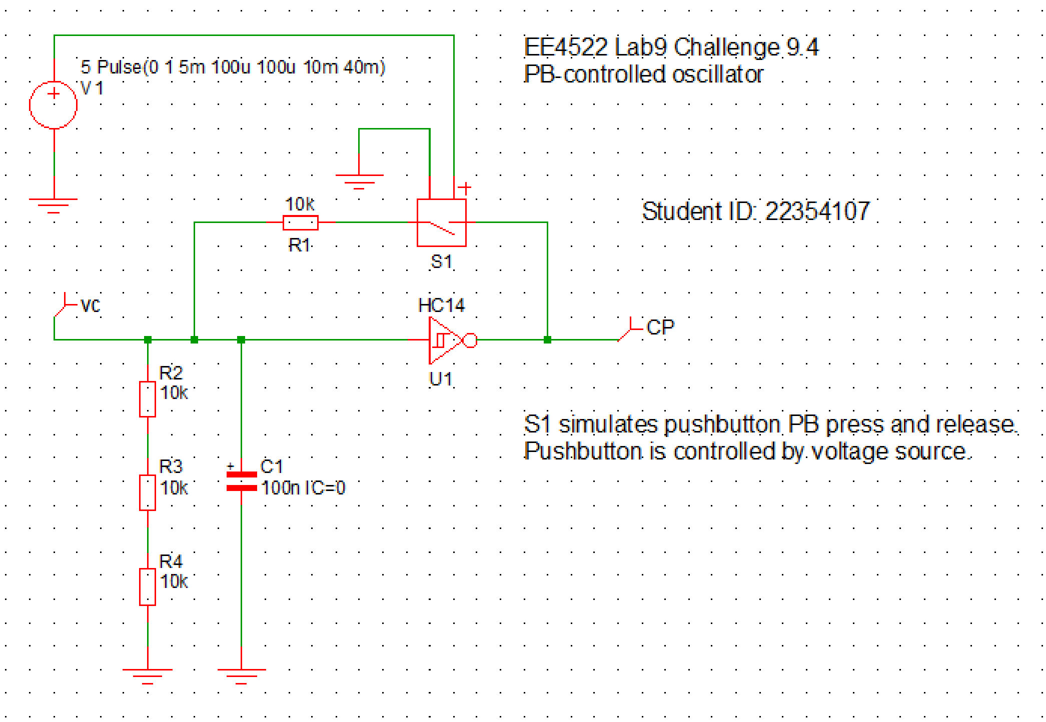
Challenge 9.5

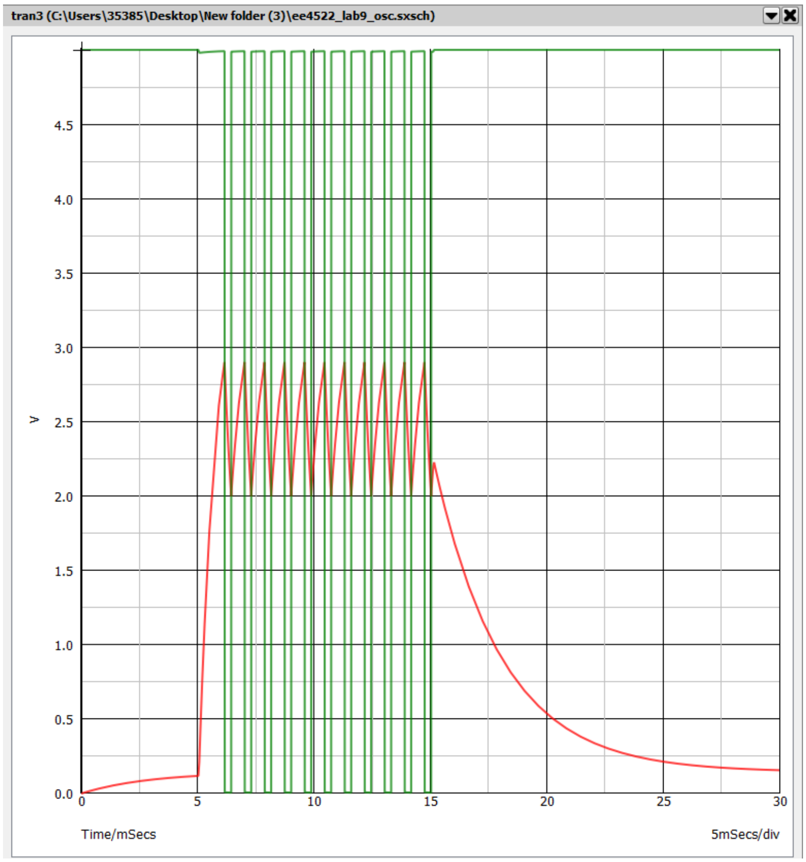
I have tested the circuit multiple times however making a table of 100 rows would take multiple pages. I have tested the circuit around 25 times and different results came out from the LED's.

Challenge 9.6









This output from the simulation is the same as the one I have achieved on the scope in the lab. We can the charge and discharge of the capacitor.

Conclusion:

In conclusion, the lab focused on testing and debugging the finite state machine (FSM). I was able to test and debug the system after I successfully was able to build it will little trouble however I was struggling with building the relaxation oscillator. When I finally build it, I was able to take all the results. As well as create the simulation and get the data from it.

Declaration of authorship: “I confirm that this lab report, submitted for assessment, is my own original work”.