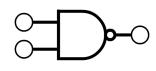
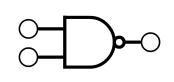
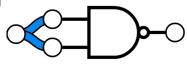
NAND

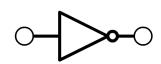




Input A	Input B	Output
0	0	1
1	0	1
0	1	1
1	1	0

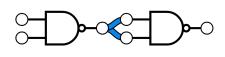
NOT

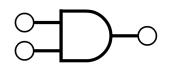




Input	Output
1	0
0	1

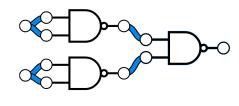
AND

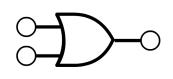




Input A	Input B	Output
0	0	0
0	1	0
1	0	0
1	1	1

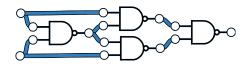
OR

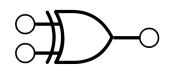




Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	1

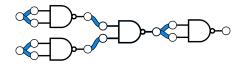
XOR

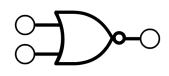




Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

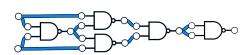
NOR

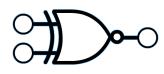




Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

XNOR





Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	1