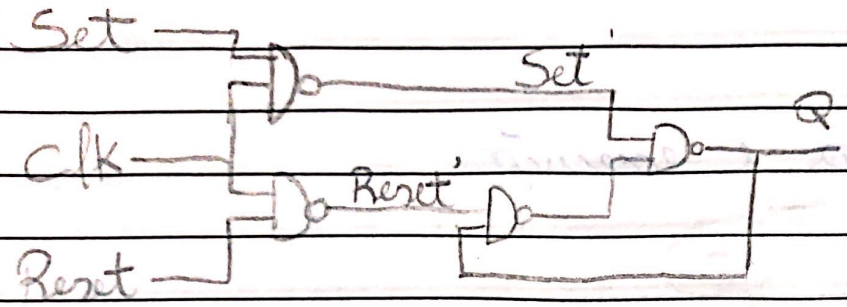


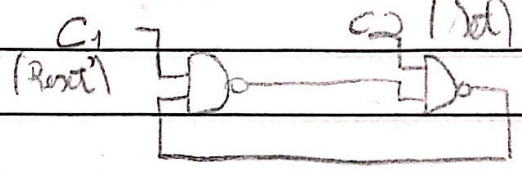
Clock	Set	Reset	Set'	Reset'	Q
1	0	0	1	1	est. anterior
1	0	1	1	0	0
1	1	0	0	1	1
1	1	1	0	0	inválido

* Clock = 0 → no change

→ Nesse caso, ambas as saídas dos portas NAND retornam 1, o que é considerado um erro lógico.

/ /

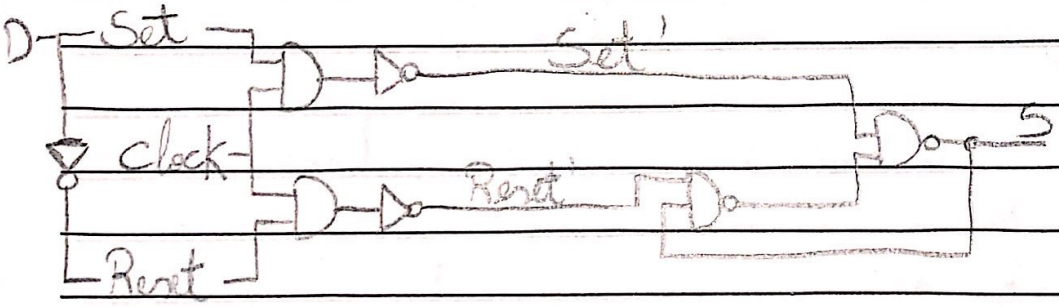
Set / Reset



↑
Unidade de memória

D → Nand

e0	e1	And	Nand
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



* quando clock for 0, impede que um novo dado seja gravado