Mahindra University Hyderabad

École Centrale School of Engineering

End-semester Examination

Program: B. Tech. **Branch: CS/ AI/ ECM/ CM** **Year: III** **Semester: I**

Subject: Operating Systems (CS 3102)

Date: 13th December, 2024 **Start Time: 10 AM**

Time Duration: 3 Hours **Max. Marks: 100**

Instructions:

1) All questions are mandatory. Please attempt all the questions in order.

2) If anyone has a doubt, please mention your assumptions and proceed with answering.

Q1. Give appropriate answers: $(10 \times 2 = 20\ marks)$

a) A process is a program in execution, and the operating system uses _____ to switch between processes efficiently.

b) Part of program that should be executed indivisibly because it accesses shared memory is

(i) Semaphore (ii) Directory (iii) Critical Section (iv) Mutual Execution

c) Banker's algorithm for resource allocation deals with _____.

d) Scheduling algorithm that most likely to cause the problem of starvation

(i) FCFS (ii) SJF (iii) RR (iv) Multi-level Scheduling

e) The mechanism that brings a page into memory only when it is needed, is called _____.

f) The memory allocation technique that suffers from external fragmentation-

(i) Paging (ii) Segmentation (iii) Fixed partitioning (iv) Variable partitioning

g) The _____ scheduling algorithm selects the process with the shortest execution time for the CPU next.

h) CPU performance is measured in terms of:

(i) Throughput (ii) MHz (iii) Flops (iv) None of the above

i) The _____ is the set of all addresses generated by a program during its execution.

j) _____ is the heart of an operating system.

Q2. Provide answers for the following: $(2 + 2 + 2 + 2) + 12 = 20\ marks$

(a) Consider the workload in the following table:

Process ID	Burst Time	Priority	Arrival Time
P1	10	4	1
P2	12	3	0
P3	5	2	2
P4	8	1	4

Draw the Gantt chart for the preemptive shortest job first and preemptive priority scheduling. What is the waiting time for each process for each of the algorithm above? What is the average waiting time for each?

(b) A processor uses 2-level page table for logical to physical address translation. The page tables for both the levels are stored in main memory. Logical address and physical address are both 32 bits wide. The memory is byte addressable. For logical to physical address translation the 10 most significant bits of logical address are used as index into 1st level page table while the next 10 bits are used as index into 2nd level page table. The 12 least significant bits of logical

address are used as offset within the page. Assume that the page table entries in both levels of page table are 4bytes wide. Further, the processor has TLB with hit ratio of 96%. The TLB caches recently used page numbers and corresponding physical page numbers. The processor also has a physically addresses cache with hit ratio of 90%, main memory access time is 10ns, cache access time is 1ns and the TLB access time is 1ns. Then what is the effective memory access time?

Q3. Answer the following questions: $(3+2)+5+(5+5)=20$ ***marks***

a) Explain Race condition with respect to Process Synchronization. What are semaphore and mutex?

b) Justify the following statement: "Cycle in resource allocation graph does not always imply the occurrence of deadlock."

c) Imagine two concurrent threads, P and Q, running at the same time. P prints '0' and '1' in a loop, first '0', then '1', and repeats this forever. Q does the same thing but in a different loop, printing '0' and '1' over and over. First, write the pseudocodes for P and Q. Now, to ensure the output always appears in the sequence '0011', use two semaphores—let's name them S and T. Figure out how to use them at specific points in the loops of P and Q so that '0011' keeps appearing nonstop without interruption.

Q4. Answer the following: $(2+3)+\big((2.5+2.5)+(2.5+2.5)\big)+(2+3)=$ **20** ***marks***

a) What is the purpose of modify bit in page table? Explain the difference between external fragmentation and internal fragmentation with suitable example.

b) If **LRU page replacement** is used with four frames, and the process considers the following page reference string:7,0,1,2,0,3,0,4,2,3,0,3,2,1,2,0,1,7,0,1. Assuming 4 frames are available and initially none of the pages are present in the main memory. Then calculate: (i) **Page Fault Ratio** (ii) **Page Hit Ratio** (iii) Now, consider a TLB added to the system with **FIFO replacement policy**. Given the TLB size is of 2 entries. Then calculate: the total number of **TLB misses** and **TLB hits** while processing the reference string. *(Initially the TLB is empty. A TLB hit is when entry for a page being referred is found in the TLB, whereas a miss is when the entry for a page being referred is not in TLB).*

c) What is Thrashing? Explain Belady's Anamoly with suitable example.

Q5. Answer the following: $(5+2)+(2+2+2)+7=20$ ***marks***

a) Explain the difference between sequential access and random access in file operations. Differentiate between absolute path and relative path.

b) Consider a disk with 1000 blocks and a block size of 512 bytes. If a file occupies 6 KB, calculate the number of blocks required for its storage under: (i) Contiguous allocation (ii) Linked allocation (iii) Indexed allocation

c) Consider a disk system has an average seek time of 60ns and the rotation rate of 3600rpm. Each track of the disk has 512 sectors each of size 2KB. Then what is the approximate time required to read 1200 random sectors?