Mahindra University Hyderabad
École Centrale School of Engineering
End-semester Regular Examination

Program: B.Tech. Branch: Computation & Mathematics Year: Second Semester: Second
Subject: Computer Organization (MA 2211)

Date: 05/06/2023 **Start Time: 10:00 PM**
Time Duration: 03:00 Hours **Max. Marks: 100**

Instructions:

1) **All questions are compulsory.**
2) **Start each answer on a new page and number your answers clearly. Answer all parts of the same question together and in sequence.**
3) **An explanation of every step is essential. Correct outcomes without description will not be evaluated.**

Question 01: Select the correct choice for the following questions with a proper explanation. Correct choices without valid justification will not be considered. *[02 × 20]*

A) If $(B2F8)_{16} = (?)_{10}$. What will be the value of "Question Mark"?

a) 51246 b) 45817 c) 32678 d) None of these

B) In a half adder, the carry output is high if the inputs are:

a) 1, 1 b) 0, 0 c) 0, 1 d) 1, 0

C) A variable on its own or in its complemented form is known as a _____

a) Product term b) Literal c) Sum term d) Word

D) Which of the following is equivalent to the Boolean expression A(A + B)?

a) AB b) 1 c) (1 + AB) d) A

E) De Morgan's theorem states that _____.

a) $(AB)' = A' + B'$ b) $(A + B)' = A' * B$

c) $A' + B' = A'B'$ d) $(AB)' = A' + B$

F) What is the primary motivation for using Boolean algebra to simplify logic expressions?

a) It may make it easier to understand the overall function of the circuit

b) It may reduce the number of gates

c) It may reduce the number of inputs required

d) All of the above

G) How many input combinations exist in a truth table for the SOP expression $(ABC' + AB'C + A'B'C)$?

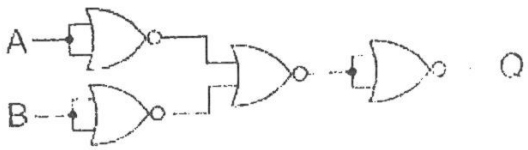
a) 1 b) 2 c) 4 d) 8

H) If A, B, and C are the inputs of a full adder, then the sum is given by _____

a) A AND B AND C b) A OR B AND C

c) A XOR B XOR C d) A OR B OR C

I) The output of the logic circuit given below represents _____ gate.



a) OR b) NOR c) AND d) NAND

J) How many AND, OR, and EXOR gates are required for the configuration of a full adder?

a) 1, 2, 2 b) 2, 1, 2 c) 3, 1, 2 d) 4, 0, 1

K) A digital multiplexer is a combinational circuit that selects _____

a) One digital information from several sources and transmits the selected one

b) Many digital information and convert them into one

c) Many decimal inputs and transmits the selected information

d) Many decimal outputs and accepts the selected information

L) A 32 to 1 multiplexer has the following terminals:

a) 32 outputs, one input, and 5 control signals

b) 32 inputs, one output, and 5 control signals

c) 5 inputs, one control signal, and 32 outputs

d) 5 inputs, 32 control signals, and one output

M) What is the full form of SR?

a) System rated b) Set reset c) Set ready d) Set Rated

N) Determine the values of A, B, C, and D that make the sum term $A' + B + C' + D$ equal to zero.

a) $A = 1, B = 0, C = 0, D = 0$ b) $A = 1, B = 0, C = 1, D = 0$

c) $A = 0, B = 1, C = 0, D = 0$ d) $A = 1, B = 0, C = 1, D = 1$

O) If inputs (a, b) is (0,0) for a 2 × 1 MUX with selector '0'. Then the output is _____?

a) 1 b) 0 c) X d) None of these

P) Any combinational circuit can be designed using only

a) AND Gates b) OR Gates c) XOR Gates d) NOR Gates

Q) How many 3 × 8 line decoders with an enable input line are needed to construct a 6 × 64 line decoder without using any other logic gate?

a) 7 b) 8 c) 9 d) 10

R) _____ converts binary-coded information to unique outputs such as decimal, octal digits, etc.

a) Decoder b) Demultiplexing c) Multiplexing d) Encoder

S) One of De Morgan's theorems states that $(A + B)' = A' \cdot B'$. Simply stated, this means that logically there is no difference between:

a) A NOR and an AND gate with inverted inputs

b) A NAND and an OR gate with inverted inputs

c) An AND and a NOR gate with inverted inputs

d) A NOR and a NAND gate with inverted inputs

T) In the S-R latch, when the SET input is made high, output Q becomes:

a) 0 b) 1

c) No change d) Application not allowed

Question 02: Answer the following questions. It is highly desirable to explain each step. Each question is worth six marks. [06 × 05]

A) Convert the following Binary Numbers into their respective Gray Codes.

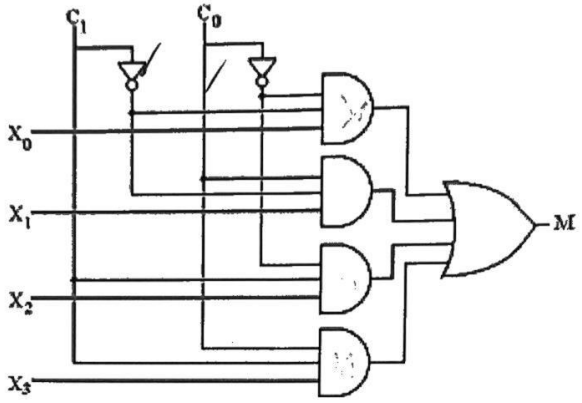
a) 1 1 0 1 1 0 b) 1 1 0 0 1 0 1 0

B) What are complements in digital computers. What are the different complements used for any number system with base r? Find the 9's and 10's complement of $(25.639)_{10}$.

C) A committee of three individuals decides issues for an organization. Each individual votes either yes or no for each proposal that arises. A proposal is passed if it receives at least two yes votes. Design a circuit that determines whether a proposal passes.

D) What is Excess-3 (or EX-3 code or XS-3) code? Convert the decimal numbers 23 and 15.46 to Excess-3 code.

E) Find the output M in the following 4×1 multiplexer, if $c_1 = 0$ and $c_0 = 1$ is given.



Question 03: It is highly desirable to provide an explanation for each step in the following questions. Each question consists of ten marks. [10 × 03]

A) Write the truth table and simplified Boolean expression with four inputs and one output for the following instances. Finally, design the combinational circuit for them.

a) The output is 1 when the binary value of the inputs is greater than five but less than or equal to ten.

b) The output is 1 when the binary value of the inputs is divisible by four.

B) Use K-maps to minimize the following Sum of Product (SOP) expansions:

a) $xy\bar{z} + x\bar{y}\,\bar{z} + \bar{x}yz + \bar{x}\,\bar{y}\,\bar{z}$

b) $xy\bar{z} + x\bar{y}\,\bar{z} + \bar{x}\,\bar{y}z + \bar{x}\,\bar{y}\,\bar{z}$

c) $wxyz + wxy\bar{z} + wx\bar{y}\,\bar{z} + w\bar{x}yz + w\bar{x}\,\bar{y}z + w\bar{x}\,\bar{y}\,\bar{z} + \bar{w}x\bar{y}z + \bar{w}\,\bar{x}yz + \bar{w}\,\bar{x}y\bar{z}$

C) Explain combinational and sequential circuits with suitable examples. Give some applications for both of them. Also highlight some of the significant differences between combinational and sequential circuits.