

legal coats x

Mahindra University École Centrale School of Engineering

2 x op

Program: B.Tech.

Hyderabad

Year: II

2 MNO

Branch: Mechatronics
Minor I Examination

Subject: EE2201 Digital Electronics

Semester: II

Date: 06.03.2023

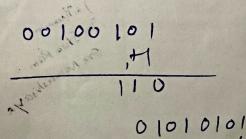
Time Duration: 1:30 Hours

Time: 10.00 AM to 11.30 AM

Max. Marks: 60

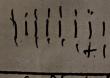
Note: Use of calculator is not allowed.

	Total Culturator is not allowed.	
Q 1	Use a Karnaugh map to reduce each expression to a minimum SOP form	(1.0)
	a. $A'B'C'D' + AC'D' + B'CD' + A'BCD + BC'D$ b. $x'z + w'xy' + w(x'y + xy')$	(12)
	Q 2	Use Quine McCluskey method to minimize
		(12)
0.0	$S = \sum (0, 1, 2, 4, 6, 8, 9, 11, 13, 15)$	
Q 3	Design a combinational circuit with 4 inputs w, x, y, and z, and one output, f. The	(12)
	output "f" is one of the segments in the seven-segment display. w, x, y and z are	
	BCD inputs.	
Q 4	For the Boolean function given by,	(10)
	F = xy'z + x'y'z + w'xy + wx'y + wxy	(12)
	a. Obtain the truth table	
	b. Use any technique to simplify the function to a minimum number of	
	literals	
	rancolon and compare to part(a)	
	d. Draw the logic diagram of the simplified expression.	1
Q 5	Obtain both 1's and 2's complements of y: following binary numbers	(12)
	i. 00010000 iii. 00000000	
	ii. 11011010 iv. 10101010	



1111 000 0

0'8 D+ ABC'+ 8 D'



160086040.