GMBP

Epd of typical Logic gate × no. of gate level

2 XOR
2 AND
1 OR

Mahindra University École Centrale School of Engineering Hyderabad

Program: B.Tech. Branch: Mechatronics Year: II Semester: II

Minor I Examination

Subject: EE2201 Digital Electronics

Date: ***06.03.2023*** Time: ***10.00 AM to 11.30 AM***

Time Duration: ***1:30 Hours*** Max. Marks: **60**

Note: **Use of calculator is not allowed.**

Q 1	Use a Karnaugh map to reduce each expression to a minimum SOP form a. $A`B`C`D` + AC`D` + B`CD` + A`BCD + BC`D$ b. $x`z + w`xy` + w(x`y + xy`)$ c. $A`B`C`D` + A`CD` + AB`D` + AFC`D + A`BD$	(12)
Q 2	Use Quine McCluskey method to minimize $S = \sum(0, 1, 2, 4, 6, 8, 9, 11, 13, 15)$	(12)
Q 3	Design a combinational circuit with 4 inputs w, x, y, and z, and one output, f. The output "f" is one of the segments in the seven-segment display. w, x, y and z are BCD inputs. 	(12)
Q 4	For the Boolean function given by, $F = xy`z + x`y`z + w`xy + wx`y + wxy$ a. Obtain the truth table b. Use any technique to simplify the function to a minimum number of literals c. Obtain the truth table for the simplified function and compare to part(a) d. Draw the logic diagram of the simplified expression.	(12)
Q 5	Obtain both 1's and 2's complements of the following binary numbers i. 00010000 iii. 00000000 ii. 11011010 iv. 10101010	(12)

00100101
+1
110

1110 1111
+1
1111 0000

01010101
+1
10110

A'BD + ABC' + B'D'

11111111
+1
100000000