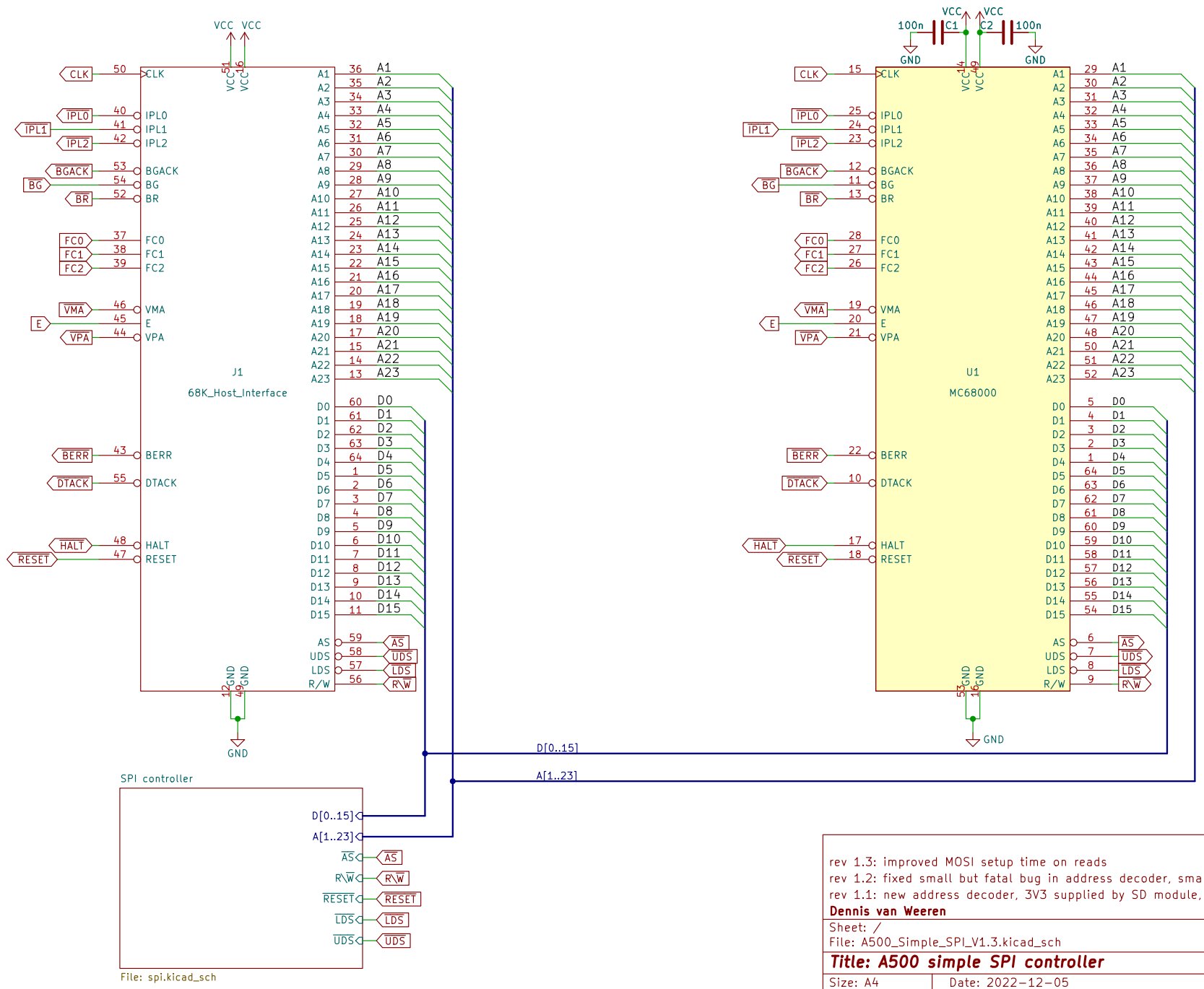


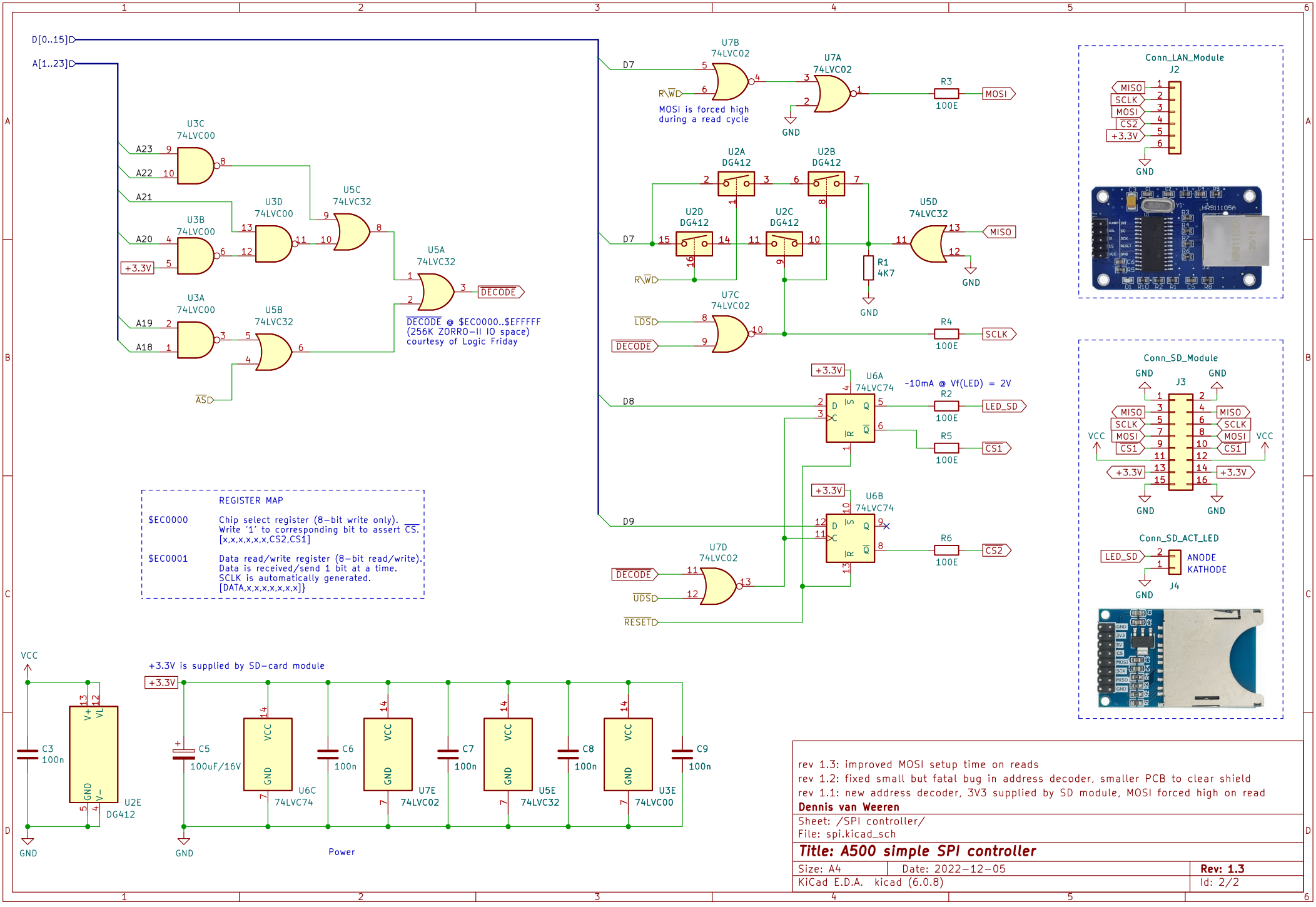
rev 1.3: improved MOSI setup time on reads
rev 1.2: fixed small but fatal bug in address decoder, smaller PCB to clear shield
rev 1.1: new address decoder, 3V3 supplied by SD module, MOSI forced high on read

Dennis van Weeren

Sheet: /
File: A500_Simple_SPI_V1.3.kicad_sch

Title: A500 simple SPI controller

Size: A4	Date: 2022-12-05	**Rev: 1.3**
KiCad E.D.A. kicad (6.0.8)		Id: 1/2


D[0..15]
A[1..23]
U3C 74LVC00
U3D 74LVC00
U3B 74LVC00
U3A 74LVC00
U5C 74LVC32
U5A 74LVC32
U5B 74LVC32
A23
A22
A21
A20
A19
A18
+3.3V
AS
DECODE
DECODE @ $EC0000..$EFFFFF
(256K ZORRO-II IO space)
courtesy of Logic Friday
U7B 74LVC02
U7A 74LVC02
D7
R\W
MOSI is forced high
during a read cycle
GND
R3
100E
MOSI
U2A DG412
U2B DG412
U2D DG412
U2C DG412
U5D 74LVC32
MISO
R1
4K7
U7C 74LVC02
LDS
R4
SCLK
U6A 74LVC74
~10mA @ Vf(LED) = 2V
D8
R2
LED_SD
R5
CS1
U6B 74LVC74
D9
R6
CS2
U7D 74LVC02
UDS
RESET
Conn_LAN_Module
J2
Conn_SD_Module
J3
VCC
Conn_SD_ACT_LED
LED_SD
ANODE
KATHODE
J4
REGISTER MAP
$EC0000 Chip select register (8-bit write only).
Write '1' to corresponding bit to assert CS.
[x,x,x,x,x,x,CS2,CS1]
$EC0001 Data read/write register (8-bit read/write).
Data is received/send 1 bit at a time.
SCLK is automatically generated.
[DATA,x,x,x,x,x,x,x,x]
+3.3V is supplied by SD-card module
C3 100n
U2E DG412
C5 100uF/16V
U6C 74LVC74
C6 100n
U7E 74LVC02
C7 100n
U5E 74LVC32
C8 100n
U3E 74LVC00
C9 100n
Power
rev 1.3: improved MOSI setup time on reads
rev 1.2: fixed small but fatal bug in address decoder, smaller PCB to clear shield
rev 1.1: new address decoder, 3V3 supplied by SD module, MOSI forced high on read
Dennis van Weeren
Sheet: /SPI controller/
File: spi.kicad_sch
Title: A500 simple SPI controller
Size: A4
Date: 2022-12-05
Rev: 1.3
KiCad E.D.A. kicad (6.0.8)
Id: 2/2