

**UNIVERSIDADE POSITIVO
ESCOLA POLITÉCNICA
ENGENHARIA ELÉTRICA
ENGENHARIA DA COMPUTAÇÃO
CIRCUITOS ELÉTRICOS II**

**MEMORIAL DESCritivo:
PROJETO INTERRUPTOR POR PALMAS**

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1 INTRODUÇÃO

A realização desse projeto visa atender a atividade do primeiro bimestre da disciplina de Circuitos Elétricos II dos cursos de Engenharia Elétrica e da Computação da Universidade Positivo. A proposta docente é construir um circuito prático com pelo menos dez elementos básicos e a presença de capacitores ou indutores. É necessário atestar o perfeito funcionamento, realizar este Memorial Descritivo e apresentar em aula. Ao realizar as atividades, o aluno se defrontará com os desafios das diversas fases do projeto e as atividades comporão a aprendizagem e treinamento do futuro engenheiro.

2 MEMORIAL DERCITIVO

Este projeto tem por objetivo inovar e trazer soluções interessantes no chaveamento de lâmpadas ou mecanismos elétricos.

2.1 DEMANDA

A opção de chaveamento por palmas responde a necessidade de acionar algum elemento elétrico sem fazer contato direto com o interruptor. Não importa qual a razão da impossibilidade de se tocar no interruptor.

2.2 DESCRIÇÃO DAS ATIVIDADES

Para executar esse projeto, seguimos o seguinte processo:

- a) Pesquisa de circuitos já disponíveis e definição de qual atenderia melhor ao projeto previamente especificado pelo professor de Circuitos Elétricos II, Jackson Milano;
- b) Verificação em aula com o professor se o circuito escolhido atende aos critérios da proposta;
- c) Teste em matriz de contatos e validação de funcionamento do referido circuito;
- d) Desenvolvimento do *layout* da placa de circuito impresso.
- e) Fabricação na universidade;
- f) Montagem dos componentes e testes finais para assegurar o devido funcionamento;
- g) Elaboração do Memorial Descritivo;

- h) Elaboração do material de apresentação em aula.

2.3 RECURSOS E MATERIAIS UTILIZADOS

O que precisamos para realizar esse projeto é:

2.3.1 Composição do circuito e especificações com base nos *datasheets*:

Destacamos alguns dados principais das especificações dos elementos utilizados no circuito. Na sessão anexo, ao final deste memorial, também trouxemos os *datasheets* na íntegra dos componentes mais relevantes.

- a) Borne modular de 2 vias

Fabricante	Metaltex
Modelo	BR102A
Tensão nominal	250 V
Corrente	16 A
Passo	5 mm
Resistencia de contato	20 mΩ
Resistencia de isolacão	500 MΩ / 1000 VDC

O borne faz a conexão entre os fios da lâmpada e o Relé. Quando o Relé é acionado, o circuito é fechado e a lâmpada acende. Custo aproximado de: R\$ 1,50 cada.

- b) Capacitor eletrolítico radial 47 µF/35 V

Fabricante	United Chemi-Con
Serie	LE
Dielétrico	Alumínio
Temperatura	-10 °C a +105 °C
Tolerância	20%
Espaço entre terminais	2,5 mm

Este capacitor suavizará as alterações da passagem da corrente entre os terminais não permitindo variações bruscas. Custo aproximado de: R\$ 0,20 cada.

c) Clip conector de 2 vias para bateria de 9 V

Fará a conexão da bateria com o circuito para fornecer a energia. Custo aproximado de: R\$ 2,50 cada.

d) Circuito integrado 555

Fabricante	Texas Instruments
Modelo	LM555 Timer
Tensão	5 a 15 V
Corrente	15 mA (máximo)

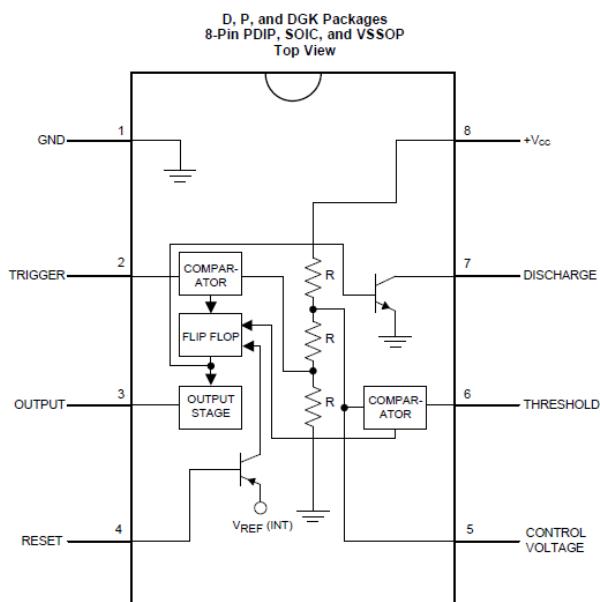


FIGURA 1 – PINAGEM CI 555
FONTE: TEXAS INSTRUMENTS, 2015

O LM555 é um dispositivo altamente estável para gerar oscilações ou atrasos de tempo precisos. Seus terminais estão dispostos como nos mostra a Figura 1 e trazem a opção de acionar (trigger) ou redefinir (reset), conforme o desejado. No circuito, ele fará a oscilação do sinal para o contador CD4017. Custo aproximado de: R\$ 1,50 cada.

e) Circuito integrado CD4017

Fabricante	Texas Instruments
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Modelo	CD4017 Counter
Tensão	5 a 15 V
Frequência Clock	2,5 a 5,5 MHz
Pulso	60 a 200 ns

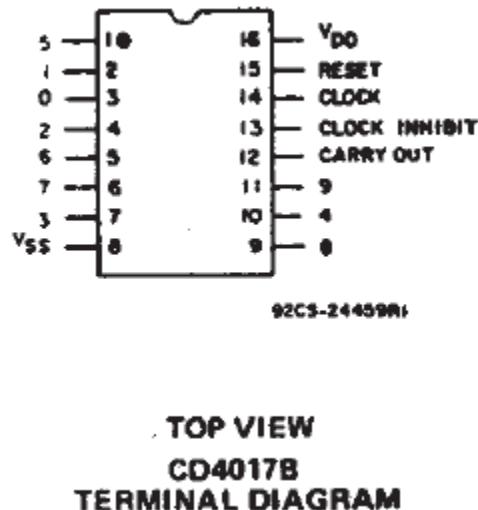


FIGURA 2 – PINAGEM CI CD4017
FONTE: TEXAS INSTRUMENTS, 2004

O contador CD4017 é um contador de década. Seus terminais, como mostra a Figura 2, fornecem sinais para os 9 dígitos (0 – 9). A depender do nível do sinal do oscilador LM555, ele emitirá ao Relé o sinal que acenderá ou apagará a lâmpada. Custo aproximado de: R\$ 1,50 cada.

f) Diodo retificador 1N4004

Fabricante	Vishay
Tensão reversa max. de pico	400 V
Tensão máx. eficaz	280 V
Tensão DC máx. de bloqueio	400 V
Retificação máx. de Corrente	1 A
Pico de corrente (onda senoidal)	30 A
Pico de corrente (onda quadrada)	45 A

Uma das aplicações do diodo é na retificação de corrente conduzindo-a para apenas um sentido e bloqueando o caminho reverso. Evitando danificar outros componentes. É esse intuito para o circuito. Custo aproximado de: R\$ 0,15 cada.

g) LED verde

Fabricante	Symtronic
Modelo	SYM-G503-30-D
Potência dissipada	60 mW
Corrente de pico	80 mA
Corrente de operação	15 a 20 mA

Utilizado nesse projeto para representar seu funcionamento. Custo aproximado de: R\$ 0,25 cada.

h) Microfone de Eletreto com 2 terminais

Sensibilidade	48 a 66 dB
Tensão de entrada	3 V
Tensão de operação	1,5 a 10 V
Consumo de corrente	0,5 mA
Pressão sonora	120 dB

Esse microfone é a porta de entrada do sinal da palma para acionamento do circuito. Custo aproximado de: R\$ 1,50 cada.

i) Bateria alcalina de dióxido de manganês 9 V

Tensão nominal	9 V
Impedância	1,7 mΩ
Terminais	Estalo miniatura

A bateria de 9 V é responsável por alimentar o circuito. Com exceção da lâmpada que é alimentada pela tensão da casa (tomada). Custo aproximado de: R\$ 5,00 cada.

j) Placa de Fenolite cobreada face simples 10 cm de largura por 10 cm de comprimento

A placa é a base onde construímos o circuito e soldamos os componentes. Custo aproximado de: R\$ 5,00 cada.

k) Relé 12 V

Fabricante	Metaltex
Modelo	AZ1RC2
Tensão nominal	12 V
Tensão de operação	acima de 9 V
Tensão de não operação	abaixo de 1,2 V
Corrente nominal	30 mA
Resistência	400 Ω

O Relé faz a conexão do circuito com a lâmpada mantendo as tensões do circuito com a da casa independentes. Quando recebe o sinal ele fecha a chave e aciona a lâmpada. Custo aproximado de: R\$ 4,00 cada.

l) Resistores:

Filme carbono: 1 kΩ; 10 kΩ; 100 kΩ

Serie	E24
Tolerância	5%
Dissipação nominal	0,5 W
Resistencia térmica	170 K/W
Tensão de operação máx.	200 V

Os resistores fazem o ajuste da corrente para o correto funcionamento e proteção dos componentes com ele conectados. Custo aproximado de: R\$ 0,15 cada.

Potenciômetro: 100 kΩ

Fabricante	Alpha
Serie	31VA
Tolerância	20%
Tensão máxima	500 V
Dissipação	0,5 W

Com o potenciômetro regulamos a intensidade da captação sonora pelo microfone. Custo aproximado de: R\$ 1,70 cada.

m) Soquete estampado para circuitos integrados

Neste projeto, utilizamos esses soquetes para encaixar os circuitos integrados LM555 e CD4017. Eles auxiliam na manutenção por deixar os componentes encaixados e sem a necessidade de soldar. Assim, no eventual defeito, basta retirar o componente encaixado. Custo aproximado para o de 8 pinos: R\$ 0,30 cada. Custo aproximado para o de 16 pinos: R\$ 0,40 cada.

n) Transistor BC548

Fabricante	Fairchild
Tensão coletor - base	50 V
Tensão coletor – emissor	30 V
Tensão emissor – base	5 V
Corrente coletor	100 mA
Dissipação coletor	500 mW



FIGURA 3 – DESENHO E TERMINAIS DO TRANSISTOR
FONTE: FAIRCHILD, 2014

Um transistor amplifica o sinal do microfone e envia para o LM555. O outro recebe o sinal da saída do CD4017 e amplifica a intensidade para acionar o Relé. Pela Figura 3, visualizamos os terminais deste componente. Custo aproximado de: R\$ 0,30 cada.

2.3.2 Confecção da placa de circuito impresso:

A fabricação da PCI, após terminado o *layout*, foi realizada na Universidade Positivo. Para isso, é necessário atender alguns requisitos conforme exposto no item 2.5 deste memorial. O valor para esse serviço foi de R\$ 10,00.

2.3.3 Equipamentos e ferramentas:

- a) Alicates de bico e de corte
 - b) Estanho para solda
 - c) Ferro para soldar
 - d) Fonte de tensão CC ajustável de 0 a 32 V (para testes)
 - e) *Jumper*
 - f) Matriz de contatos
 - g) Multímetro digital

2.4 DIAGRAMA ELÉTRICO DO CIRCUITO

As conexões entre os componentes estão dispostas conforme demonstra a Figura 4 abaixo:

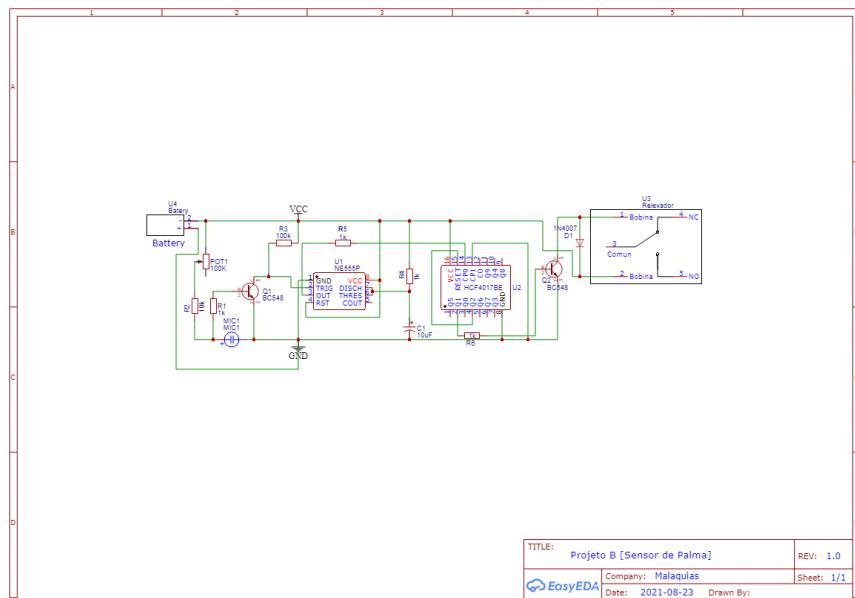


FIGURA 4 – ESQUEMA ELÉTRICO DO PROJETO
FONTE: OS AUTORES

2.5 LAYOUT DA PLACA DE CIRCUITO IMPRESSO

O layout final do circuito está demonstrado na Figura 5 abaixo:

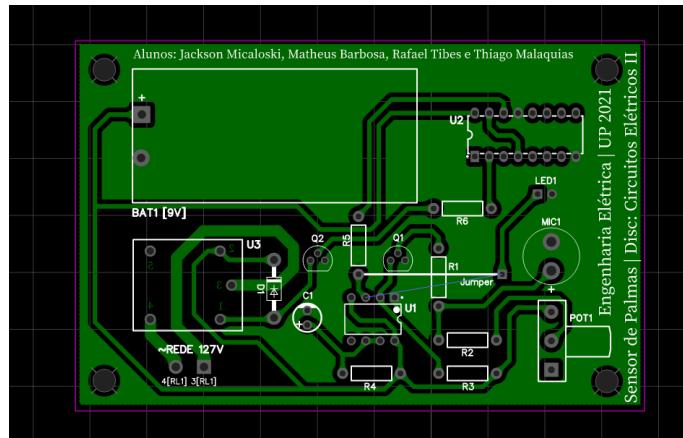


FIGURA 5 – LAYOUT DO PROJETO

FONTE: OS AUTORES

Para que fosse possível fabricar a PCI na Universidade, desenvolvemos, a pedido do fabricante, o *layout* no *software EasyEDA* e geramos o arquivo em formato *Gerber*. O tamanho máximo da utilização da placa não excede a 10 cm de largura por 10 cm de comprimento. O circuito todo foi preparado numa única face. Os furos, para os terminais dos componentes, são de 1 mm de diâmetro e as trilhas de 0,8 mm de espessura.

A Figura 6 é o resultado da placa com as trilhas elétricas e as furações para os terminais dos componentes.

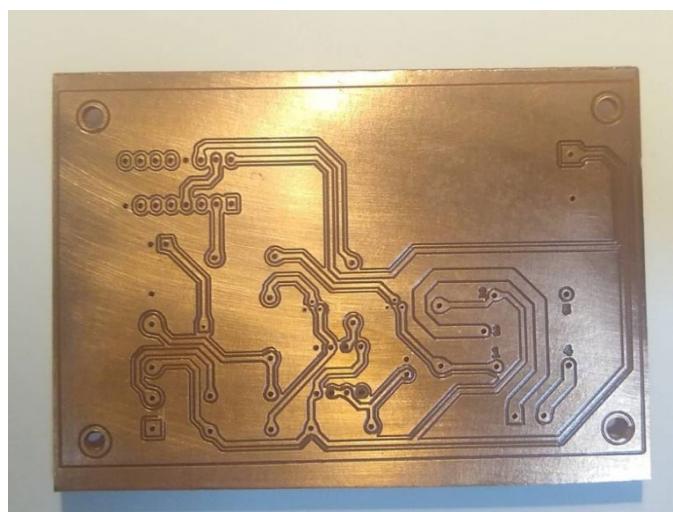


FIGURA 6 – PRODUÇÃO DA PCI

FONTE: OS AUTORES

2.6 MONTAGEM

A montagem dos componentes na placa está representado pela Figura 7. Nessa fase, posicionamos cada componente, em seu devido lugar, e soldamos na placa. Tomando os devidos cuidados com o ferro de solda, por sua elevada temperatura de trabalho, e com a fumaça tóxica gerada pelo estanho.



FIGURA 7 – MONTAGEM FINAL DO PROJETO
FONTE: OS AUTORES

Um dos integrantes do projeto, teve a oportunidade de projetar e imprimir, em uma impressora 3D, através do software *SolidWorks (2017)*, um “case” para a placa eletrônica. A Figura 8 demonstra como ficou a placa alocada neste “case”.

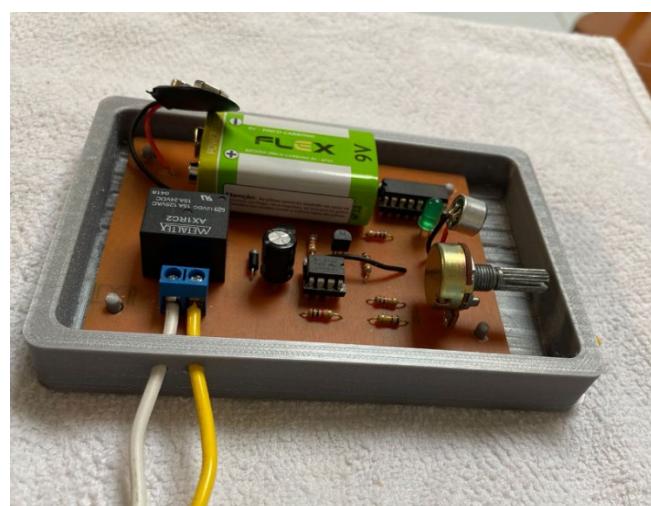


FIGURA 8 – CASE DO PROJETO
FONTE: OS AUTORES

2.7 CUSTOS

A Tabela 1 a seguir é um panorama geral dos custos com os componentes necessários para a execução do projeto. Estão fora do escopo dela as ferramentas necessárias, insumos, hora técnica, gastos de energia elétrica e logístico com transportes.

TABELA 1 – CUSTOS GERAIS PARA FABRICAÇÃO

Item	Componente	Quantidade	Custo unitário (R\$)	Custo total (R\$)
1	Borne	1	1,50	1,50
2	Capacitor	1	0,20	0,20
3	CI LM555	1	1,50	1,50
4	CI CD4017	1	1,50	1,50
5	Conektor bateria	1	2,50	2,50
6	Diodo	1	0,15	0,15
7	LED	1	0,25	0,25
8	Microfone	1	1,50	1,50
9	Bateria	1	5,00	5,00
10	Placa Fenolite	1	5,00	5,00
11	Relé	1	4,00	4,00
12	Resistor 1 kΩ	4	0,15	0,60
13	Resistor 10 kΩ	1	0,15	0,15
14	Resistor 100 kΩ	1	0,15	0,15
15	Potenciômetro 100 kΩ	1	1,70	1,70
16	Soquete 8 pinos	1	0,30	0,30
17	Soquete 16 pinos	1	0,40	0,40
18	Transistor	2	0,30	0,60
19	Fabricação (UP)	1	10,00	10,00
TOTAL:		23	36,25	37,00

FONTE: OS AUTORES

3 CONSIDERAÇÕES FINAIS

Inicialmente, pesquisamos e escolhemos o circuito, nos reunimos e montamos ele na matriz de contato aplicando os conceitos adquiridos no curso até o momento de forma prática e, consequentemente, verificando a funcionalidade do nosso projeto. Realizamos duas montagens do mesmo circuito em *protoboards* diferentes. O que havíamos escolhido tinha como finalidade, ao detectar uma frequência sonora próxima ao microfone, acender a lâmpada ligada através do relé e apagá-la segundos depois. O circuito também tinha um LED que indicava o funcionamento sem a necessidade de conectar a lâmpada. Quando realizamos os testes, o LED acionava e, após alguns instantes de tempo (variação devida a capacidade do capacitor utilizado), se apagava. Embora o circuito seja funcional, concluímos que não tinha tanto apelo comercial para uma fabricação em massa, porque entendemos que os futuros compradores teriam interesse em também desligar a lâmpada da mesma forma como a ligaram.

Por isso, resolvemos procurar outro circuito que o usuário pudesse controlar o desligamento da lâmpada, no momento que desejasse, não dependendo do capacitor. Encontramos um novo circuito, o qual atendia nosso objetivo, com bastante similaridade ao primeiro e a adição principal de um novo componente, o circuito integrado CD4017.

Com os componentes do segundo circuito, executamos os testes montando na *protoboard* e obtivemos o resultado esperado. Então, partimos para a elaboração do *layout* da PCI. Como aderimos à indicação do professor Jackson Milano para a fabricação, entramos em contato com a Universidade Positivo. Conforme solicitado, fizemos o *layout* no software *EasyEDA* e atendemos aos requisitos técnicos para a fabricação. Fazer o roteamento das trilhas, otimizando cada espaço e sem cruzar as linhas por causa da placa ser em uma única camada, se mostraram um grande desafio. Após várias tentativas, conseguimos aperfeiçoar o desenho e deixá-lo com apenas um *jumper* de conexão. Finalizamos gerando o arquivo *Gerber* e enviamos para a universidade. A produção levou apenas dois dias.

Após o recebimento da placa impressa, iniciamos a montagem dos componentes. A montagem exigiu muitos dos conceitos aprendidos na aula de Laboratório do primeiro semestre do curso de Engenharia Elétrica, matéria ministrada pelo professor Jackson Milano, onde foi necessário a realização dos processos de soldagem em circuitos impressos. Conseguimos fazer a montagem sem maiores problemas. Encaixamos os componentes e soldamos na placa. Ao fim, testamos novamente e alcançamos o resultado positivo na montagem.

Com poucos elementos já é possível iniciar projetos simples de eletrônica. Esse simples não significa fácil ou rápido de fazer, talvez não para a eletrônica. Exige tempo e dedicação. São muitas etapas a serem realizadas. Neste projeto tivemos a experiência de construir do zero um circuito. Essa experiência foi muito importante para o estudo destes acadêmicos de engenharia. A aprendizagem foi enorme. Houveram muitos momentos que comprovamos os conhecimentos e outros de busca de informação para passar o obstáculo. A nossa percepção é de que ainda temos muito caminho pela frente, muito o que estudar e aprender. Começamos a olhar diferente uma placa eletrônica, agora imaginando a forma como foi construída, a complexidade, o roteamento, as camadas, os testes, o desenvolvimento. Experimentos como esse ficam gravados no acervo pessoal do conhecimento e da experiência do aluno.

REFERÊNCIAS

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FAIRCHILD. BC546, BC547, BC548, BC549, BC550 - NPN Epitaxial Silicon Transistor. 2014. Disponível em: <<https://www.mouser.com/datasheet/2/149/BC547-190204.pdf>>. Acesso em: 16 set. 2021.

ANEXO A – DATASHEET LM555

 Product Folder Sample & Try Technical Documents Tools & Software Support & Community

LM555
SNAS514D – FEBRUARY 2000–REVISED JANUARY 2015

1 Features

- Direct Replacement for SE555/NE555
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- Output Can Source or Sink 200 mA
- Output and Supply TTL Compatible
- Temperature Stability Better than 0.005% per °C
- Normally On and Normally Off Output
- Available in 8-pin VSSOP Package

2 Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Linear Ramp Generator

3 Description

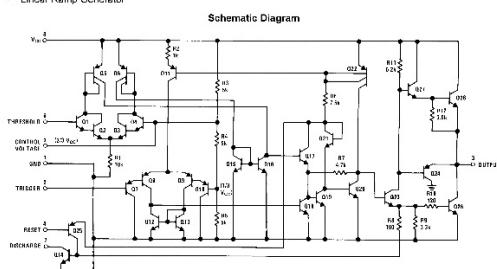
The LM555 is a highly stable device for generating accurate time delays, timing intervals, oscillations, and pulse trains. It provides for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and amplitude are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM555	SOIC (8) PCP ⁽²⁾ (8) VSSOP ⁽³⁾ (8)	4.00 mm × 3.97 mm 8.81 mm × 8.35 mm 3.00 mm × 3.00 mm

(1) For all available packages, see the orderable section at the end of the datasheet.

Schematic Diagram



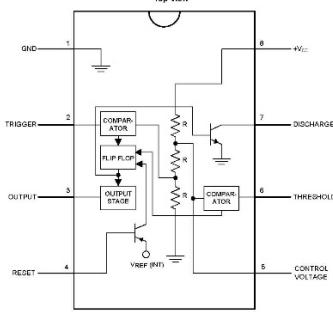
4 Revision History

Changes from Revision C (March 2013) to Revision D	Page
• Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	13

5 Pin Configuration and Functions

D, P, and DCK Packages
8-Pin PDIP, SOIC, and VSSOP
Top View



Pin Functions

PIN NO.	NAME	I/O	DESCRIPTION
5	Control Voltage	I	Controls the threshold and trigger levels. It determines the pulse width of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform.
7	DISCHARGE	I	Open collector output which discharges a capacitor between intervals in phase with output.
1	GND	O	Ground reference voltage.
3	Output	O	Output driven waveform.
4	RESET	I	High level pulse applied to this pin to disable or reset the timer. When not used for reset, this pin should be connected to VCC to avoid false triggering.
6	Threshold	I	Compares the voltage applied to this terminal with a reference voltage of 20 mV. The amplitude of voltage applied to this terminal is responsible for the set state of the flip-flop.
2	Trigger	I	Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin.
8	V ⁽⁴⁾	I	Supply voltage with respect to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

	MIN	MAX	UNIT	
Power Dissipation ⁽¹⁾	LM555CM, LM555CN ⁽⁴⁾ :	1.80	mW	
	LM555P:	1.00	mW	
Soldering ⁽²⁾	PCP Package	280	°C	
Information	Small Outline Packages (SOIC and VSSOP)	210	°C	
	Infrared (15 Seconds)	220	°C	
Storage temperature, T _{STG}		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated. Recommended Operating Conditions: Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) 200°C maximum soldering temperature for 10 seconds. See the Soldering Techniques section for detailed information.

(3) For operating at elevated temperatures the device must be derated above 20°C based on a 150°C maximum junction temperature and a thermal resistance of 108°C/W (PCP), 17°C/W (SOIC), and 204°C/W (VSSOP) junction to ambient.

(4) Refer to RE-1555X drawing of military LM555 and LM555U versions for specifications.

6.2 ESD Ratings

V _{L(A)} ⁽¹⁾	Electrostatic discharge (Human-body mode) (HBM) per ANSI/ESD/ESD-TR-001 ⁽¹⁾⁽²⁾	VALUE	UNIT
		±500	V

(1) JEDEC document JEP-155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) The ESD information listed is for the SOIC package.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Supply Voltage	MIN	MAX	UNIT
Temperature, T _A	0	70	°C
Operating junction temperature, T _J	70		°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM555			
	8 PINS	SOIC	VSSOP	UNIT	
R _{θJA}		106	176	204	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRRA855.

FIGURA 9 – DATASHEET LM555 – PARTE 1
FONTE: TEXAS INSTRUMENTS, 2015



LM555
SNAS54BD – FEBRUARY 2000 – REVISED JANUARY 2015

6.5 Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC} = 5 \text{ V}$, $R_1 = \infty$	4.5	16	16	V
Supply Current	$V_{CC} = 15 \text{ V}$, $R_1 = \infty$ (Low State) ⁽²⁾	3	6		
		10	15		mA
Timing Error, Monostable					
Initial Accuracy		1%			
Drift with Temperature	$R_1 = 1 \text{ k}\Omega$ to $100 \text{ k}\Omega$, $C = 0.1 \mu\text{F}$ ⁽⁴⁾	50			ppm/ $^{\circ}\text{C}$
Accuracy over Temperature		1.5%			
Drift with Supply		0.1%			V
Timing Error, Astable		2.25			
Initial Accuracy		2.25			
Drift with Temperature	$R_1, R_2 = 1 \text{ k}\Omega$ to $100 \text{ k}\Omega$, $C = 0.1 \mu\text{F}$ ⁽⁴⁾	150			ppm/ $^{\circ}\text{C}$
Accuracy over Temperature		3.0%			
Drift with Supply		0.20%			%
Threshold Voltage		0.657			V_{CC}
Trigger Voltage	$V_{CC} = 15 \text{ V}$	1			V
Trigger Current	$V_{CC} = 5 \text{ V}$	1.87			V
Reset Voltage		0.4	0.5	0.9	μA
Reset Current		0.1	0.4	0.6	mA
Threshold Current	$I_{OL} = 10 \text{ mA}$	0.1	0.25	0.5	μA
Control Voltage Level	$V_{CC} = 15 \text{ V}$	9	10	11	V
	$V_{CC} = 5 \text{ V}$	2.6	3.33	4	V
Pin 7 Leakage Output High		1	100		nA
Pin 7 Sat. ⁽⁵⁾					
Output Low	$V_{CC} = 15 \text{ V}$, $I_1 = 15 \text{ mA}$	150			mV
Output Low	$V_{CC} = 4.5 \text{ V}$, $I_1 = 4.5 \text{ mA}$	50	200		mV
Output Voltage Drop (Low)	$V_{CC} = 15 \text{ V}$				
	$I_{OL} = 10 \text{ mA}$	0.1	0.25	0.5	V
	$I_{OL} = 50 \text{ mA}$	0.4	0.75	1.0	V
	$I_{OL} = 100 \text{ mA}$	2	2.5	3.0	V
	$I_{OL} = 200 \text{ mA}$	2.5			V
	$V_{CC} = 5 \text{ V}$				
	$I_{OL} = 5 \text{ mA}$	0.25	0.35	0.5	V
	$I_{OL} = 1 \text{ mA}$				V

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions are those conditions under which the device is intended to operate. Electrical Characteristics are given under particular test conditions which ensures specific performance limits. This assumes that the device is within the Recommended Operating Conditions. Specifications are not ensured for parameters where no limit is given; however, the typical value is a guaranteed specification.
- (3) Supply current when output high typically 1 mA less at $V_{CC} = 5 \text{ V}$.
- (4) Tested between 25° and 125° C.
- (5) Total current determined by maximum value of $R_1 + R_2$ for 15 V operation. The maximum total ($R_1 + R_2$) is 20 MΩ.
- (6) No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

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Electrical Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage Drip (High)	$I_{OL} = 200 \text{ mA}$, $V_{CC} = 15 \text{ V}$	12.75	13.3	16	V
	$I_{OL} = 100 \text{ mA}$, $V_{CC} = 15 \text{ V}$	12.75	13.3	16	V
	$V_{CC} = 5 \text{ V}$	2.75	3.3	4	V

6.6 Typical Characteristics

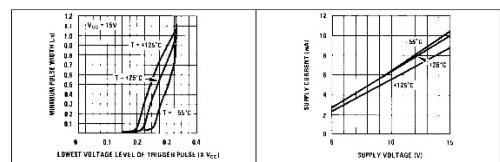


Figure 1. Minimum Pulse Width Required For Triggering

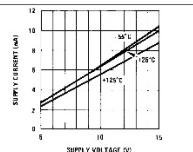


Figure 2. Supply Current vs. Supply Voltage

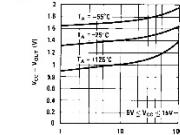


Figure 3. High Output Voltage vs. Output Source Current

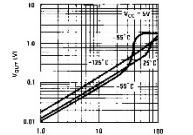


Figure 4. Low Output Voltage vs. Output Sink Current

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6. Substrate Connection Procedure Copyright © 2000–2015, Texas Instruments Incorporated Product Folder Links: LM555



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Typical Characteristics (continued)

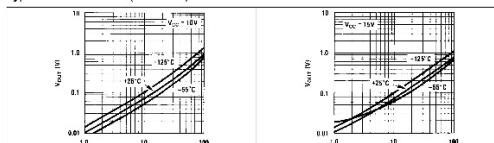


Figure 5. Low Output Voltage vs. Output Sink Current

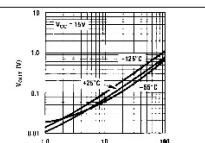


Figure 6. Low Output Voltage vs. Output Sink Current

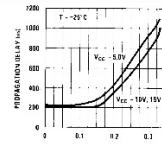


Figure 7. Output Propagation Delay vs. Voltage Level of Trigger Pulse

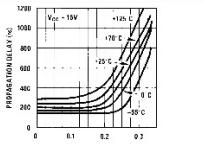


Figure 8. Output Propagation Delay vs. Voltage Level of Trigger Pulse

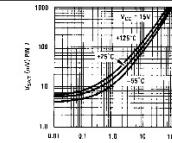


Figure 9. Discharge Transistor (Pin 7) Voltage vs. Sink Current

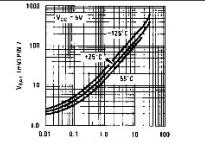


Figure 10. Discharge Transistor (Pin 7) Voltage vs. Sink Current

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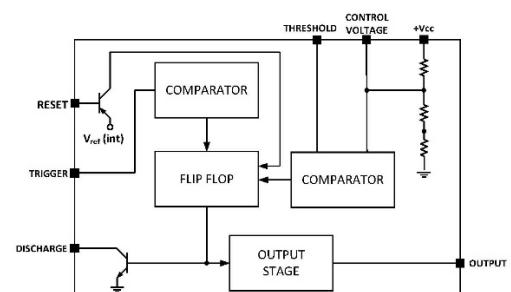
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7. Detailed Description

7.1 Overview

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the timer is triggered controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits. The LM555 are available in 8-pin PDIP, SOIC, and VSSOP packages and is a direct replacement for SE555/NE555.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Direct Replacement for SE555/NE555

The LM555 timer is a direct replacement for SE555 and NE555. It is pin-to-pin compatible so that no schematic or layout changes are necessary. The LM555 come in an 8-pin PDIP, SOIC, and VSSOP package.

7.3.2 Timing From Microseconds Through Hours

The LM555 has the ability to have timing parameters from the microseconds range to hours. The time delay of the system can be determined by the time constant of the R and C value used for either the monostable or astable configuration. A nomograph is available for easy determination of R and C values for various time delays.

7.3.3 Operates in Both Astable and Monostable Mode

The LM555 can operate in both astable and monostable mode depending on the application requirements.

• Monostable mode: The LM555 timer acts as a "one-shot" pulse generator. The pulse begins when the LM555 timer receives a signal at the trigger input that falls below a 1/3 of the voltage supply. The width of the output pulse is determined by the time constant of an RC network. The output pulse ends when the voltage on the

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FIGURA 10 – DATASHEET LM555 – PARTE 2
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Feature Description (continued)

- capacitor equals $2/3$ of the supply voltage. The output pulse width can be extended or shortened depending on the application by adjusting the R and C values.
- Astable (free-running) mode: The LM555 timer can operate as an oscillator and puts out a continuous stream of rectangular pulses having a specified frequency. The frequency of the pulse stream depends on the values of R_A , R_B , and C.

7.4 Device Functional Modes

7.4.1 Monostable Operation

In this mode of operation the timer functions as a one-shot [Figure 11]. The external capacitor is initially held discharged until a trigger pulse is applied to pin 2. Upon application of a negative trigger pulse of less than $1/3 V_{CC}$ to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

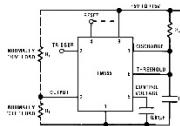


Figure 11. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1 R_C$, at the end of which time the output voltage reaches $2/3 V_{CC}$. The comparator then makes the flip-flop which then discharges the capacitor and drives the output to its low state. Figure 12 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.

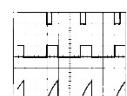


Figure 12. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least $10 \mu s$ before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, TI recommends connecting the Reset pin to V_{CC} to avoid any possibility of false triggering.

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Device Functional Modes (continued)

Figure 13 is a nomograph for easy determination of R, C values for various time delays.

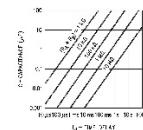


Figure 13. Time Delay

7.4.2 Astable Operation

If the circuit is connected as shown in Figure 14 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_x and R_B and discharges through R_B . Thus the duty cycle may be precisely set by the ratio of the two resistors.

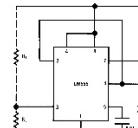


Figure 14. Astable

In this mode of operation, the capacitor charges and discharges between $1/3 V_{CC}$ and $2/3 V_{CC}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 15 shows the waveforms generated in this mode of operation.

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Device Functional Modes (continued)

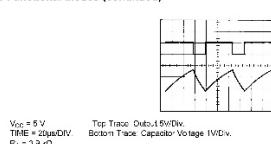


Figure 15. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693 (R_x + R_y) C \quad (1)$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_y) C \quad (2)$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693 (R_x + 2R_y) C \quad (3)$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1}{0.693 (R_x + 2R_y) C} \quad (4)$$

Figure 16 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{t_1}{T} = \frac{R_x}{R_x + 2R_y} \quad (5)$$

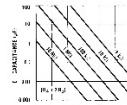


Figure 16. Free Running Frequency

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM555 timer can be used in a various configurations, but the most commonly used configuration is in monostable mode. A typical application for the LM555 timer in monostable mode is shown on an LED for a specific time duration. A pushbutton is used as the trigger to output a high pulse when trigger pin is pulsed low. This simple application can be modified to fit any application requirement.

8.2 Typical Application

Figure 17 shows the schematic of the LM555 that flashes an LED in monostable mode.

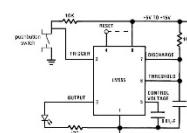


Figure 17. Schematic of Monostable Mode to Flash an LED

8.2.1 Design Requirements

The main design requirement for this application requires calculating the duration of time for which the output stays high. The duration of time is dependent on the R and C values (as shown in Figure 17) and can be calculated by:

$$t = 1.1 \times R \times C \text{ seconds} \quad (6)$$

8.2.2 Detailed Design Procedure

To allow the LED to flash on for a noticeable amount of time, a 5 second time delay was chosen for this application. By using Equation 6, RC equals 4.545. If R is selected as $100 k\Omega$, $C = 45.4 \mu F$. The values of $R = 100 k\Omega$ and $C = 47 \mu F$ were selected based on standard values of resistors and capacitors. A momentary push button with a series diode to ground is connected to the trigger input with a 10-k Ω current limiting resistor pulled to the supply voltage. When the push button is pressed, the trigger pin goes to GND. An LED is connected to the output pin with a current limiting resistor in series from the output of the LM555 to GND. The reset pin is not used and was connected to the supply voltage.

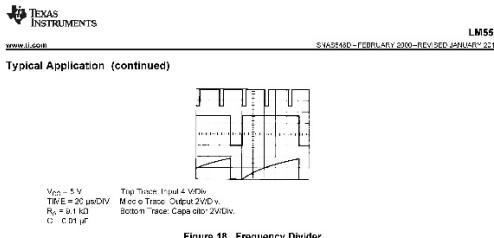
8.2.2.1 Frequency Divider

The monostable circuit of Figure 11 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 18 shows the waveforms generated in a divide by three circuit.

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FIGURA 11 – DATASHEET LM555 – PARTE 3
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8.2.2 Additional Information

Lower comparator storage time can be as long as 10 μ s when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 μ s minimum. Delay time reset to output is 0.47 μ s typical. Minimum reset pulse width must be 0.3 μ s typical. Pin 7 current switches within 30 ns of the output (pin 3) voltage.

8.2.3 Application Curves

The data shown below was collected with the circuit used in the typical applications section. The LM555 was configured in the monostable mode with a time delay of 5.17 s. The waveforms correspond to:

- Top Waveform (Yellow) – Capacitor voltage
- Middle Waveform (Green) – Trigger
- Bottom Waveform (Purple) – Output

As the trigger pin pulses high, the capacitor voltage starts charging and the output goes high. The output goes low as soon as the capacitor voltage reaches 2/3 of the supply voltage, which is the time delay set by the R and C value. For this example, the time delay is 5.17 s.



9 Power Supply Recommendations

The LM555 requires a voltage supply within 4.5 V to 16 V. Adequate power supply bypassing is necessary to protect associated circuitry. The minimum recommended capacitor value is 0.1 μ F in parallel with a 1- μ F electrolytic capacitor. Place the bypass capacitors as close as possible to the LM555 and minimize the trace length.

10 Layout

10.1 Layout Guidelines

Standard PCB rules apply to routing the LM555. The 0.1- μ F capacitor in parallel with a 1- μ F electrolytic capacitor should be as close as possible to the LM555. The capacitor used for the time delay should also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

Figure 20 is the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01- μ F bypass capacitor for control voltage pin
- C3 – 0.1- μ F bypass ceramic capacitor
- C4 – 1- μ F electrolytic bypass capacitor
- R1 – based on time delay calculations
- U1 – LM555

10.2 Layout Example

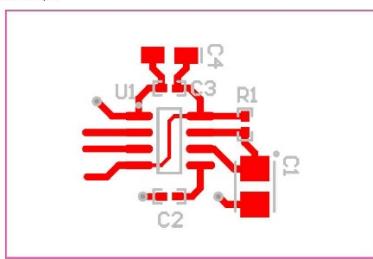


Figure 20. Layout Example



11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLY2022 — TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

FIGURA 12 – DATASHEET LM555 – PARTE 4
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PACKAGE OPTION ADDENDUM

11-Jan-2021

PACKAGING INFORMATION

Orderable Device	Status (¹⁰)	Package Type	Package Drawing	Pin	Package Qty ¹¹	Eco Plan (¹²)	Lead finish/ Ball material (¹³)	MSL Peak Temp (¹⁴)	Op Temp (°C)	Device Marking (^{14a})	Samples
LM555CN	NRND	SOIC	D	8	96	Non-RoHS & Green	Call TI	Call TI	0 to 70	LM555CN	
LM555CM/NOPB	ACTIVE	SOIC	D	8	96	RoHS & Green	SN	Level I-250C-UNLIM	0 to 70	LM555CN	Samples
LM555CM	NRND	VSSOP	DGK	8	1000	Non-RoHS & Green	Call TI	Call TI	0 to 70	ZSS	
LM555CM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level I-250C-UNLIM	0 to 70	ZSS	Samples
LM555CMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level I-250C-UNLIM	0 to 70	ZSS	Samples
LM555CMX	NRND	SOIC	D	8	2500	Non-RoHS & Green	Call TI	Call TI	0 to 70	LM555CN	
LM555CN/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level I-250C-UNLIM	0 to 70	LM555CN	Samples
LM555CN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	Call TI SN	Level I-NA-UNLIM	0 to 70	LM555CN	Samples

¹⁰The marking status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not yet productive. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

¹¹RoHS: TI defines "RoHS" to mean semi-board products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. While designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may refer to these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) base flame retardants meet IEC60950 low halogen requirements of <1000ppm. Arsenic trioxide based flame retardants must also meet >1000ppm threshold requirement.

¹²MSL, Peak Temp. - The Moltke Solderability Level rating according to the JEDEC industry standard classifications, and peak solder temperature.¹³There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category of the device.

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PACKAGE OPTION ADDENDUM

11-Jan-2021

¹⁴Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indicated then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.¹⁵Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the material value exceeds the maximum column width.

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FIGURA 13 – DATASHEET LM555 – PARTE 5
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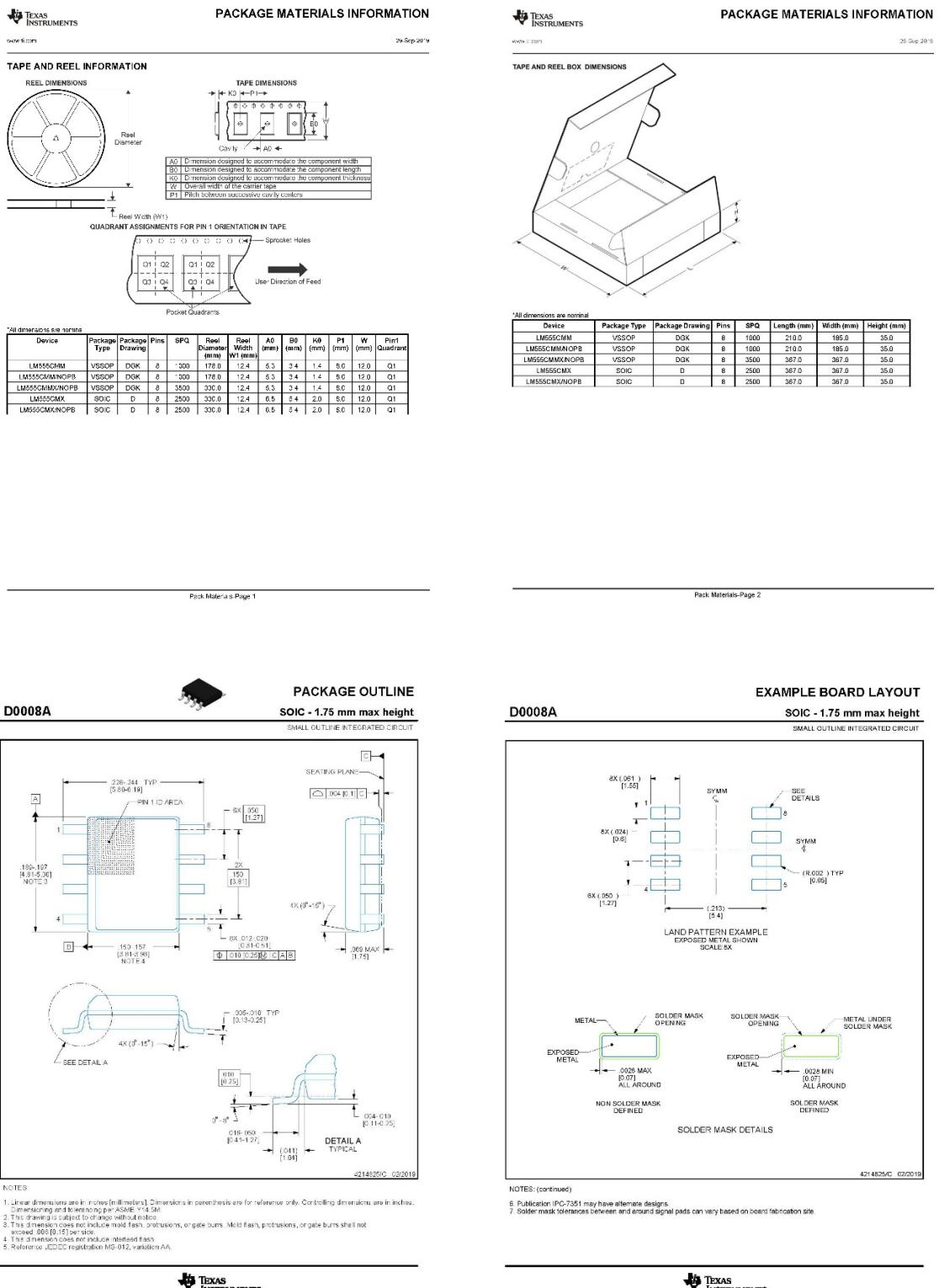


FIGURA 14 – DATASHEET LM555 – PARTE 6
FONTE: TEXAS INSTRUMENTS, 2015

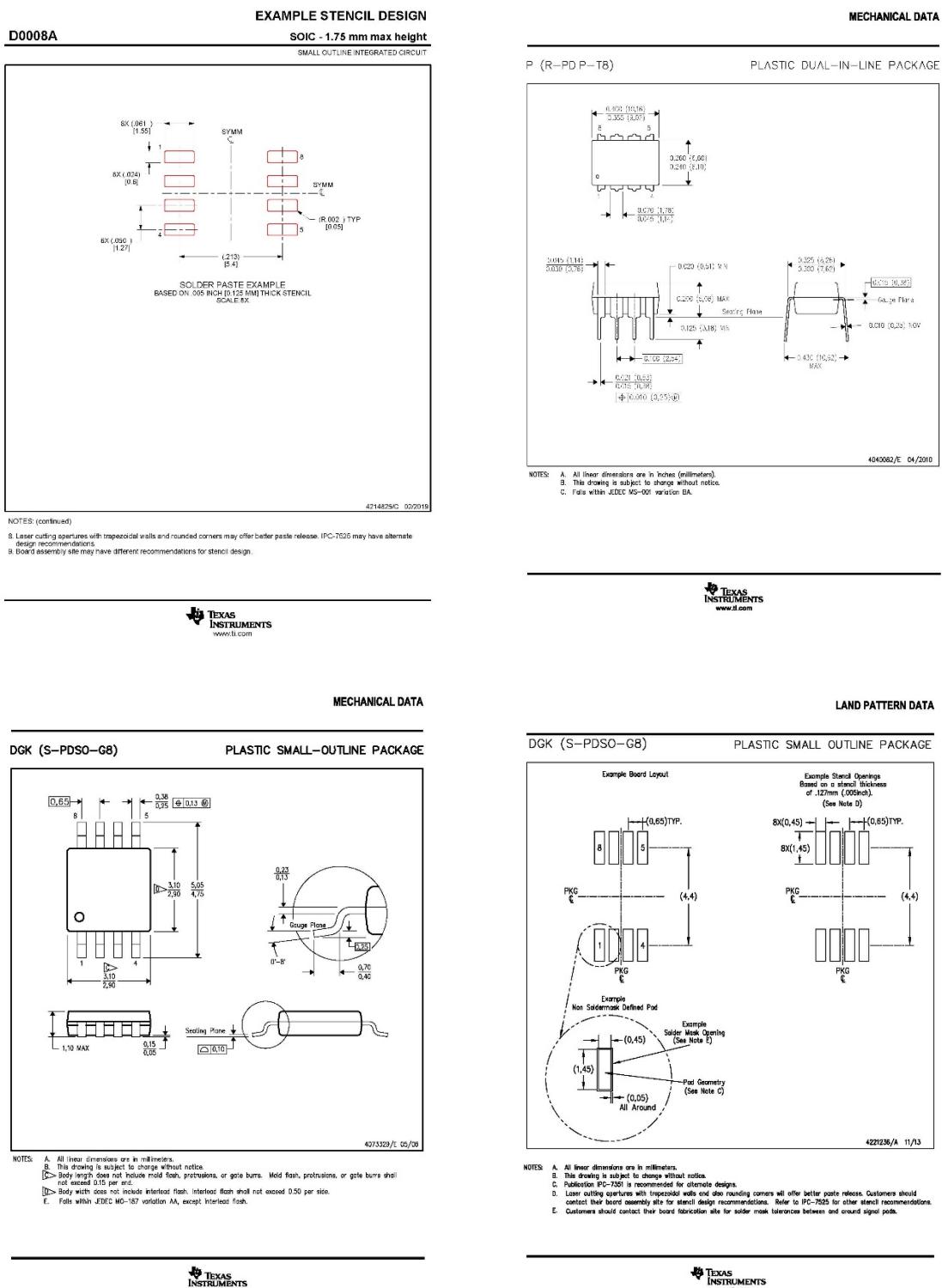


FIGURA 15 – DATASHEET LM555 – PARTE 7
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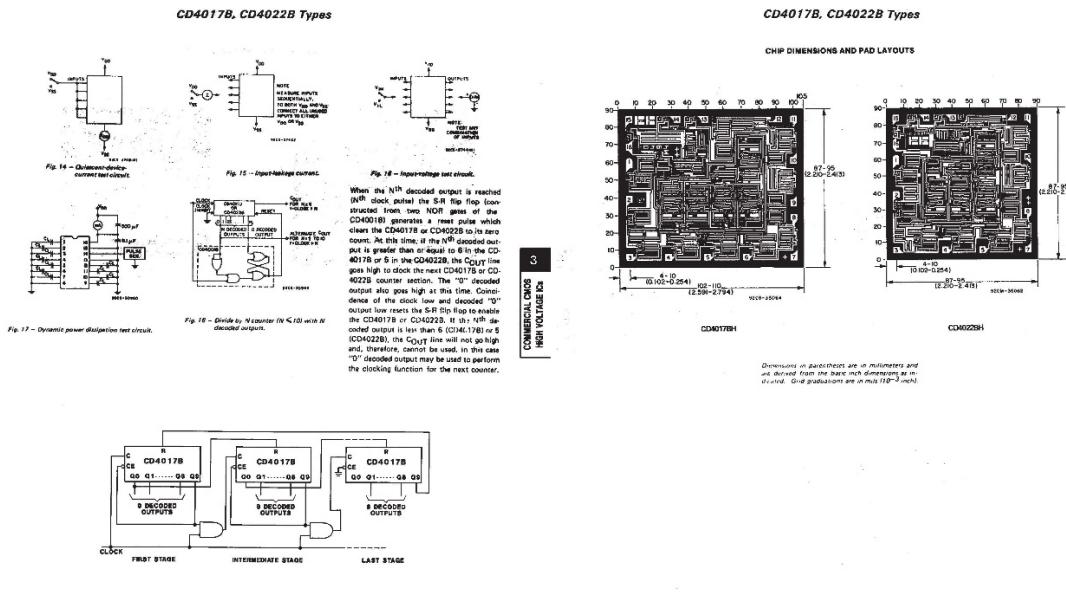
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FIGURA 16 – DATASHEET LM555 – PARTE 8
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Da Figura 9 a Figura 16, com tamanho reduzido em virtude da grandeza de informações e por se tratar de uma referência neste anexo, reunimos todas as 27 páginas do *datasheet* disponibilizado pelo fabricante em oito partes.



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FIGURA 18 – DATASHEET CD4017 – PARTE 2
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PACKAGE OPTION ADDENDUM

14-Aug-2021

Orderable Device	Status (¹)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (²)	Lead finish/ Ball material (³)	MSL Peak Temp (³)	Op Temp (°C)	Device Marking (⁴ / ⁵)	Samples
CD4022BPWR	ACTIVE	TSSOP	P/W	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM022B	Samples
CD4022PWRG4	ACTIVE	TSSOP	P/W	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM022B	Samples
JM38510/05651BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05651BEA	Samples
M38510/05651BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05651BEA	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a ";" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.⁽⁶⁾ Lead/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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PACKAGE OPTION ADDENDUM

14-Aug-2021

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4017B, CD4017B-MIL, CD4022B, CD4022B-MIL :

• Catalog : CD4017B, CD4022B

• Military : CD4017B-MIL, CD4022B-MIL

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

Addendum-Page 3

FIGURA 19 – DATASHEET CD4017 – PARTE 3
FONTE: TEXAS INSTRUMENTS, 2004

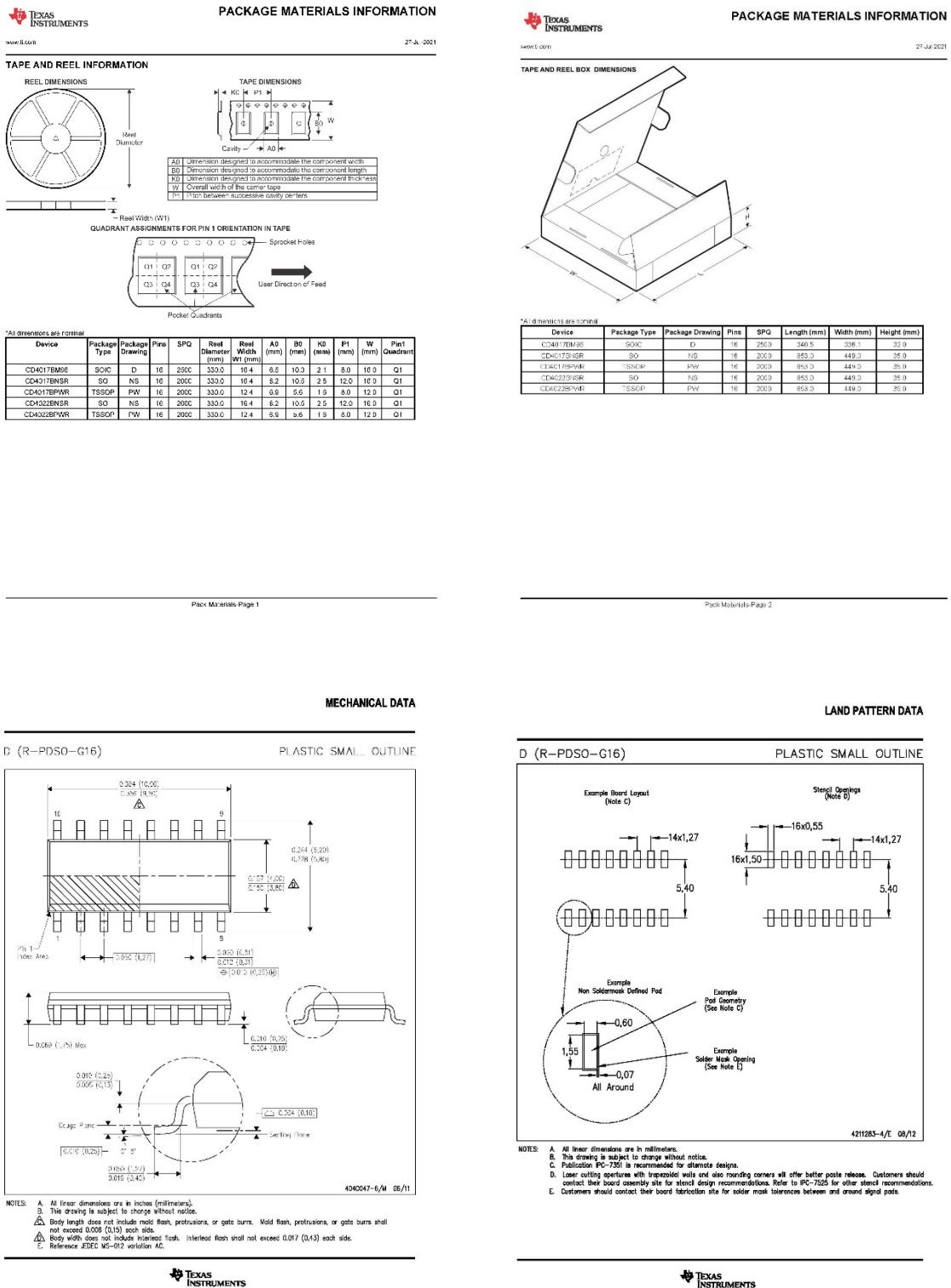


FIGURA 20 – DATASHEET CD4017 – PARTE 4
FONTE: TEXAS INSTRUMENTS, 2004

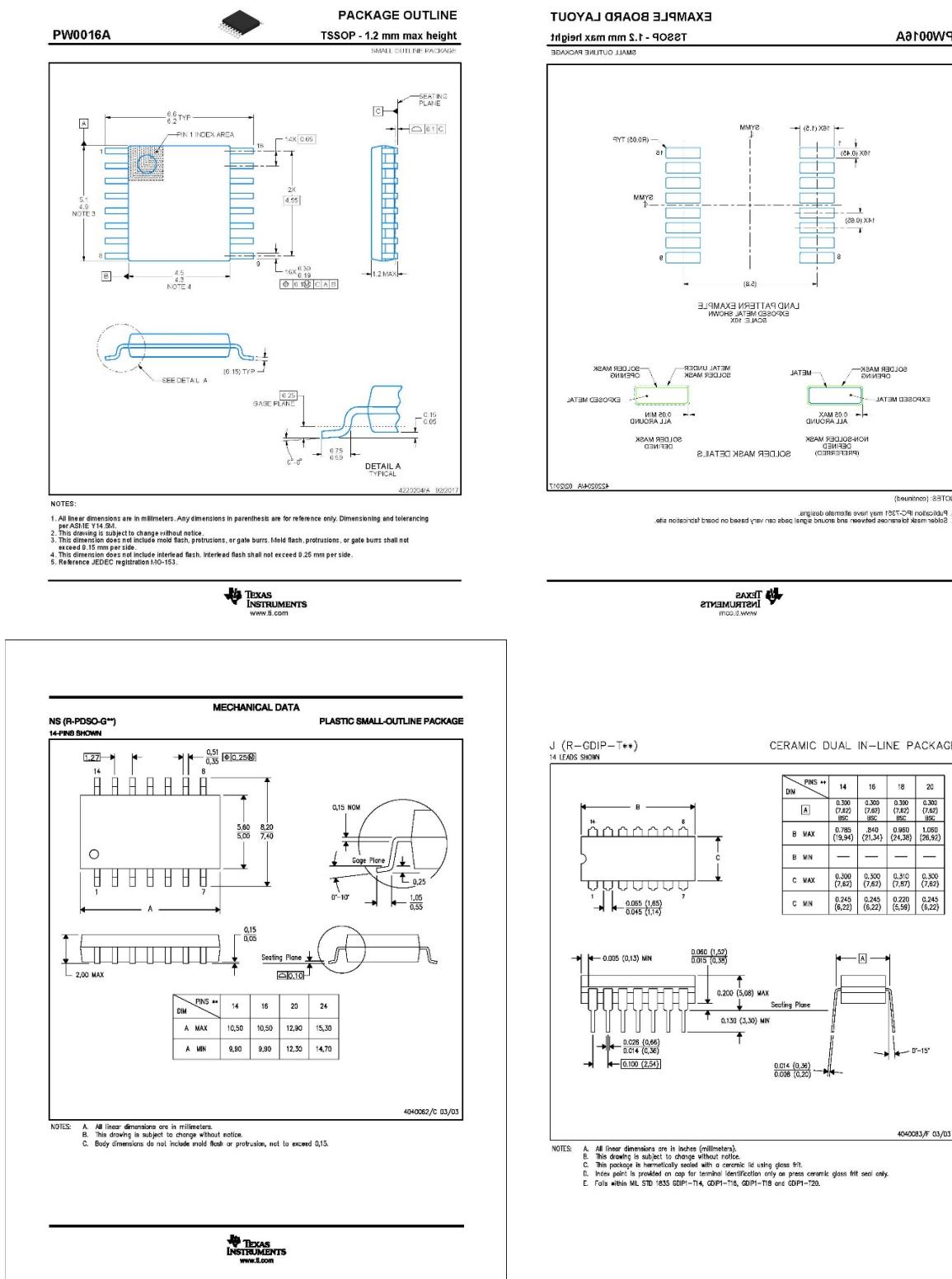


FIGURA 21 – DATASHEET CD4017 – PARTE 5
FONTE: TEXAS INSTRUMENTS, 2004

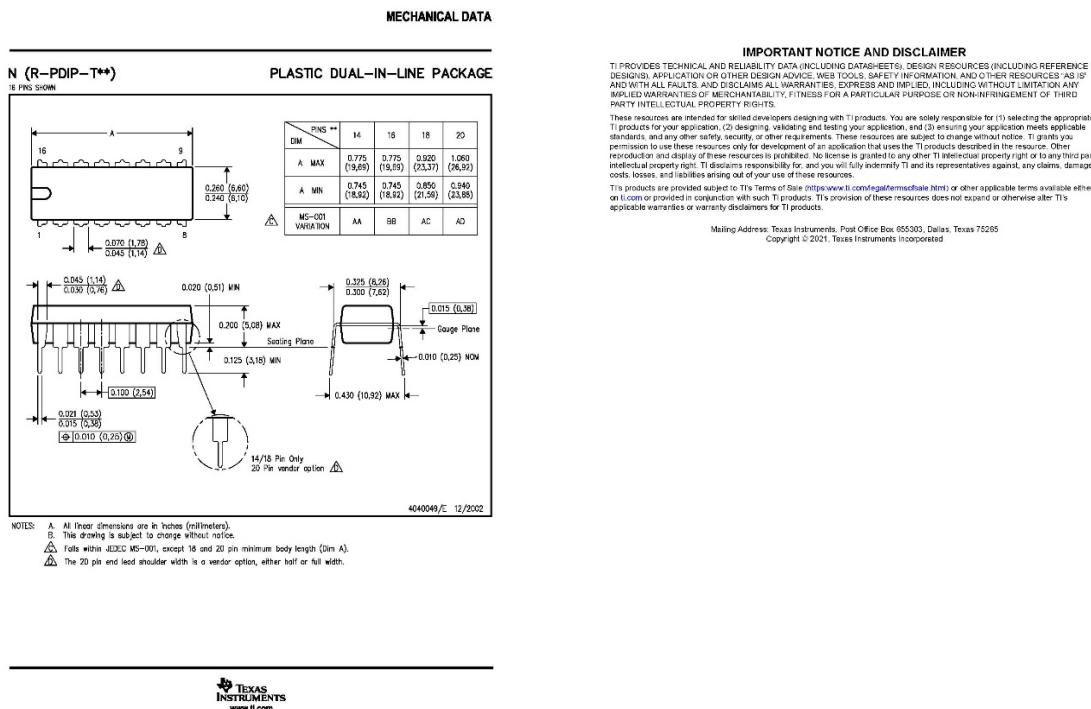


FIGURA 22 – DATASHEET CD4017 – PARTE 6
FONTE: TEXAS INSTRUMENTS, 2004

Reunimos em seis partes, Figura 17 a Figura 22, novamente em tamanho reduzido, as 20 páginas do *datasheet* do contador CD4017.