

Relatório 03 - Laboratório de Arquitetura de Computadores

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28 de fevereiro de 2019

Figura 1: ALU de 4 bits

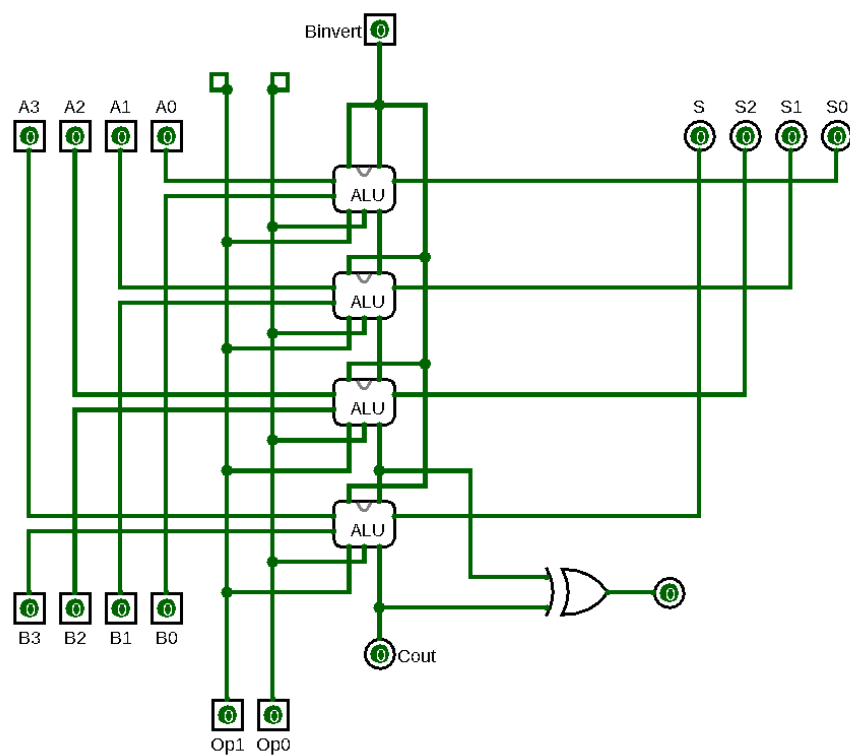


Figura 2: ALU de 1 bit

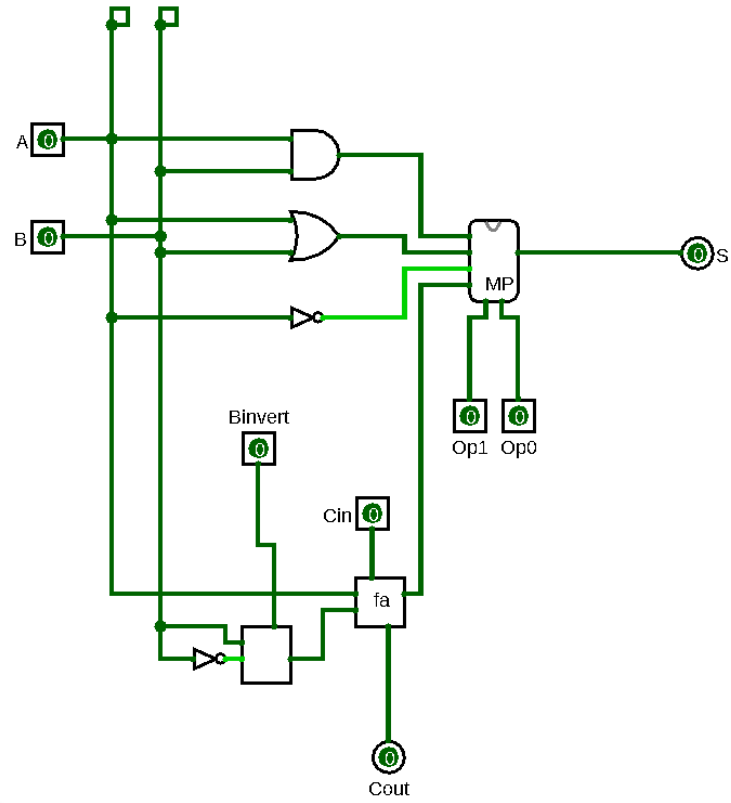


Figura 3: Multiplexador 4x1

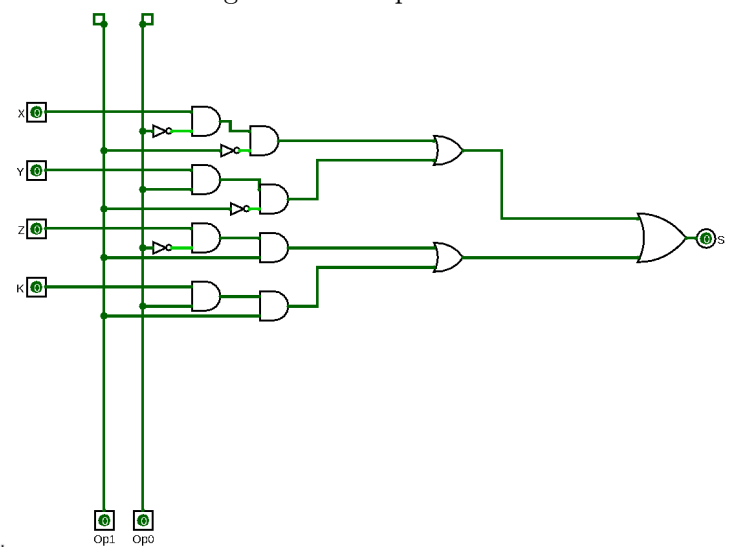


Figura 4: Multiplexador 2x1

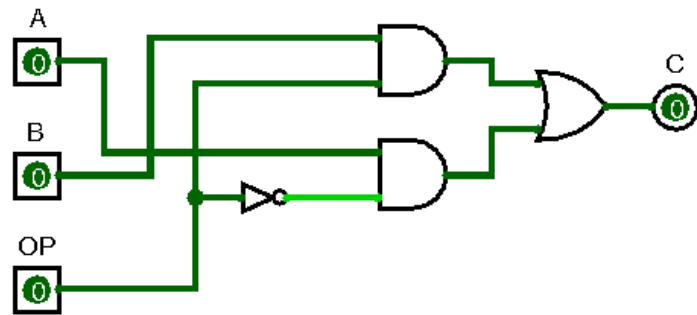


Figura 5: Full adder

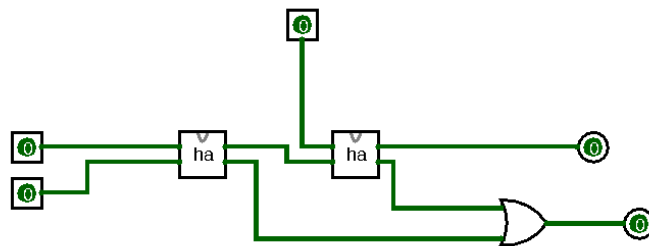


Figura 6: Half adder

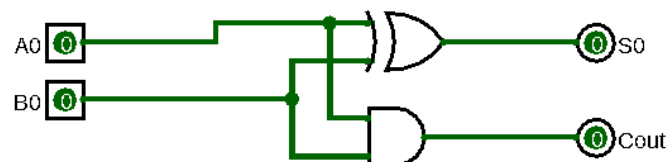


Figura 7: Parte 2 - and(a,b)

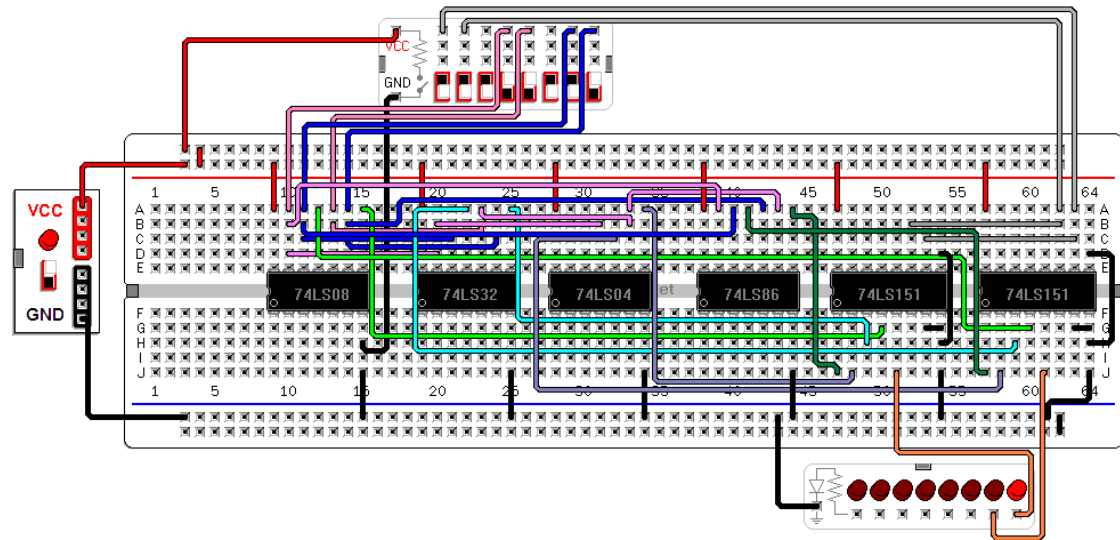


Figura 8: Parte 2 - or(a,b)

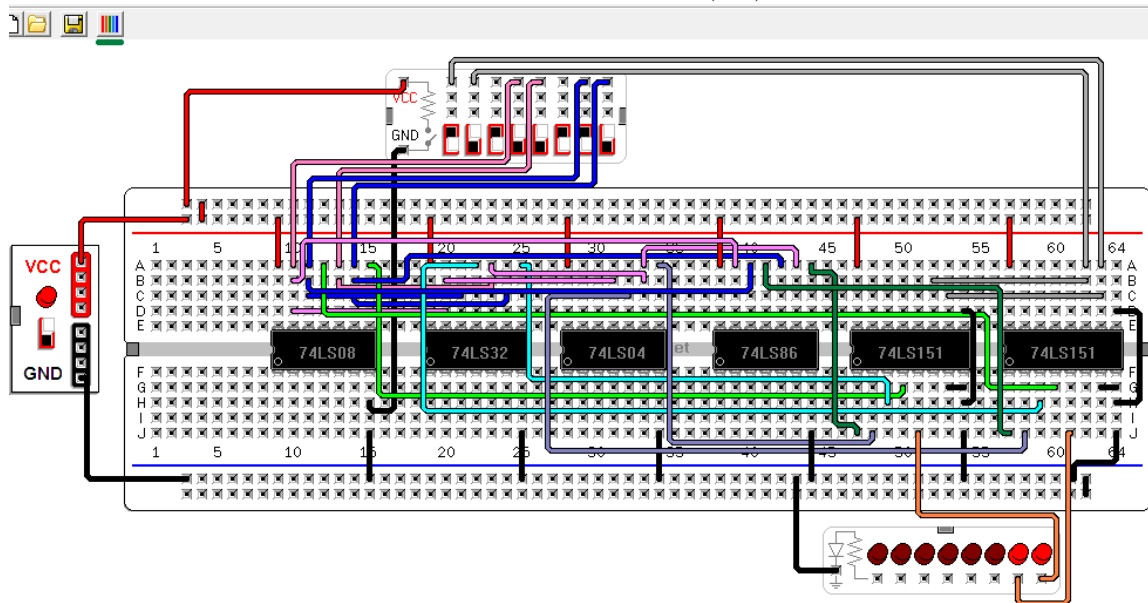


Figura 9: Parte 2 - soma(a,b)

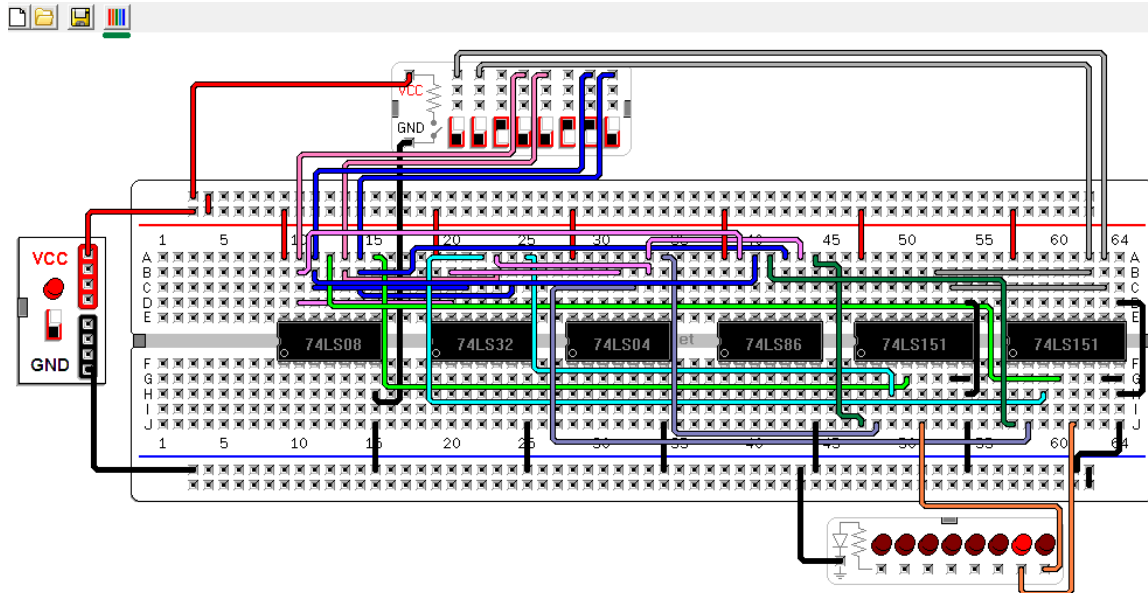


Figura 10: Parte 2 - not(a)

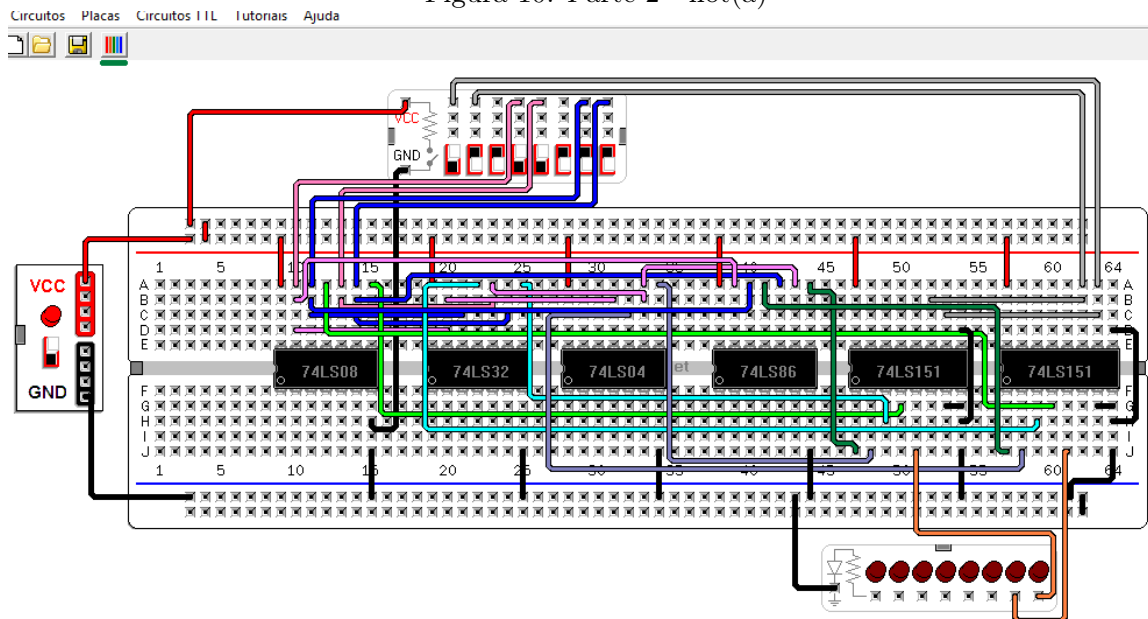


Figura 11: Parte 2 - and(b,a)

