Digital System Design

Mathias Balling & Mads Thede

Last updated: February 27, 2024

Contents

1 VHDL

Very High Speed Integrated Circuit Hardware Description Language. It is a programming language that has been designed and optimized for describing the behavior of digital systems.

1.1 VHDL Syntax

VHDL is not case sensitive, but it is a good practice to use upper case for keywords and lower case for everything else. VHDL describes hardware and so instructions are executed in a concurrent manner, meaning that all instructions are executed at once.

Comments are written with two hyphens (- -).

if, case and loop statements

Every if statement has a corresponding then component and each if statement is terminated with an end if; If an else if statement is needed then it can be written as elsif.

```
if x = '0' and y = '0' or z = '1' then
  blah;
  blah;
end if;
```

Each case statement is terminated with end case; Each loop statement has a corresponding end loop;

```
case (expression) is
  when choices =>
    <sequential statements>
  when choices =>
    <sequential statements>
  when others =>
    <sequential statements>
end case;
```

Signal and variable assignments

Among the most frequently used object types there is the signal object type, the variable object type, and the constant object type. The signal type is the software representation of a wire in the digital system. The variable type is used to store local information. The constant type is used to store constant information.

Signals are declared at the top of the architecture body, just before the keyword begin. Variables must be declared inside the process construct and are local.

Assigning a value to a signal is done using the signal assignment operator <=.

$$C <= not(A);$$

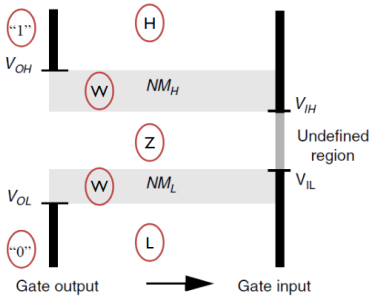
Assigning a value to a variable is done using the variable assignment operator :=.

$$B := A;$$

A variable changes its value soon after the variable assignment is executed. Instead a signal changes its value "some time" after the signal assignment expression is evaluated.

1.2 VHDL Design Units

STD LOGIC



Character	Value
'U'	uninitialized
'X'	strong drive, unknown logic value
'0'	strong drive, logic zero
'1'	strong drive, logic one
'Z'	high impedance
'W'	weak drive, unknown logic value
'L'	weak drive, logic zero
'H'	weak drive, logic one
'-'	don't care

Entity

The entity describes how the unit interfaces with the outside world. The entity lists the various inputs and outputs of the underlying system.

Architecture

Describes what the circuit actually does. It describes the internal implementation of the associated entity. An architecture can be written by means of three modeling techniques plus any combination of these three: dataflow, behavioral, and structura plus any combination of these three.

Karnaugh map (K-map)

A method of circuit optimization. Aims to reduce logic functions more quickly and easily compared to Boolean algebra.

Combinational circuits

It is defined as the time independent circuits which do not depend upon previous inputs to generate any output. e.g. Encoder, Decoder, Multiplexer, Demultiplexer etc.

Sequential circuits

Dependent on clock cycles and depends on present as well as past inputs to generate any output. e.g. Flip-flops, Counters, Registers etc.

Concurrent Statements CHDL has the ability to execute a virtually unlimited number of statements at the same time and in a concurrent manner. The key thing to remember is that we are designing hardware.

Conditional Signal Assignment when

Conditional signal assignment is a concurrent statement that assigns a value to a signal based on the value of a condition. The syntax is:

```
<target> <= <expression> when <condition> else
        <expression> when <condition> else
        <expression>;
```

Selected Signal Assignment with select

Selected signal assignments only have one assignment operator. Selected signal assignment differs from conditional assignment statements in that assignments are based upon the evaluation of one expression. The syntax is:

```
with <choose_expression> select
  <target> <= <expression> when <choices>,
              <expression> when <choices>
              <expression> when others;
```

The general form of the selected signal assignment statement is similar to switch statements as seen in algorithmic programming languages such as C.

Process Statements

The process statement is a stement which contains a certain number of instructions that, when the process statement is executed, are executed sequentially. In other words the process statement is a tool that can be used for executing a certain number of instructions in a sequential manner.

1.3 Standard models in VHDL Architecture

Data-flow style architecture

Circuits are described by showing the input and ouput relationships between the various built-in components of the VHDL language.

Behavioral style architecture

It provides no details as to how the design is implemented in actual hardware. The behavioral style models how the circuit outputs will react to the circuit inputs. Whereas in data-flow modeling you somewhat need to have a feel for the underlying logic in the circuit. In other words, data-flow modeling describes how the circuit should look in terms of logic gates whereas behavioral modeling describes how the circuit should behave.