```
--------------------------------------------------------------------------------
-- ALU.VHD
--------------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use ieee.std_logic_unsigned.all;

library lib_nanoproc;
use lib_nanoproc.nano_pkg.all;

entity ALU is
port (  a,b : in std_logic_vector(len_data_bus-1 downto 0);
    alu_code : in std_logic_vector(1 downto 0);
    r : out std_logic_vector(len_data_bus-1 downto 0));
end ALU;

architecture behavior of ALU is
begin
    process (a,b,alu_code)
    begin
        case alu_code is
        when alu_add => r<=std_logic_vector(unsigned(b) + unsigned(a));
        when alu_sub => r<=std_logic_vector(unsigned(b) - unsigned(a));
        when alu_and => r<=std_logic_vector(unsigned(b) and unsigned(a));
        when others => r<=std_logic_vector(unsigned(b) + unsigned(a));
        end case;
    end process;
end behavior;


--------------------------------------------------------------------------------
-- DEC3TO8.VHD
--------------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity DEC3TO8 is
port (  w   : in std_logic_vector(2 downto 0);
    y   : out std_logic_vector(0 to 7));
end DEC3TO8;

architecture behavior of DEC3TO8 is
begin
    process (w)
    begin
    case w is
        when "000" => y <= "10000000";
        when "001" => y <= "01000000";
        when "010" => y <= "00100000";
        when "011" => y <= "00010000";
        when "100" => y <= "00001000";
        when "101" => y <= "00000100";
        when "110" => y <= "00000010";
        when "111" => y <= "00000001";
        when others =>
    end case;
    end process;
```

```
end behavior;
```