University of Colorado Boulder

Electrical and Computer Engineering

University of Colorado Boulder

ECEN3730 Practical PCB Design Manufacture

LABORATORY REPORT

Lab 9 Report: Cross talk between signal-return loops

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1 Introduction

In this lab, we explored the impact of different interconnect approaches on cross talk between an aggressor and victim signal-return path pair. We specifically focused on measuring switching noise cross talk and how it is affected by the number of I/O pins switching simultaneously, as well as the routing geometry of the interconnects and return paths. We use a special board with different layouts to see the effect of cross talk.

2 Objectives and Learning Outcomes

1. To practice measuring switching noise cross talk by triggering the oscilloscope on the aggressor signal.
2. To examine different wiring options for signal paths and return paths.
3. To distinguish and identify the signal path and the return path of any interconnect.
4. To compare the timing using both the digitalWrite and PORTB commands.
5. To write the microcode for a pulse train for 1 to 6 I/O pins switching simultaneously with different patterns.
6. To measure the victim noise signature.
7. To evaluate how switching noise scales with the number of simultaneous switching signals.
8. To evaluate how cross talk to the victim line varies as the physical wiring of the aggressor and the victim changes.
9. To identify the routing geometry that creates the lowest cross talk.

3 Methodology

3.1 Circuit

- We were given a board with three closed-loop configurations: Common return for the victim line, Separate return for the victim line, and Ground plain return.

3.1.1 Measurements

- The circuit has header pins that are sized up to connect to an Arduino Uno's pins d8-d13. These are the aggressor lines. Using the Arduino, we can toggle each pin and see the effect in the parallel running victim line.
- From previous labs, aswell as the data sheet of the Arduino Uno, we can see the rise time will be around $5us$.
- This is a fast rise time, and will generate a lot of noise in the circuit.

4 Measurements and Outcomes

4.1 Case 1: Ground plane

4.1.1 Initial predictions

- We can assume the case with a ground plane will be the best. This case has the biggest return path for all signals, as well as the continuous plain. This will reduce ground loops and make the noise induced in the victim line much less.

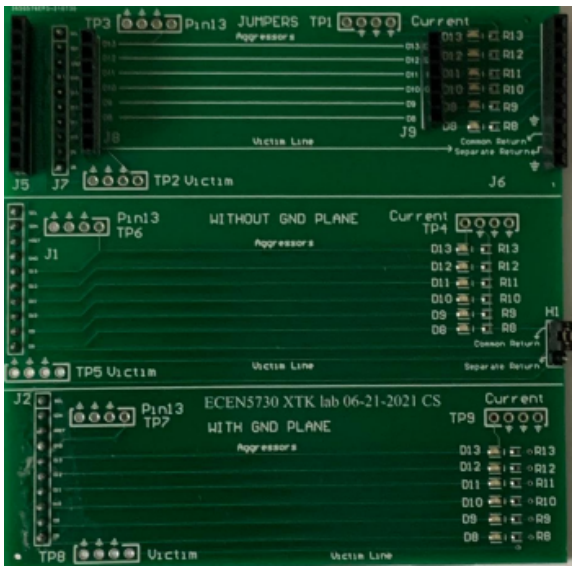

Figure 1: Circuit board used in lab

4.1.2 Measurements

Trigger pin 13 (Yellow)

Victim line (Green)

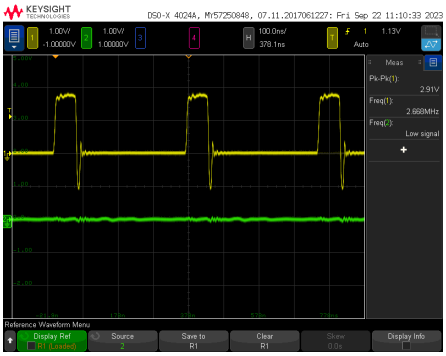

Figure 2: All IO's switching.

Figure 3: IO d8 and d13 switching

- In figure 2, we see the noise introduced is only around $50mV$. In figure 2 we have all the io's(pins d8-d13) turning on and off as fast as possible. We can see this happens at a frequency of around $2.6Mhz$.
- In figure 3, we see the noise is slightly reduced. Only pins d8 and d13 are switching. We do this to see the effect of the closest line to the victim. We see here the speed of switching has not changed, however, the noise is slightly reduced.

4.2 Case 2: No Ground plane, Separate return

4.2.1 Initial predictions

- This case, there is no ground plane, and the victim line will have its own return. Because of the missing ground plane, we can guess the ground loops will be greater, and more noise will be introduced into the circuit.

4.2.2 Measurements

Trigger pin 13 (Yellow)

Victim line (Green)

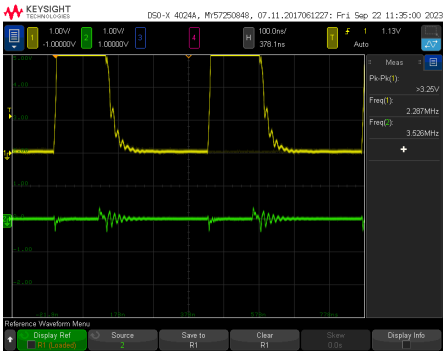

Figure 4: All IO's switching.

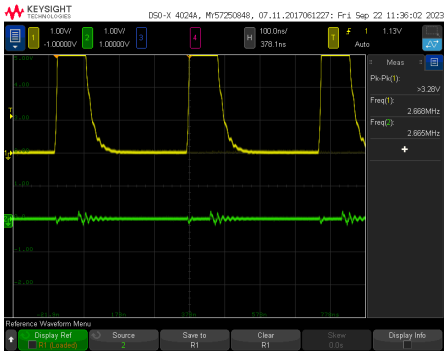

Figure 5: IO d8 and d13 switching

- In figure 4, we see the noise introduced is much more then before. The peak noise is around $450mV$.
- In figure 5, we see the noise is reduced. The peak noise is around $200Mv$. Only pins d8 and d13 are switching. We can see here the proximity of the lines has a big impact.

4.3 Case 3: No Ground plane, Shared return

4.3.1 Initial predictions

- This case, there is no ground plane, and the victim line will share its return with all the aggressor lines. We expect to see the same level of noise due to the missing ground plane, however, more noise on top of that will be introduced due the the shared return. I would guess the nose will be doubled from case 2.

4.3.2 Measurements

Trigger pin 13 (Yellow)

Victim line (Green)

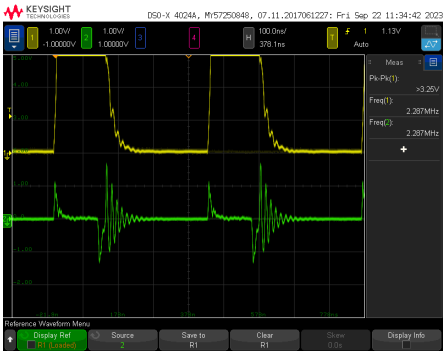

Figure 6: All IO's switching.

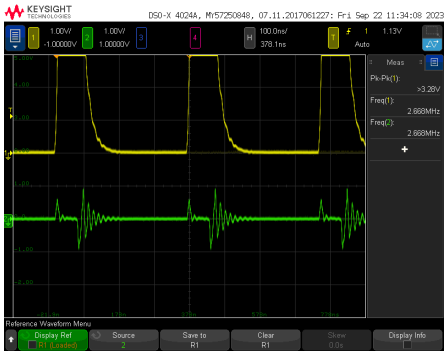

Figure 7: IO d8 and d13 switching

4.4 Experiment

- To see the sources of noise better, I decided to conduct an experiment. I want to trigger each pin separately and view the effect it has on the victim line. I wrote some Arduino code to toggle each pin one by one starting on pin d13, and going down to pin d8. This will toggle each pin high and low separately, so we can see their unique noise signature.

4.4.1 Initial predictions

- I expect to see the same variations in peak noise due to the layout as we saw above. However, in this case, I expect to the noise "ramp up" as pins are toggled closer to the victim line.

4.4.2 Measurements

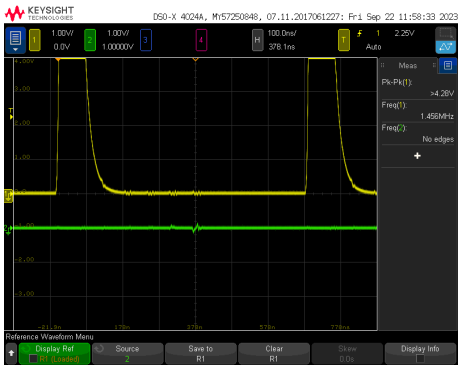

Figure 8: Experiment with Case 1

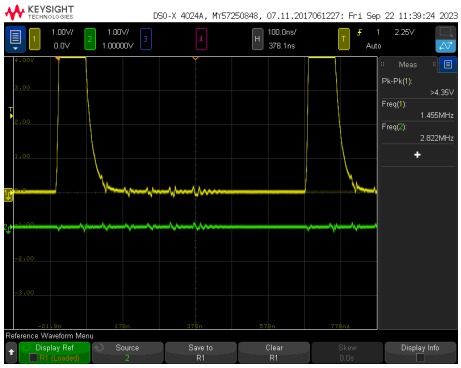

Figure 9: Experiment with Case 2

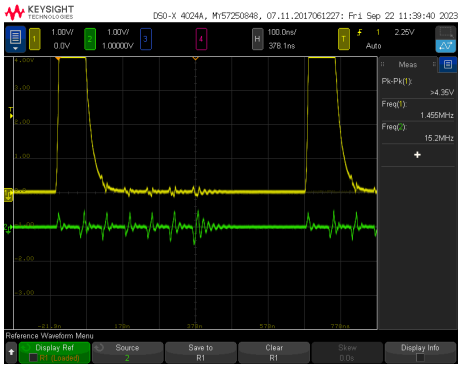

Figure 10: Experiment with Case 3

- This shows an interesting trend. We see the last noise spike corresponding with pin d8 has the most impact, however, the noise doesn't ramp down linearly. This implies pure proximity is not the greatest factor for noise. The whole circuit and how all the signal paths and returns are laid out all contribute the the noise.

5 Results

5.1 Experimental observations

- To better understand the circuits we can find the mutual inductance for each case and see how the PCB layout alters it.
  - $VitctimVoltage = 6 * L * \frac{AgressorVoltage}{AgressorResistance}/RiseTime.$
  - Slowest-Case Rise Time: $30ns$
  - Case 1:
    - Max noise measured: 0.4V
    - Resistor Voltage: 1.5V
  - Case 2:
    - Max noise measured: 2V
    - Resistor Voltage: 1.5V
  - Case 3:
    - Max noise measured: 3.6V
    - Resistor Voltage: 1.5V

Case	Measured Mutual Inductance
1	$62nH$
2	$331nH$
3	$564nH$

- We see the less optimal the layout, the more mutual inductance. By using best practices we can reduce this and keep noise to a minimum.

5.2 Takeaways

In summary, this lab highlights the importance of careful interconnect design to minimize switching noise cross talk, especially when dealing with fast-switching signals. The results demonstrate that separate return paths and appropriate routing geometry are essential for achieving low cross talk in electronic circuits.

- The rise time of the aggressor signal significantly affects switching noise, with shorter rise times leading to greater noise.
- For signals with rise times shorter than about 100 nsec, switching noise becomes a concern.
- Best practices for reducing cross talk involve using short signal-return path leads and keeping signal and return path conductors close together.
- The choice of return path for aggressor and victim signals plays a crucial role in minimizing cross talk.
- Separating return paths, such as using a plane, reduces switching noise cross talk effectively.
- Cross talk is influenced not only by the proximity of signal traces but also by the configuration of the entire interconnect.