University of Colorado Boulder

Electrical and Computer Engineering

University of Colorado Boulder

ECEN3730 Practical PCB Design Manufacture

LABORATORY REPORT

Board 2 Report

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Submission Date : 10/29/2023

1 Introduction

Board two is used as a demonstration of how layout affects noise on a PCB. In this board, we use a 555 timer to generate a PWM signal and feed it into two hex inverters. One hex inverter has a bad layout, and the other has a good layout using best practices. Each hex inverter will have the same layout. We will explore the differences in noise on both parts of the circuit.

2 Objectives

This section delves deeper into the specific outcomes of Board 2. The focus is on:

1. Demonstrating the influence of layout decisions on switching noise: The main objective is to show that good design practices lead to lower noise levels compared to poor design practices.
2. Implementing best design practices on one circuit and bad practices on another: Board 2 creates two identical circuits, but the layout varies significantly. This enables the illustration of noise reduction through proper design.

3 Plan of Record

Board 2's design process. The design plan involves several key steps:

1. Creating a schematic and defining parts
    - 1206 size SMD parts
    - Timer circuitry designed for about 500 Hz and 50% duty cycle.
2. Determining power requirements
    - 5 V AC to DC converter to power board.
3. Selecting components such as the hex inverters, 555 timer, LEDs, and resistors
    - Use red LEDs and 50 ohm resistors as the load to three of the switching outputs of the hex inverters
4. Planning signal routing and the layout
    - Copper poured return plane and single return path.
5. Designing an isolation switch for the circuit
    - Switches at each of the key signal nodes. 5v, 555.
6. Incorporating test points for measurements
    - Test points for each of the inverters to measure noise. 5v, 3.3v, 555.
7. Implementing quiet high and low signals
    - Each of the inverters will have one input tied to ground and one tied to Vcc.
8. Engineering the layout with two sides: one adhering to best practices, the other illustrating poor layout decisions.
    - Bad layout will have a far decoupling cap, one return path, and long traces.

4 What it means to work

- Power Rail Stability: The board must deliver a stable power rail voltage of approximately 3.3 V, and the 5 V rail (when applicable) should be close to 5 V.
- 555 Timer Functionality: The 555 timer should generate a clock signal with a frequency of around 500 Hz and a duty cycle close to 50%. The signal's rise time should be within the expected range.
- Hex Inverter Performance: The hex inverter circuits should operate correctly, producing an inverted output signal when triggered.
- Low Switching Noise: The switching noise should be lower in the "good layout" circuit compared to the "bad layout" circuit. Proper layout design should visibly minimize the switching noise.
- Measurement Accuracy: All measurements taken during the experiment should align with expectations based on design specifications.

5 Board Design, Assembly, Bring-Up Testing

5.1 Initial Block Diagram:

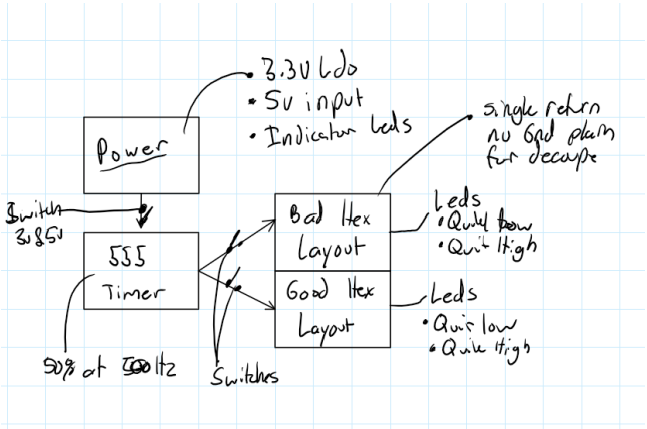

Figure 1: Block Diagram for Board 2

5.2 Schematic of board

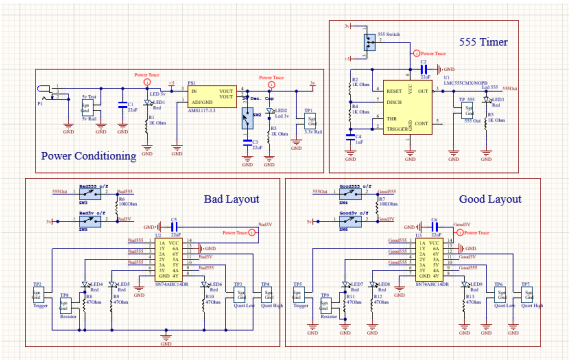

Figure 2: Schematic for Board 2

5.3 Altium designer board layout

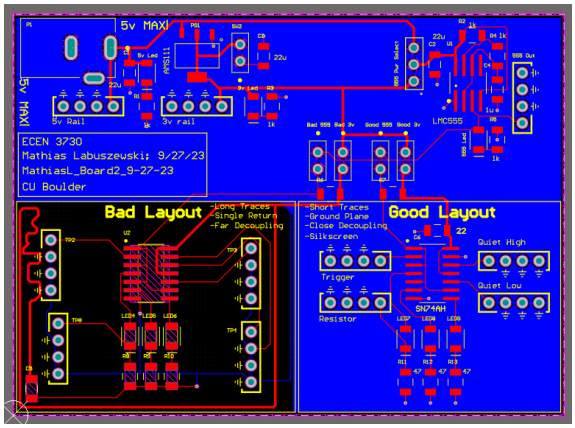

Figure 3: Board layout

5.4 Altium designer 3d view

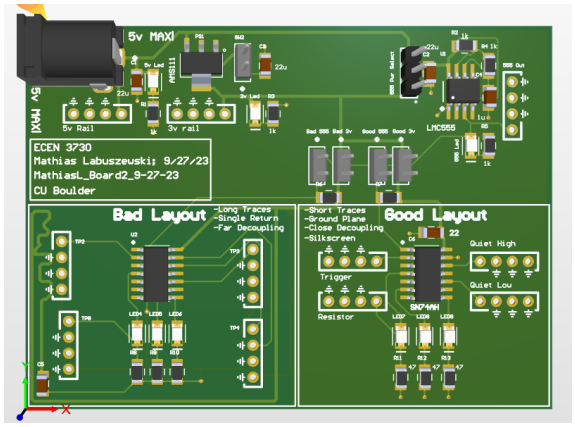

Figure 4: 3d Board layout

5.5 Manufactured board

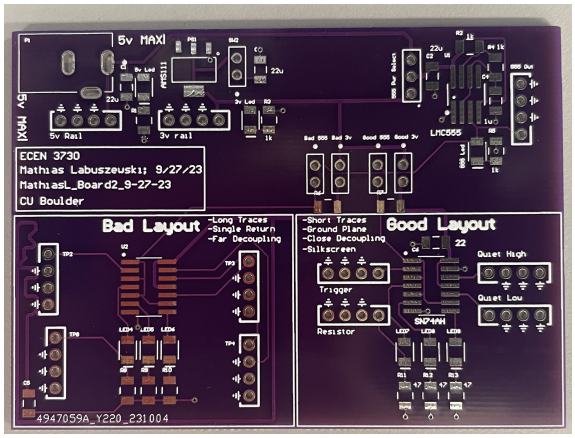

Figure 5: Physical Board 2

5.6 Assembled board

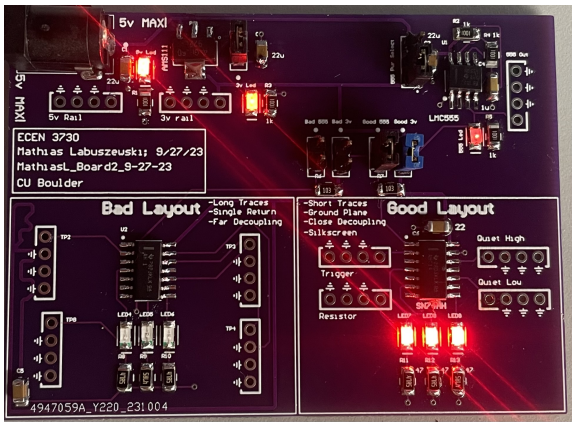

Figure 6: Assembled and working board 2

5.7 Board being tested

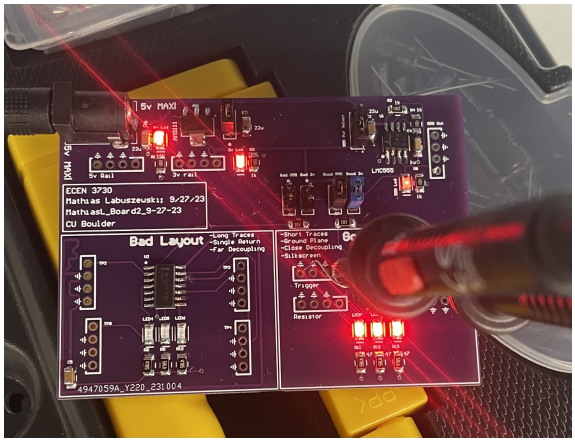

Figure 7: Testing Board 2

6 Measurements

6.1 Estimating Noise

- Before we take measurements, we should anticipate what we expect to see.
- What we expect to see is a general increase in noise from the good to the bad layout. We expect the good layout to have the least amount of switching noise and the fastest rise times. As for the bad layout, we expect to much more switching noise. With only a single return we expect to see noise on the low and high sides of the hex inverter. The far decoupling capacitor will also allow for massive power collapse and thus slower rise times.

6.2 Measuring Quiet High and Quiet Low

The quiet high line's input is connected to the ground and the quiet low is connected to Vcc. We expect to see more noise on the quiet high.

6.2.1 Good Layout

Yellow - Scope Trigger point Green - Quiet low and Quiet hi.

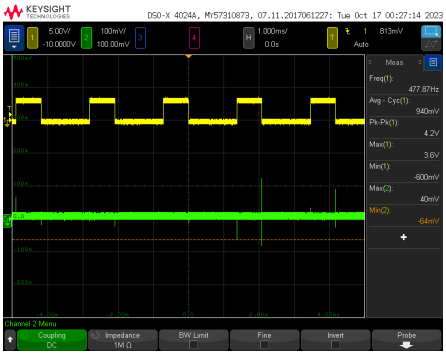

Figure 8: Quiet Low

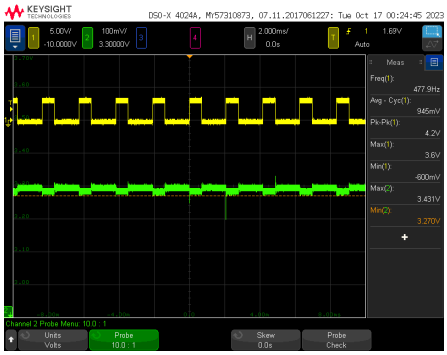

Figure 9: Quiet High

As we predicted, the quiet low will have less noise. The quiet high will have more noise, as the leds are loading the hex inverter. We can see very slight transients in the low and high, however. Lowering the time scale we can see the rise time of the good board.

Figure 10: Quiet Low Rise time - 2ns

Figure 11: Quiet High Rise time - 2ns

The low line has much less of a voltage spike when compared to the high line. The high line will have a power rail collapse due to the switching elements inside the hex inverter. Not only does it draw a constant load on the 3.3v rail as we saw before, but it also creates a very fast transient. The rise times of the good layout are around 2ns. When we measure the bad layout, we expect to see this increase. The noise on the quiet high is around 120mV and 90mv on the low.

6.2.2 Bad Layout

Yellow - Scope Trigger point Green - Quiet low and Quiet hi.

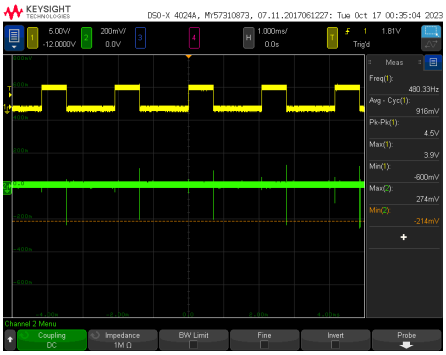

Figure 12: Quiet Low

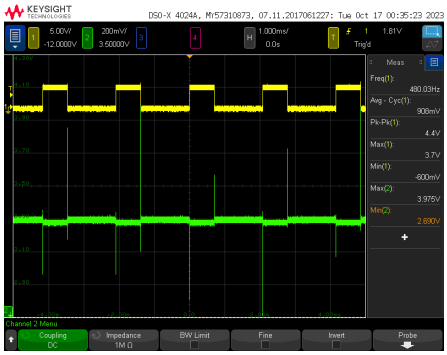

Figure 13: Quiet High

As we predicted, the quiet low will have less noise. The quiet high will have more noise, as the leds are loading the hex inverter. When compared to the good layout, we see much bigger spikes in the quiet low and quiet high. These are due to the far decoupling capacitor and single return line.

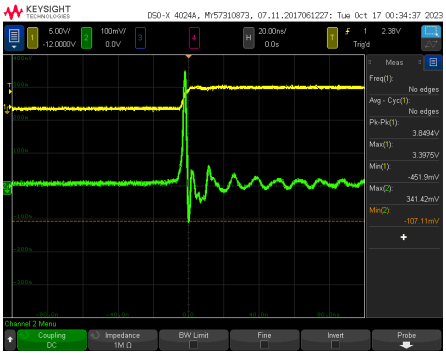

Figure 14: Quiet Low Rise time - 5ns

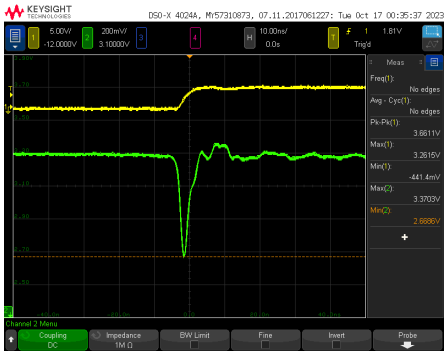

Figure 15: Quiet High Rise time - 5ns

The low line has a much greater voltage spike and longer rise time. The voltage spike is around 0.4v. The rise time is around 5ns. The quiet high has around 0.7v of noise and a rise time of 5ns. The noise on the quiet high is only power rail collapse, due to the far decoupling capacitor. The quiet low line's noise is mostly in the positive region, due to the single return line and current transient on that line.

6.3 Measuring Power rail noise

We want to investigate the power rail noise. We expect to see noise in the power rails when the current is switched. This will happen synchronously to the 555 timer output. I would expect to see less noise on the 3v rail compared to the 5v rail. This is due to the more local voltage regulation, as well as the LDO using a feedback loop to keep the voltage stable. The bad layout should have a much greater noise signature in general.

6.3.1 Good Layout

Yellow - Scope Trigger point Green - 3v and 5v.

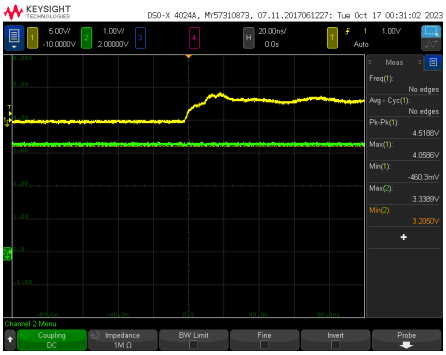

Figure 16: 3v power rail using good layout

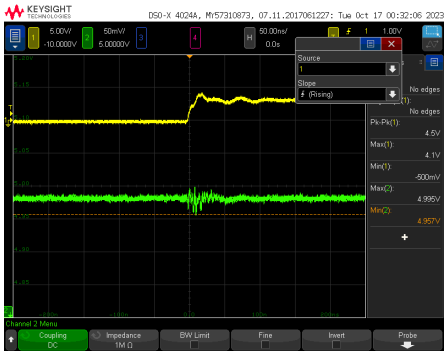

Figure 17: 5v power rail using good layout

As we predicted, the 5v power rail has more noise than the 3v. The 3v power rail looks very clean and shows little noise. The close decoupling capacitor really helps keep the noise out of the power rail.

6.3.2 Bad Layout

Yellow - Scope Trigger point Green - 3v and 5v.

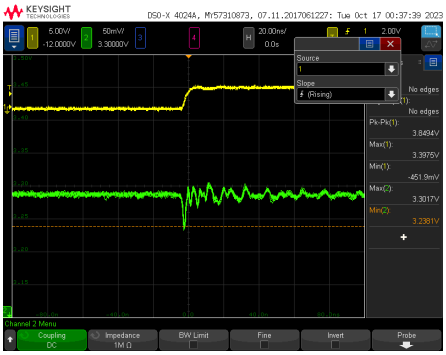

Figure 18: 3v power rail using Bad Layout

Figure 19: 5v power rail using Bad Layout

In the bad layout, we see more noise on the rails. We still see a similar amount of noise on the 5v rail, however, the 3v rail has much more noise and ringing. This is due to the far decoupling capacitor not providing local energy storage, and the single return line creating large current transients back to the 3.3v LDO.

7 Analysis

With the above results, I can conclude my board did work and function correctly as outlined in the POR. The only thing that did not work well was the assembly of the board. I had soldered on every component and tried to test the board. The leads were blinking and did not function correctly, and the measurements would come and go. After inspecting the board, I found my 555 timer's timing resistors were not soldered down. I had only attached one leg of the resistor. After soldering down the other leg, it worked correctly.

No hard errors were made. The only soft error was forgetting to add silk screen labels to some of the components. This was not an issue as the component annotation was there and I could cross-reference with Altium.

I was glad I added lots of test points and isolation switched. I added extra switches to measure the LDO with and without the capacitor, however, I did not get around to measuring it.

8 Summary of Findings

- Power Rail Stability: The board successfully delivered a stable power rail voltage of approximately 3.3 V, and 5v.
- 555 Timer Functionality: The 555 timer generated a clock signal with a frequency close to 500 Hz and exhibited a duty cycle of approximately 50%. The rise time of the signal was within the expected range.
- Hex Inverter Performance: Both hex inverter circuits operated as expected, producing an inverted output signal when triggered and switching accurately.
- Switching Noise Analysis: We observed noticeable differences in switching noise between the good layout and bad layout circuits. The good layout circuit consistently exhibited lower switching noise.
- Measurement Accuracy: All measurements aligned closely with the initial design. All signals were measured using a 10x probe with spring tip.

9 Impact of Layout

The experiment clearly demonstrated the critical importance of layout decisions in minimizing switching noise. The good layout circuit, designed with a continuous return plane and decoupling capacitors located close to IC power pins, showed significantly lower switching noise compared to the bad layout circuit with no ground plane and distant decoupling capacitors.

Layout plays a crucial role in controlling emi, ground bounce, and power rail noise, and ensuring the proper operation of electronic circuits. The results highlight the significance of adhering to best design practices, such as proper component placement and decoupling capacitor positioning to mitigate switching noise and maintain signal integrity.

10 Conclusion

In this lab experiment, we set out to explore the influence of layout decisions on switching noise in a PCB. We designed a board Board 2 with two identical circuits but different layouts: one adhering to best design practices, and the other demonstrating bad features of a bad layout. The experiment aimed to assess the impact of these layouts on switching noise and measure various parameters to see the board's performance.