# University of Colorado Boulder

**Electrical and Computer Engineering**


University of Colorado Boulder

**ECEN3730 Practical PCB Design Manufacture**

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# LABORATORY REPORT

**Lab 15: Bogatin's good-bad switching noise board**

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# 1 Introduction

Lab 15 provides an opportunity to explore switching noise expectations and principles for board design, emphasizing critical design aspects: maintaining a continuous return path under signal traces and using low-inductance decoupling capacitors near IC power pins. The lab aims to demonstrate important problems related to switching noise on a board with varying design qualities. This board features a 555 timer as a clock and three hex inverter circuits, two designed with a continuous return plane and another intentionally designed poorly to create switching noise. The lab focuses on measuring switching noise on quiet HIGH and quiet LOW inverter pins, as well as the power rails.

# 2 Objectives

1. Explore and understand the impact of design practices on switching noise.
2. Measure the switching properties of the board.
3. Compare and contrast switching noise in the "good" and "bad" design regions.
4. Identify important design features for noise reduction.

# 3 Test Board

The board used for this lab is a variation of board 2. The board operates with a 5 V power source, utilizing a 555 timer, 3v LDR, and hex inverters. Three regions on the board showcase different design scenarios: a bad design, a design with no return plane and a distant decoupling capacitor; a bad design with a ground plane but distant decoupling capacitor; and a good design with a ground plane and a close decoupling capacitor.

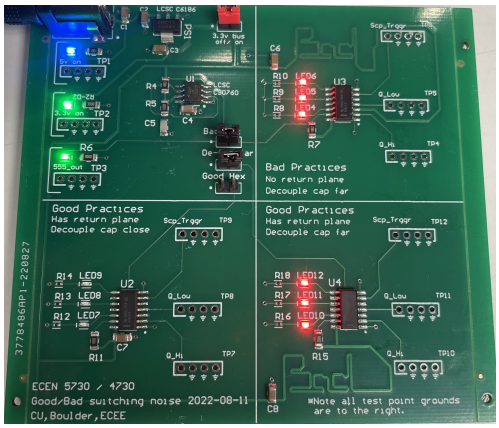


**Figure 1:** Picture of Board 1

The board is built in 3 main sections. There is the power conditioning, 555 timer, and the hex inverter. The hex inverter features 6 inputs and 6 outputs. Two of the inputs are tied to ground and Vcc respectively. The other 3 are connected to the 555 timer output, and drive led's. The last input is also connected to the 555 timer and is used as a trigger for the oscilloscope. There are 3 different layouts of the hex inverter, all with identical schematics. The only difference is how the PCB and components are laid out.

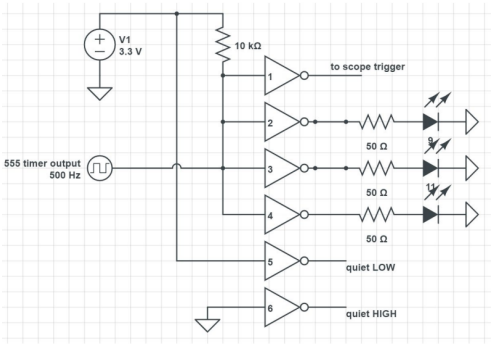


**Figure 2:** Hex inverter schematic

There are test points on the quiet hi and quiet low, aswell as the trigger. The 5v and 3v power rails also have a test point we will measure.

# 4 Methodology

## 4.1 Estimating Noise

- Before we take measurements, we should anticipate what we expect to see.
- What we expect to see is a general increase in noise from the good to bad layout. We expect the good layout to have the least amount of switching noise, and fastest rise times. The good layout with the further capacitor will have not much noise, but the rise times should increase compared to the close capacitor. The switching noise will also be slightly higher, but much less than the bad layout. As for the bad layout, we expect to much more switching noise. With only a single return we expect to see noise on the low and high sides of the hex.

## 4.2 Measuring Quiet High and Quiet Low

The quiet high line's input is connected to the ground and the quiet low is connected to Vcc. We expect to see more noise on the quiet high.

### 4.2.1 Good Layout

Yellow - Scope Trigger point Green - Quiet low and Quiet hi.

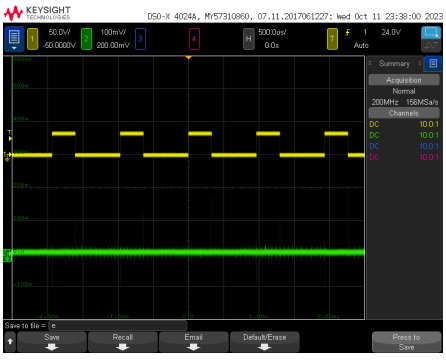

**Figure 3:** Quiet Low

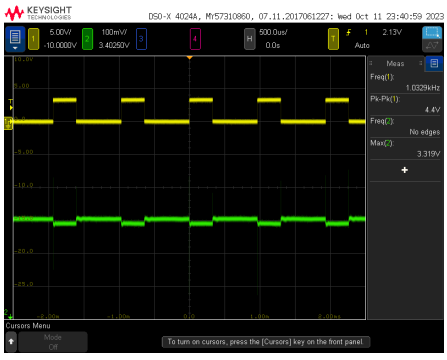

**Figure 4:** Quiet High

Quiet low and Quiet high. We see the low line has very minimal noise, which is caused by the continuous ground plane. The quiet high has much more switching noise. He can see the output stays at a constant level when it changes. This is likely due to the current being used to drive the led's.

### 4.2.2 Good Layout with far capacitor

Yellow - Scope Trigger point Green - Quiet low and Quiet hi.

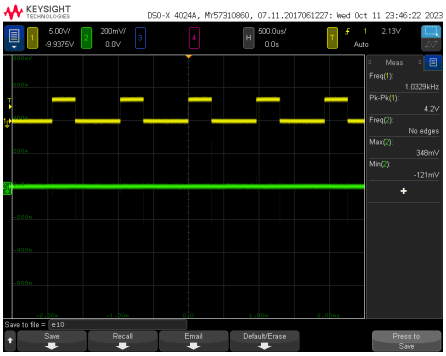

**Figure 5:** Quiet Low

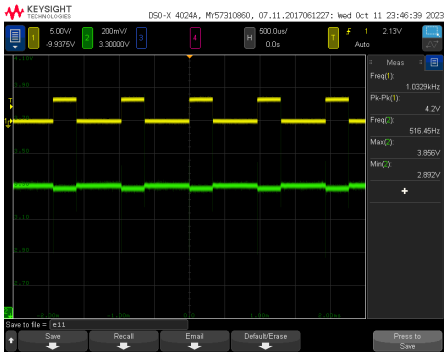

**Figure 6:** Quiet High

Quiet low and Quiet high. We see the low line has very minimal noise, which is caused by the continuous ground plane, the same as what we saw before. The quiet high has a very similar shape as the good case, but the rise time and noise transient have grown due to the decoupling capacitor being placed further away. We will investigate this more later.

### 4.2.3 Bad Layout

Yellow - Scope Trigger point Green - Quiet low and Quiet hi.

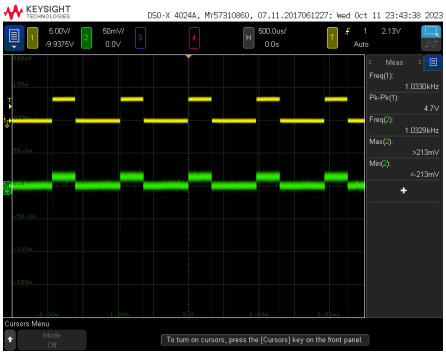

**Figure 7:** Quiet Low

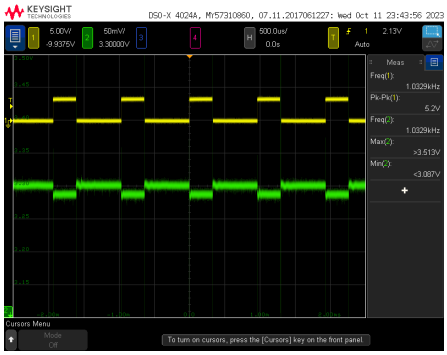

**Figure 8:** Quiet High

Quiet low and Quiet high. We see the low line now has lots and lots of noise. There is only a single return line, so all the noise is now feeding back. The line is not very stable. The Quiet High also has lots of noise. We can see there is some ripple in the waveform on the falling and rising edge. There are very large transients during the switching as well. We can see lines that extend below the range of the scope. We will look at this later.

## 4.3 Measuring Power rail noise

We want to investigate the power rail noise. We expect to see noise in the power rails when the current is switched. This will happen synchronously to the 555 timer output. I would expect to see less noise on the 3v rail compared to the 5v rail. This is due to the more local voltage regulation, as well as the LDO using a feedback loop to keep the voltage stable.

### 4.3.1 Good Layout

Yellow - Scope Trigger point Green - 3v and 5v.

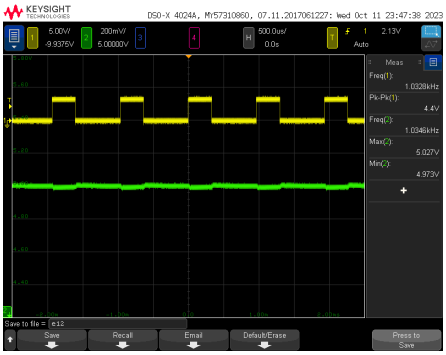

**Figure 9:** 5v power rail using good layout

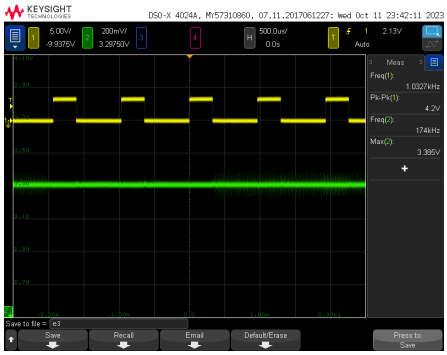

**Figure 10:** 3v power rail using good layout

As we predicted, the 5v power rail has more noise than the 3v. The 3v power rail looks very clean and shows little noise. The close decoupling capacitor really helps keep the noise out of the power rail.

### 4.3.2 Good Layout with far capacitor

Yellow - Scope Trigger point Green - 3v and 5v.

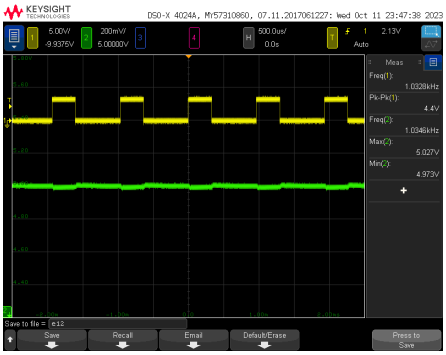

**Figure 11:** 5v power rail using good layout with far capacitor

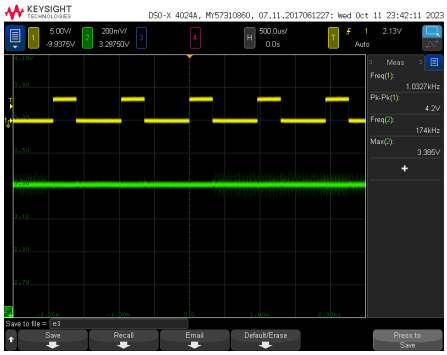

**Figure 12:** 3v power rail using good layout with far capacitor

Again the 3v power rail has less noise than the 5v rail. However, now we see the 3v rail is not as clean of a signal as it was before. Some noise has been introduced. This is because of the decoupling capacitor does not provide the proper local energy storage the hex inverter needs when switching. In turn, it creates noise in the 3v rail, which also backtracks to the 5v rail.

### 4.3.3 Bad Layout

Yellow - Scope Trigger point Green - 3v and 5v.

**Figure 13:** 5v power rail using Bad Layout

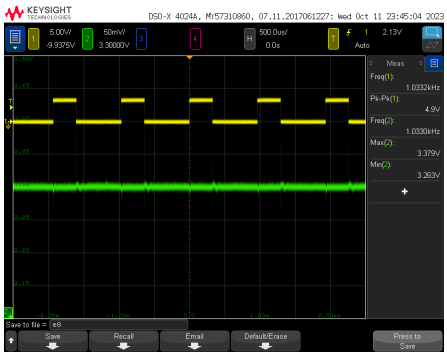

**Figure 14:** 3v power rail using Bad Layout

In the bad layout, the noise is amplified even more. The 3v rail has lots of switching noise on the rise and fall of the 555 timer and has large transient spikes. We see the effect of this in the 5v power rail. The LDO has to compensate and in turn, feeds noise into the 5v power rail. A larger capacitor on the 5v power rail would help reduce a lot of the switching noise.

## 4.4 Measuring Rise and Fall times

We want to investigate the rise and fall time closer. We will take a look at the quiet high line on all 3 variations of the hex layout. With the info we saw above, we expect to see larger noise transients on the bad layout and good far decoupling capacitor layout.

### 4.4.1 Good Layout

Yellow - Scope Trigger point Green - Quiet High

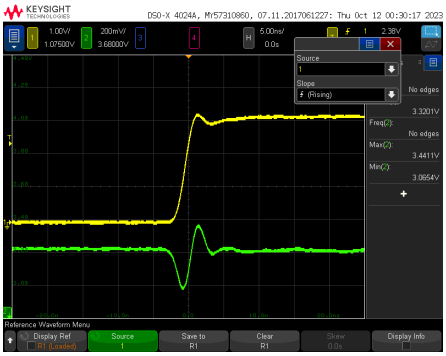

**Figure 15:** Quiet high rise time - 2.5ns

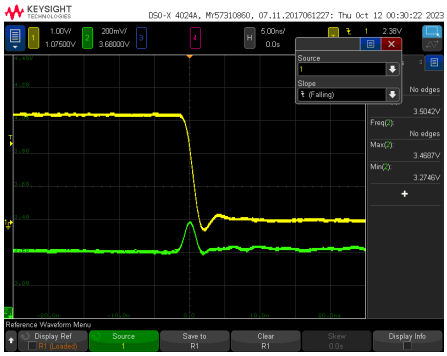

**Figure 16:** Quiet high fall time - 2ns

We can see during the rise we get a noise of 0.4Vpp and during the fall we get a noise of 0.2Vpp. The rise and fall times are very fast, so we expect to see some noise.

### 4.4.2 Good Layout with far capacitor

Yellow - Scope Trigger point Green - 3v and 5v.

**Figure 17:** Quiet high rise time - 4.5ns

**Figure 18:** Quiet high fall time - 2ns

Interestingly, we see the rise time has nearly doubled compared to the good layout. Without the local energy storage very close, there is lots of loop inductance and the IC does not have as much instantaneous current. We see this in the noise on the rise. The voltage dips down all the way to 2.5v! There is around 0.8 Vpp of noise on the rising edge. During the falling edge, we see another massive spike upwards of 4.2v. This again is caused by the far decoupling capacitor and higher loop inductance. the noise is around 1.2Vpp.

### 4.4.3 Bad Layout

Yellow - Scope Trigger point Green - 3v and 5v.

**Figure 19:** Quiet high rise time - 8ns

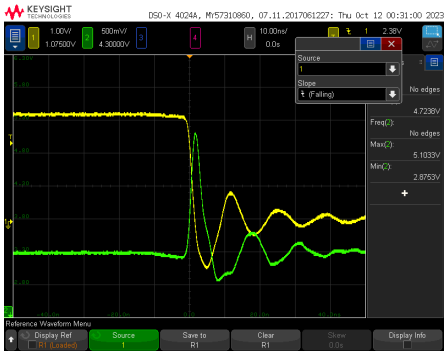

**Figure 20:** Quiet high fall time - 2ns

The rise time has doubled once again. This is due to the increased loop inductance. Not only is there now a long path from the capacitor to the IC, there is also a long return path. There is a massive power collapse, and on the quiet high line, we see the voltage dips down to around 2.4v. The noise is around 1.1Vpp. This is greater than both other cases. As we saw before with the far capacitor, we expect to see a large transient during the falling edge. There is around 2.3Vpp of noise on the quiet high. The voltage peaks up to 5.1v!

Interestingly we see the fall times on all three layouts stay relatively the same. We expect to see the rise times increase as there is increasing less local energy storage and greater loop inductance with the three cases. Interestingly, the good layout still has lots of noise, but also a very fast rise time. With a rise time of the bad layout, we would expect to see very little noise. Trace length and return paths have a very big effect on the performance of the circuit.

## 4.5 Outcomes and Best Design Practices

- Ground Plane: Create a solid ground plane to provide a low-impedance return path for high-speed signals and reduce ground bounce.
- Signal Return Paths: Ensure that signal return paths are as short and direct as possible to minimize loop areas and reduce inductance.
- Use Decoupling Capacitors: Place decoupling capacitors close to the power pins of integrated circuits to absorb high-frequency noise and provide local energy storage.
- Proper Termination: Terminate traces correctly to minimize signal reflections and ringing.
- Short Paths: Use short traces to reduce loop inductance and signal travel time.

## 4.6 Conclusion

In conclusion, Lab 15 highlights the importance of board design in minimizing switching noise. By examining a board with good and bad design regions, this lab offers valuable insights into the effects of design choices on noise levels. It underscores the significance of adhering to good design practices, particularly in scenarios where noise reduction is crucial. The ability to measure and analyze switching noise is a valuable skill for any electronics engineer.