PSoC® Creator™
Project Datasheet for Laboratoire3

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Table of Contents

1 Overview

The Cypress PSoC 6 is a family of 32-bit devices with the following characteristics:

- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals such as PWM, UART, SPI and I2C
- Analog subsystem that includes 12-bit SAR ADC, comparators, op amps, CapSense, LCD drive and more
- Several types of memory elements, including SRAM and flash
- Programming and debug system through Serial Wire Debug (SWD)
- High-performance 32-bit ARM Cortex-M4 core with a nested vectored interrupt controller (NVIC)
- Flexible routing to all pins

Figure 1 shows the major components of a typical PSoC 63 series member PSoC 6 device. For details on all the systems listed above, please refer to the PSoC 6 Technical Reference Manual .

Figure 1. PSoC 63 Device Series Block Diagram

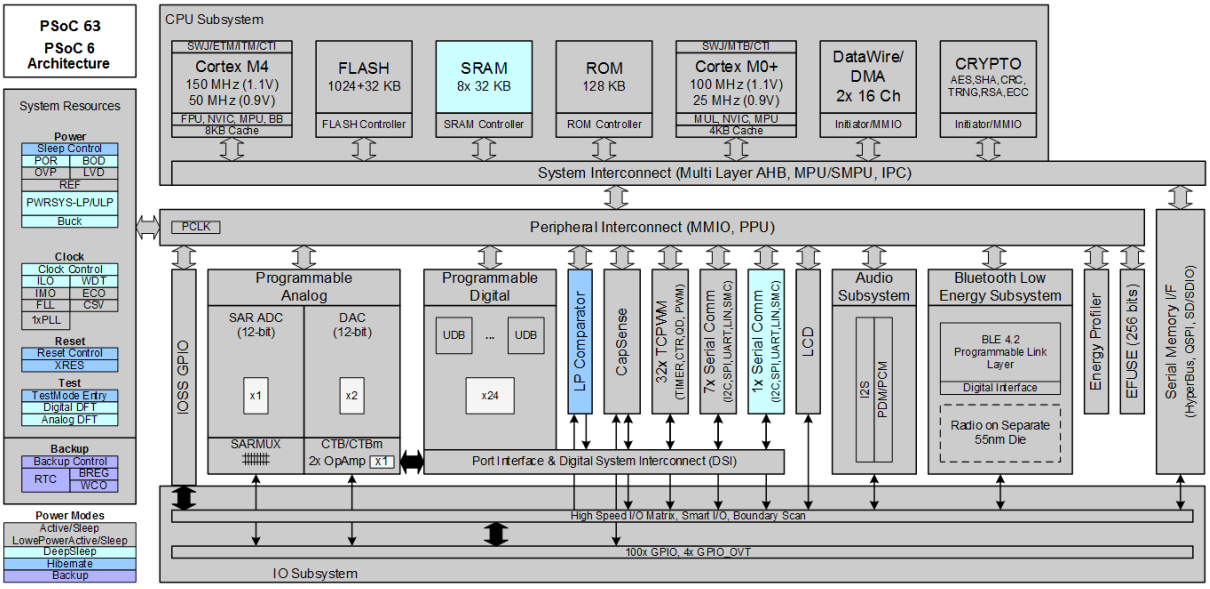


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C6347BZI-BLD53
Package Name	116-BGA-BLE
Family	PSoC 6
Series	PSoC 63
Max CPU speed (MHz)	150
Flash size (kB)	1024
SRAM size (kB)	288
Vdd range (V)	1.7 to 3.6
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

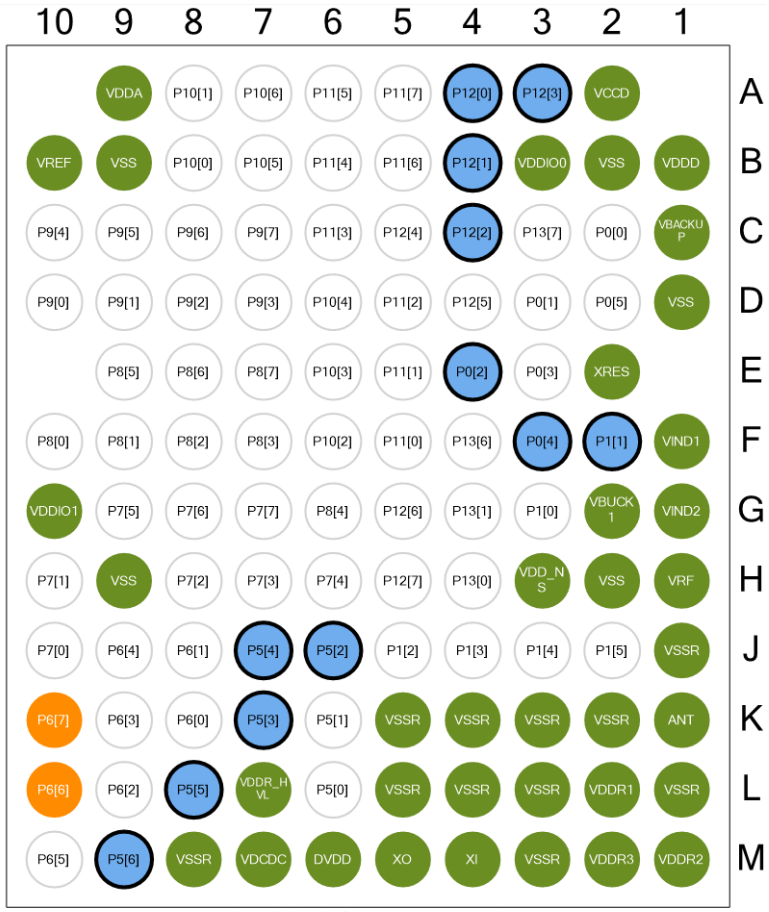
Resource Type	Used	Free	Max	% Used
Digital Clocks	0	8	8	0.00 %
Crypto Accelerator	0	1	1	0.00 %
Interrupts [CM0+]	5	27	32	15.63 %
Interrupts [CM4]	1	146	147	0.68 %
IO	14	64	78	17.95 %
Interprocessor Communication	0	16	16	0.00 %
MCWDT	0	2	2	0.00 %
CapSense	0	1	1	0.00 %
Energy Profiler	0	1	1	0.00 %
Real Time Clock	0	1	1	0.00 %
Bluetooth Low Energy	0	1	1	0.00 %
I2S	0	1	1	0.00 %
PDM/PCM	0	1	1	0.00 %
SCB	1	8	9	11.11 %
Serial Memory Interface	0	1	1	0.00 %
DMA Channels	0	32	32	0.00 %
LCD	0	1	1	0.00 %
SmartIO	0	2	2	0.00 %
TCPWM	2	30	32	6.25 %
UDB				
Macrocells	0	96	96	0.00 %
Unique P-terms	0	192	192	0.00 %
Total P-terms	0			
Datapath Cells	0	12	12	0.00 %
Status Cells	1	11	12	8.33 %
Status Registers	1			
Control Cells	0	12	12	0.00 %
7-Bit IDAC	0	2	2	0.00 %
Continuous Time DAC	0	1	1	0.00 %
LP Comparator	0	2	2	0.00 %
Opamp	0	2	2	0.00 %
Sample and Hold	0	1	1	0.00 %

Resource Type	Used	Free	Max	% Used
SAR ADC	0	1	1	0.00 %
DieTemp Sensor	0	1	1	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



CY8C6347BZI-BLD53
116-BGA-BLE
(bottom view)

2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode
2	VCCD	VCCD	Power	
3	P12[3]	CY_EINK_Ssel	Software In/Out	Strong drive
4	P12[0]	\CY_EINK_SPIM:mosi_m\	Dgtl Out	Strong drive
5	P11[7]	GPIO [unused]		
6	P11[5]	GPIO [unused]		
7	P10[6]	GPIO [unused]		
8	P10[1]	GPIO [unused]		
9	VDDA	VDDA	Power	
11	VDDD	VDDD	Power	
12	VSS	VSS	Power, Dedicated	
13	VDDIO0	VDDIO0	Power	
14	P12[1]	\CY_EINK_SPIM:miso_m\	Dgtl Out	HiZ analog
15	P11[6]	GPIO [unused]		
16	P11[4]	GPIO [unused]		
17	P10[5]	GPIO [unused]		
18	P10[0]	GPIO [unused]		
19	VSS	VSS	Power, Dedicated	
20	VREF	VREF	Dedicated	
21	VBACKUP	VBACKUP	Power	
22	P0[0]	GPIO [unused]		
23	P13[7]	GPIO [unused]		
24	P12[2]	\CY_EINK_SPIM:sclk_m\	Dgtl Out	Strong drive
25	P12[4]	GPIO [unused]		
26	P11[3]	GPIO [unused]		
27	P9[7]	GPIO [unused]		
28	P9[6]	GPIO [unused]		
29	P9[5]	GPIO [unused]		
30	P9[4]	GPIO [unused]		
31	VSS	VSS	Power, Dedicated	
32	P0[5]	GPIO [unused]		
33	P0[1]	GPIO [unused]		
34	P12[5]	GPIO [unused]		
35	P11[2]	GPIO [unused]		
36	P10[4]	GPIO [unused]		
37	P9[3]	GPIO [unused]		
38	P9[2]	GPIO [unused]		
39	P9[1]	GPIO [unused]		
40	P9[0]	GPIO [unused]		
42	XRES	XRES	Dedicated	
43	P0[3]	GPIO [unused]		
44	P0[2]	CY_EINK_DisploEn	Software In/Out	Strong drive

Pin	Port	Name	Type	Drive Mode
45	P11[1]	GPIO [unused]		
46	P10[3]	GPIO [unused]		
47	P8[7]	GPIO [unused]		
48	P8[6]	GPIO [unused]		
49	P8[5]	GPIO [unused]		
51	VIND1	VIND1	Dedicated	
52	P1[1]	GreenLED	Dgtl Out	Res pull up
53	P0[4]	SW2	Dgtl In	Res pull up
54	P13[6]	GPIO [unused]		
55	P11[0]	GPIO [unused]		
56	P10[2]	GPIO [unused]		
57	P8[3]	GPIO [unused]		
58	P8[2]	GPIO [unused]		
59	P8[1]	GPIO [unused]		
60	P8[0]	GPIO [unused]		
61	VIND2	VIND2	Dedicated	
62	VBUCK1	VBUCK1	Power	
63	P1[0]	OVT IO [unused]		
64	P13[1]	GPIO [unused]		
65	P12[6]	GPIO [unused]		
66	P8[4]	GPIO [unused]		
67	P7[7]	GPIO [unused]		
68	P7[6]	GPIO [unused]		
69	P7[5]	GPIO [unused]		
70	VDDIO1	VDDIO1	Power	
71	VRF	VRF	Power	
72	VSS	VSS	Power, Dedicated	
73	VDD_NS	VDD_NS	Power	
74	P13[0]	GPIO [unused]		
75	P12[7]	GPIO [unused]		
76	P7[4]	GPIO [unused]		
77	P7[3]	GPIO [unused]		
78	P7[2]	GPIO [unused]		
79	VSS	VSS	Power, Dedicated	
80	P7[1]	GPIO [unused]		
81	VSSR	VSSR	Dedicated	
82	P1[5]	OVT IO [unused]		
83	P1[4]	OVT IO [unused]		
84	P1[3]	OVT IO [unused]		
85	P1[2]	OVT IO [unused]		
86	P5[2]	CY_EINK_DispRst	Software In/Out	Strong drive
87	P5[4]	CY_EINK_DispEn	Software In/Out	Strong drive
88	P6[1]	GPIO [unused]		
89	P6[4]	GPIO [unused]		
90	P7[0]	GPIO [unused]		
91	ANT	ANT	Dedicated	
92	VSSR	VSSR	Dedicated	
93	VSSR	VSSR	Dedicated	
94	VSSR	VSSR	Dedicated	
95	VSSR	VSSR	Dedicated	

Pin	Port	Name	Type	Drive Mode
96	P5[1]	GPIO [unused]		
97	P5[3]	CY_EINK_DispBusy	Software In/Out	HiZ analog
98	P6[0]	GPIO [unused]		
99	P6[3]	GPIO [unused]		
100	P6[7]	GPIO [unused]	Dgtl In	Res pull down
101	VSSR	VSSR	Dedicated	
102	VDDR1	VDDR1	Dedicated	
103	VSSR	VSSR	Dedicated	
104	VSSR	VSSR	Dedicated	
105	VSSR	VSSR	Dedicated	
106	P5[0]	GPIO [unused]		
107	VDDR_HVL	VDDR_HVL	Power, Dedicated	
108	P5[5]	CY_EINK_Discharge	Software In/Out	Strong drive
109	P6[2]	GPIO [unused]		
110	P6[6]	GPIO [unused]	Dgtl In	Res pull up
111	VDDR2	VDDR2	Dedicated	
112	VDDR3	VDDR3	Dedicated	
113	VSSR	VSSR	Dedicated	
114	XI	XI	Dedicated	
115	XO	XO	Dedicated	
116	DVDD	DVDD	Dedicated	
117	VDCDC	VDCDC	Dedicated	
118	VSSR	VSSR	Dedicated	
119	P5[6]	CY_EINK_Border	Software In/Out	Strong drive
120	P6[5]	GPIO [unused]		

Abbreviations used in Table 3 have the following meanings:

- Dgtl Out = Digital Output
- HiZ analog = High impedance analog
- Res pull up = Resistive pull up
- Dgtl In = Digital Input
- Res pull down = Resistive pull down

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
P0[0]	22	GPIO [unused]		
P0[1]	33	GPIO [unused]		
P0[2]	44	CY_EINK_DisploEn	Software In/Out	Strong drive
P0[3]	43	GPIO [unused]		
P0[4]	53	SW2	Dgtl In	Res pull up
P0[5]	32	GPIO [unused]		
P1[0]	63	OVT IO [unused]		
P1[1]	52	GreenLED	Dgtl Out	Res pull up
P1[2]	85	OVT IO [unused]		
P1[3]	84	OVT IO [unused]		
P1[4]	83	OVT IO [unused]		
P1[5]	82	OVT IO [unused]		
P10[0]	18	GPIO [unused]		
P10[1]	8	GPIO [unused]		
P10[2]	56	GPIO [unused]		
P10[3]	46	GPIO [unused]		
P10[4]	36	GPIO [unused]		
P10[5]	17	GPIO [unused]		
P10[6]	7	GPIO [unused]		
P11[0]	55	GPIO [unused]		
P11[1]	45	GPIO [unused]		
P11[2]	35	GPIO [unused]		
P11[3]	26	GPIO [unused]		
P11[4]	16	GPIO [unused]		
P11[5]	6	GPIO [unused]		
P11[6]	15	GPIO [unused]		
P11[7]	5	GPIO [unused]		
P12[0]	4	\CY_EINK_SPIM:mosi_m\	Dgtl Out	Strong drive
P12[1]	14	\CY_EINK_SPIM:miso_m\	Dgtl Out	HiZ analog
P12[2]	24	\CY_EINK_SPIM:sclk_m\	Dgtl Out	Strong drive
P12[3]	3	CY_EINK_Ssel	Software In/Out	Strong drive
P12[4]	25	GPIO [unused]		
P12[5]	34	GPIO [unused]		
P12[6]	65	GPIO [unused]		
P12[7]	75	GPIO [unused]		
P13[0]	74	GPIO [unused]		
P13[1]	64	GPIO [unused]		
P13[6]	54	GPIO [unused]		
P13[7]	23	GPIO [unused]		
P5[0]	106	GPIO [unused]		
P5[1]	96	GPIO [unused]		
P5[2]	86	CY_EINK_DispRst	Software In/Out	Strong drive

Port	Pin	Name	Type	Drive Mode
P5[3]	97	CY_EINK_DispBusy	Software In/Out	HiZ analog
P5[4]	87	CY_EINK_DispEn	Software In/Out	Strong drive
P5[5]	108	CY_EINK_Discharge	Software In/Out	Strong drive
P5[6]	119	CY_EINK_Border	Software In/Out	Strong drive
P6[0]	98	GPIO [unused]		
P6[1]	88	GPIO [unused]		
P6[2]	109	GPIO [unused]		
P6[3]	99	GPIO [unused]		
P6[4]	89	GPIO [unused]		
P6[5]	120	GPIO [unused]		
P6[6]	110	GPIO [unused]	Dgtl In	Res pull up
P6[7]	100	GPIO [unused]	Dgtl In	Res pull down
P7[0]	90	GPIO [unused]		
P7[1]	80	GPIO [unused]		
P7[2]	78	GPIO [unused]		
P7[3]	77	GPIO [unused]		
P7[4]	76	GPIO [unused]		
P7[5]	69	GPIO [unused]		
P7[6]	68	GPIO [unused]		
P7[7]	67	GPIO [unused]		
P8[0]	60	GPIO [unused]		
P8[1]	59	GPIO [unused]		
P8[2]	58	GPIO [unused]		
P8[3]	57	GPIO [unused]		
P8[4]	66	GPIO [unused]		
P8[5]	49	GPIO [unused]		
P8[6]	48	GPIO [unused]		
P8[7]	47	GPIO [unused]		
P9[0]	40	GPIO [unused]		
P9[1]	39	GPIO [unused]		
P9[2]	38	GPIO [unused]		
P9[3]	37	GPIO [unused]		
P9[4]	30	GPIO [unused]		
P9[5]	29	GPIO [unused]		
P9[6]	28	GPIO [unused]		
P9[7]	27	GPIO [unused]		

Abbreviations used in Table 4 have the following meanings:

- Dgtl In = Digital Input
- Res pull up = Resistive pull up
- Dgtl Out = Digital Output
- HiZ analog = High impedance analog
- Res pull down = Resistive pull down

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
\CY_EINK_SPIM:miso_m\	P12[1]	Dgtl Out
\CY_EINK_SPIM:mosi_m\	P12[0]	Dgtl Out
\CY_EINK_SPIM:sclk_m\	P12[2]	Dgtl Out
CY_EINK_Border	P5[6]	Software In/Out
CY_EINK_Discharge	P5[5]	Software In/Out
CY_EINK_DispBusy	P5[3]	Software In/Out
CY_EINK_DispEn	P5[4]	Software In/Out
CY_EINK_DispIoEn	P0[2]	Software In/Out
CY_EINK_DispRst	P5[2]	Software In/Out
CY_EINK_Ssel	P12[3]	Software In/Out
GPIO [unused]	P6[5]	
GPIO [unused]	P7[5]	
GPIO [unused]	P6[6]	Dgtl In
GPIO [unused]	P5[1]	
GPIO [unused]	P12[6]	
GPIO [unused]	P13[1]	
GPIO [unused]	P6[4]	
GPIO [unused]	P7[6]	
GPIO [unused]	P7[7]	
GPIO [unused]	P8[4]	
GPIO [unused]	P6[2]	
GPIO [unused]	P7[1]	
GPIO [unused]	P5[0]	
GPIO [unused]	P7[2]	
GPIO [unused]	P6[3]	
GPIO [unused]	P6[7]	Dgtl In
GPIO [unused]	P6[0]	
GPIO [unused]	P7[0]	
GPIO [unused]	P13[0]	
GPIO [unused]	P6[1]	
GPIO [unused]	P7[3]	
GPIO [unused]	P7[4]	
GPIO [unused]	P12[7]	
GPIO [unused]	P9[5]	
GPIO [unused]	P9[4]	
GPIO [unused]	P9[6]	
GPIO [unused]	P11[3]	
GPIO [unused]	P9[7]	
GPIO [unused]	P11[7]	

Name	Port	Type
GPIO [unused]	P11[2]	
GPIO [unused]	P12[5]	
GPIO [unused]	P0[5]	
GPIO [unused]	P0[1]	
GPIO [unused]	P11[6]	
GPIO [unused]	P11[4]	
GPIO [unused]	P10[1]	
GPIO [unused]	P11[5]	
GPIO [unused]	P10[6]	
GPIO [unused]	P13[7]	
GPIO [unused]	P12[4]	
GPIO [unused]	P0[0]	
GPIO [unused]	P10[5]	
GPIO [unused]	P10[0]	
GPIO [unused]	P13[6]	
GPIO [unused]	P11[0]	
GPIO [unused]	P8[5]	
GPIO [unused]	P8[7]	
GPIO [unused]	P8[6]	
GPIO [unused]	P8[1]	
GPIO [unused]	P8[0]	
GPIO [unused]	P8[2]	
GPIO [unused]	P10[2]	
GPIO [unused]	P8[3]	
GPIO [unused]	P10[3]	
GPIO [unused]	P9[2]	
GPIO [unused]	P9[1]	
GPIO [unused]	P9[3]	
GPIO [unused]	P10[4]	
GPIO [unused]	P0[3]	
GPIO [unused]	P9[0]	
GPIO [unused]	P11[1]	
GreenLED	P1[1]	Dgtl Out
OVT IO [unused]	P1[5]	
OVT IO [unused]	P1[4]	
OVT IO [unused]	P1[0]	
OVT IO [unused]	P1[2]	
OVT IO [unused]	P1[3]	
SW2	P0[4]	Dgtl In

Abbreviations used in Table 5 have the following meanings:

- Dgtl Out = Digital Output
- Dgtl In = Digital Input

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Allow but warn

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Embedded Trace (ETM)	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

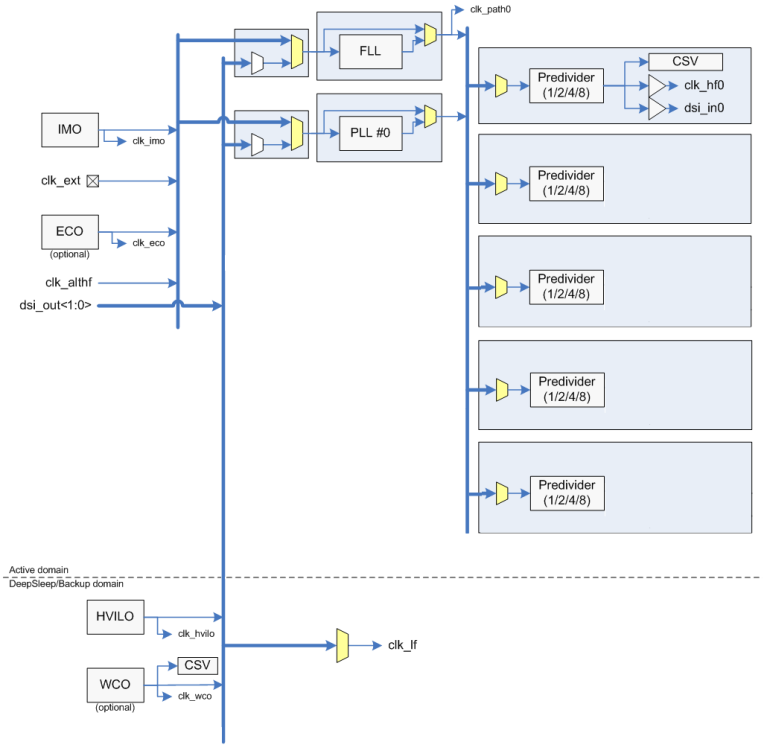
Name	Value
Power Mode	1.1V LDO Linear Regulator
External PMIC Output	Disabled
vBackup Source	VDDD
VBACKUP (V)	3.3
VDD_NS (V)	3.3
VDDA (V)	3.3
VDDD (V)	3.3
VDDIO0 (V)	3.3
VDDIO1 (V)	3.3
VDDR_HVL (V)	3.3
Variable VDDA	False

4 Clocks

The clock system includes these clock resources:

- Multiple internal clock sources:
  - 8 MHz Internal Main Oscillator (IMO) ±1%
  - 32 kHz Internal Low Speed Oscillator (ILO) ±30% output
  - 32.768 kHz Precision Internal Low Speed Oscillator (PILO) ±2% output
- Internal FLL and PLL can be used to increase frequency generated by HF clock sources
- Source clocks, FLL, and PLL can be used to drive 5 separate HF clocks
- HFCLK0 can be used to drive peripherals and UDBs
- LFCLK is typically used for DeepSleep wakeup timer

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
Clk_HF0	NONE	FLL	100 MHz	100 MHz	±2.4	True	True
Clk_Peri	NONE	Clk_HF0	100 MHz	100 MHz	±2.4	True	True
Clk_Fast	NONE	Clk_HF0	100 MHz	100 MHz	±2.4	True	True
FLL	NONE	PathMux0	100 MHz	100 MHz	±2.4	True	True
Clk_Slow	NONE	Clk_Peri	50 MHz	50 MHz	±2.4	True	True
Clk_Pump	NONE	FLL	25 MHz	25 MHz	±2.4	True	True
PathMux4	NONE	IMO	8 MHz	8 MHz	±1	True	True
Clk_Timer	NONE	IMO	8 MHz	8 MHz	±1	True	True
IMO	NONE		8 MHz	8 MHz	±1	True	True
PathMux3	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux0	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux1	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux2	NONE	IMO	8 MHz	8 MHz	±1	True	True
Clk_Bak	NONE	Clk_LF	32 kHz	32 kHz	±10	True	True
Clk_LF	NONE	ILO	32 kHz	32 kHz	±10	True	True
ILO	NONE		32 kHz	32 kHz	±10	True	True
Clk_AltSysTick	NONE	Clk_LF	32 kHz	32 kHz	±10	True	True
PILO	NONE		32.768 kHz	? MHz	±2	False	False
Clk_HF1	NONE	FLL	? MHz	? MHz	±0	False	False
ExtClk	NONE		24 MHz	? MHz	±0	False	False
WCO	NONE		32.768 kHz	? MHz	±0.015	False	False
Clk_HF2	NONE	FLL	? MHz	? MHz	±0	False	False
Clk_HF3	NONE	FLL	? MHz	? MHz	±0	False	False
PLL0	NONE	PathMux1	100 MHz	? MHz	±0	False	False
DigSig2	NONE		? MHz	? MHz	±0	False	False
ECO	NONE		24 MHz	? MHz	±0	False	False
AltHF	NONE		32 MHz	? MHz	±0	False	False
Clk_HF4	NONE	FLL	? MHz	? MHz	±0	False	False
DigSig1	NONE		? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

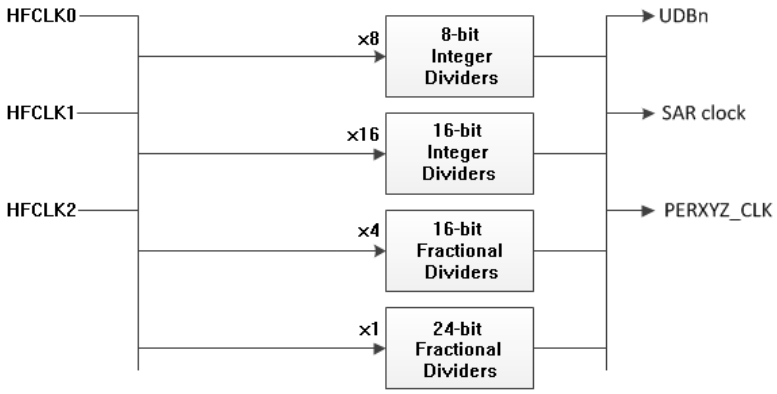


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
CY_EINK_-SPIM_SCBCLK	UNKNOWN	Clk_Peri	100 MHz	100 MHz	±2.4	True	True
PWM_CLOCK	UNKNOWN	Clk_Peri	20 kHz	20 kHz	±2.4	True	True
EINK_Clock	UNKNOWN	Clk_Peri	2 kHz	2 kHz	±2.4	True	True
Clock_2	UNKNOWN	Clk_Peri	100 Hz	100 Hz	±2.4	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 6 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CySysClkImo API routines
  - CySysClkIlo API routines
  - CySysClkEco API routines
  - CySysClkWco API routines
  - CySysClkWrite API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	CortexM0p Vector	CortexM0p Priority	CortexM4 Vector	CortexM4 Priority	Deep Sleep Wakeup Capable
CY_EINK_SPIM_SCB_IRQ	47			47	7	No

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 6 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 6 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

This design has no flash protection specified; all blocks are unprotected.

For more information on Flash memory and protection, please refer to:

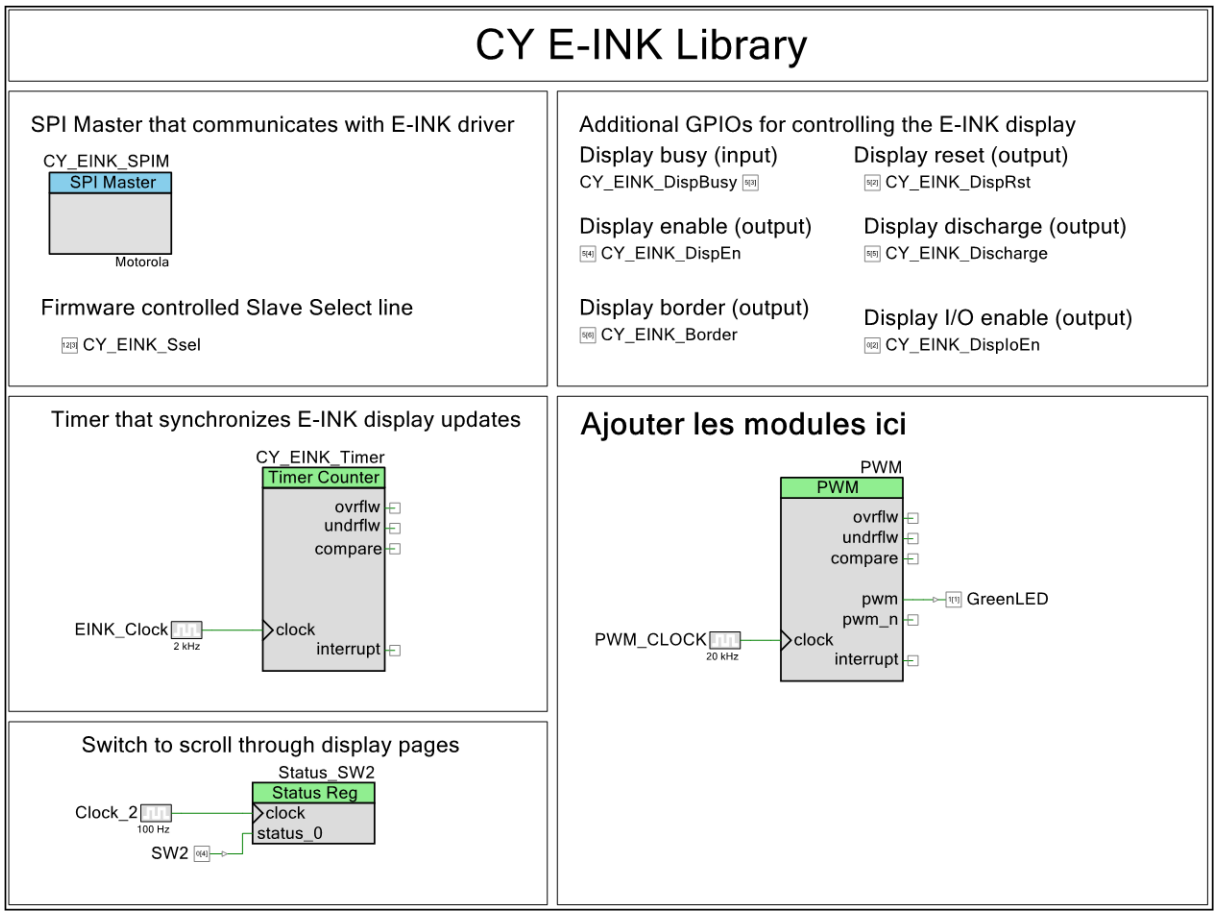
- Flash Protection chapter in the PSoC 6 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CySysFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: CY_eInk_Library

Figure 5. Schematic Sheet: CY_eInk_Library



This schematic sheet contains the following component instances:

- Instance CY_EINK_SPIM (type: SCB_SPI_PDL_v2_0)
- Instance CY_EINK_Timer (type: TCPWM_Counter_PDL_v1_0)
- Instance PWM (type: TCPWM_PWM_PDL_v1_0)
- Instance Status_SW2 (type: CyStatusReg_v1_90)

8 Components

8.1 Component type: CyStatusReg [v1.90]

8.1.1 Instance Status_SW2

Description: The Status Register allows the firmware to read values from digital signals.
Instance type: CyStatusReg [v1.90]
Datasheet: online component datasheet for CyStatusReg

Table 12. Component Parameters for Status_SW2

Parameter Name	Value	Description
Bit0Mode	Transparent	Bit Mode for Bit 0 of the Status Register
Bit1Mode	Transparent	Bit Mode for Bit 1 of the Status Register
Bit2Mode	Transparent	Bit Mode for Bit 2 of the Status Register
Bit3Mode	Transparent	Bit Mode for Bit 3 of the Status Register
Bit4Mode	Transparent	Bit Mode for Bit 4 of the Status Register
Bit5Mode	Transparent	Bit Mode for Bit 5 of the Status Register
Bit6Mode	Transparent	Bit Mode for Bit 6 of the Status Register
Bit7Mode	Transparent	Bit Mode for Bit 7 of the Status Register
BusDisplay	false	Displays the input terminals as bus
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Interrupt	false	Shows the interrupt terminal
MaskValue	0	Defines the value of the interrupt mask
NumInputs	1	Defines the number of status inputs (1-8)
User Comments		Instance-specific comments.

8.2 Component type: SCB_SPI_PDL [v2.0]

8.2.1 Instance CY_EINK_SPIM

Description: SPI (SCB) communications interface
Instance type: SCB_SPI_PDL [v2.0]
Datasheet: online component datasheet for SCB_SPI_PDL

Table 13. Component Parameters for CY_EINK_SPIM

Parameter Name	Value	Description
Bit Order	MSB First	This parameter defines the direction in which the serial data is transmitted. When set to the MSB first, the most-significant bit is transmitted first. When set to the LSB first, the least-significant bit is transmitted first.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Data Rate (kbps)	20000	This parameter specifies the data rate in kbps. The actual data rate may differ based on the available clock frequency and component settings. This parameter has no effect if the Enable Clock From Terminal parameter is true. The range: 1-25000 kbps.
Deassert SS Between Data Elements	false	This parameter determines if individual data transfers are separated by the slave select de-selection.
Enable Clock from Terminal	false	This parameter provides a clock terminal to connect a clock outside the component.
Enable Input Glitch Filter	false	This parameter applies a digital 3-tap median filter to the SPI input lines.
Enable MISO Late Sampling	false	This option allows the master to sample the MISO signal by half of the SCLK period later (on the alternate serial clock edge). Late sampling addresses the round-trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master.
Interrupt	Internal	This parameter allows choosing between Internal and External placement of the Interrupt Component.
Mode	Master	This parameter specifies the mode of the SPI operation as: the slave or master.
Number of SS	0	This parameter determines the number of the slave-select lines. The slave has a single slave-select line. The master has up to 4 lines. The range: 1-4.

Parameter Name	Value	Description
Oversample	5	This parameter defines how many Component clocks are used to generate the SCLK period (only applicable for the master mode). When the oversample is even the first and second phase of the clock period are the same. Otherwise the first phase of the clock signal period is one component's clock cycle longer than the second phase. The range: 4-16 (MISO presents) and 2-16 (MISO is removed).
Remove MISO	false	This option allows a removal of the MISO pin from the SPI interface
Remove MOSI	false	This option allows a removal of the MOSI pin from the SPI interface.
Remove SCLK	false	This option allows a removal of the SCLK pin from the SPI interface.
RX Data Width	8	This option defines the width of a single data element for the RX direction in bits. This number must match with TX Word Width for all SPI sub-modes except National Semiconductor (Microwire). The range: 4-16.
RX Output	false	This parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA trigger input or left unconnected.
SCLK Free Running	false	This parameter allows the master to generate SCLK continually. It is useful when the master SCLK is connected to the slave device which uses it for functional operation rather than only the SPI functionality.
SCLK Mode	CPHA = 0, CPOL = 0	This parameter specifies the serial clock phase (CPHA) and polarity (CPOL) combination.
Show SPI Terminals	false	This parameter removes internal pins and expose signals to terminals. These terminals must be connected to the pins or SmartIO component.
Sub Mode	Motorola	This parameter specifies the sub-mode of the SPI as: Motorola, TI (Start Coincides), TI (Start Precedes), or National Semiconductor (Microwire

Parameter Name	Value	Description
TX Data Width	8	This option defines the width of a single data element for the TX direction in bits. This number must match with RX Word Width for all SPI sub-modes except National Semiconductor (Microwire). The range: 4-16.
TX Output	false	This parameter enables the TX trigger output terminal of the component. This terminal must be connected to the DMA trigger input or left unconnected.
User Comments		Instance-specific comments.

8.3 Component type: TCPWM_Counter_PDL [v1.0]

8.3.1 Instance CY_EINK_Timer

Description: This component implements a Timer/Counter using the TCPWM hardware block
Instance type: TCPWM_Counter_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_Counter_PDL

Table 14. Component Parameters for CY_EINK_Timer

Parameter Name	Value	Description
Clock Prescaler	Divide by 2	Divides down the input clock
Compare 0	5000	Sets the compare value. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Compare or Capture	Compare	Selects the mode for the compare capture register
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Direction	Up	Selects the direction the counter counts
Count Input	Disabled	Determines if a count input is needed and how that input is registered
Enable Compare Swap	false	When selected the compare register is swapped between compare 0 and compare 1 each time the comparison is true
Interrupt Source	None	Selects which events can trigger an interrupt
Period	10000	Sets the period of the Timer/Counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered
Resolution	16-bits	Selects the size of the counter

Parameter Name	Value	Description
Run Mode	One Shot	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered
Stop Input	Disabled	Determines if a stop input is needed and how that input is registered
User Comments		Instance-specific comments.

8.4 Component type: TCPWM_PWM_PDL [v1.0]

8.4.1 Instance PWM

Description: This component implements a PWM using the TCPWM hardware block
Instance type: TCPWM_PWM_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_PWM_PDL

Table 15. Component Parameters for PWM

Parameter Name	Value	Description
Clock Prescaler	Divide by 1	Divides down the input clock
Compare 0	1	Sets the compare value. When the count value equals the compare the compare output pulses high. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Input	Disabled	Determines if a count input is needed and how that input is registered
Enable Compare Swap	false	When selected the compare register is swapped between compare 0 and compare 1 on the next OV/UN after the swap is registered
Enable Period Swap	false	If checked the periods will be swapped at the next OV/UN when a swap event has been registered
Interrupt Source	None	Selects which events can trigger an interrupt
Invert PWM Output	false	If checked the main PWM output is inverted
Invert PWM_n Output	false	If checked the main PWM_n output is inverted
Kill Input	Disabled	Determines how the kill input behaves
Kill Mode	Stop on Kill	Determines what the kill signal does to the PWM

Parameter Name	Value	Description
Period 0	1000	Sets the period of the counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
PWM Alignment	Left Aligned	Selects which direction the PWM counts in. Left = Up, Right = Down, Center/Asymmetric = Up/Down
PWM Mode	PWM	Selects the PWM mode of operation
PWM Resolution	16-bits	Selects the width of the PWM
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered
Run Mode	Continuous	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered
Swap Input	Disabled	This input controls when compare and period swaps occur
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 6 register map is covered in the PSoC 6 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 6 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 6 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines