

Table 42. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
$f_{\text{PLL_IN}}$	PLL input clock ⁽¹⁾	1 ⁽²⁾	8.0	24 ⁽²⁾	MHz
	PLL input clock duty cycle	40 ⁽²⁾	-	60 ⁽²⁾	%
$f_{\text{PLL_OUT}}$	PLL multiplier output clock	16 ⁽²⁾	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200 ⁽²⁾	μs
Jitter _{PLL}	Cycle-to-cycle jitter	-	-	300 ⁽²⁾	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by $f_{\text{PLL_OUT}}$.
2. Guaranteed by design, not tested in production.