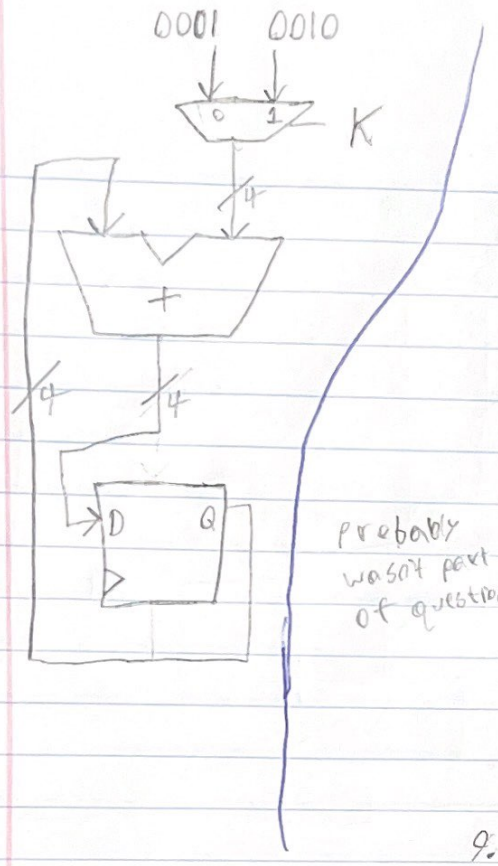

9.

probably wasn't part of question

9. DRAM (Dynamic Random access memory) is a type of semiconductor memory. Random access is needed to directly access a part of memory directly instead of going through everything one by one till you find what you are looking for. DRAM is different from other types of Ram because it is dynamic, meaning it needs to be "refreshed" with an electronic charge every few milliseconds to make up for leaking charge from the capacitor

9.a) RowHammering is a security exploit that takes advantage of DRAM, DRAM cells are stored very densly, repeatedly activating rows of memory can cause electrical charges to leak resulting in random bit flips. like "hammering" a row.

Sources: margret Rouse, Techopedia
Alexander S. Gillis, Techtarget

9.b) ReRAM (Resistive RAM) is exciting because it is a non-volatile memory with low power consumption and fast write. ReRAM is is a base for in-memory computing architectures which can be used to get over the challenges of implementing machine learning. A major problem being fetching data and writing it back and experiencing a memory-wall Bottleneck

Source: ReRam Based machine Learning, Hao YU

CE HW 5

1. The problematic situation is when both R and S inputs are zero then you attempt to change both to a 1 at the same time to hold the value but this causes an oscillating Loop

3. Moores Law: Theory that number of transistors, will double every 2 years, start: 1876 End: soon probably (In an Integrated Circuit)
Dennard Scaling: As transistors get smaller their power density stays constat, so that the power stays proportional to area

4. It stopped mainly due to supply voltage limits, As transistor get smaller, density got too much and on-chip resources needed to stay dark

6. D-flipflops are: made of D-latches which can never have an oscillatory condition. D-flipflops also only change state at the rising clock edge which is helpful in making Datapaths and eliminating noise

7. $2^{14} \times 8$, there are 32,768 nibbles of storage: $\frac{2^{14} \times 8}{4}$

32000 Decoder: 14 inputs for the address with 1 output to select a row
MUXS: 2^{14} inputs one for each row, one output, 14 bit selector input (ther would be 8 muxs

8.