CE387: Real-Time Digital Systems Design and Verification with FPGAs
Professor David Zaretsky
Assignment 3
Motion Detection

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Simulation Results

- **Clock cycle count:** 884745 cycles (got from keeping track in testbench)
- **Errors reported:** 0 (Testbench output confirmed 0 errors for all blocks).

Synthesis Results

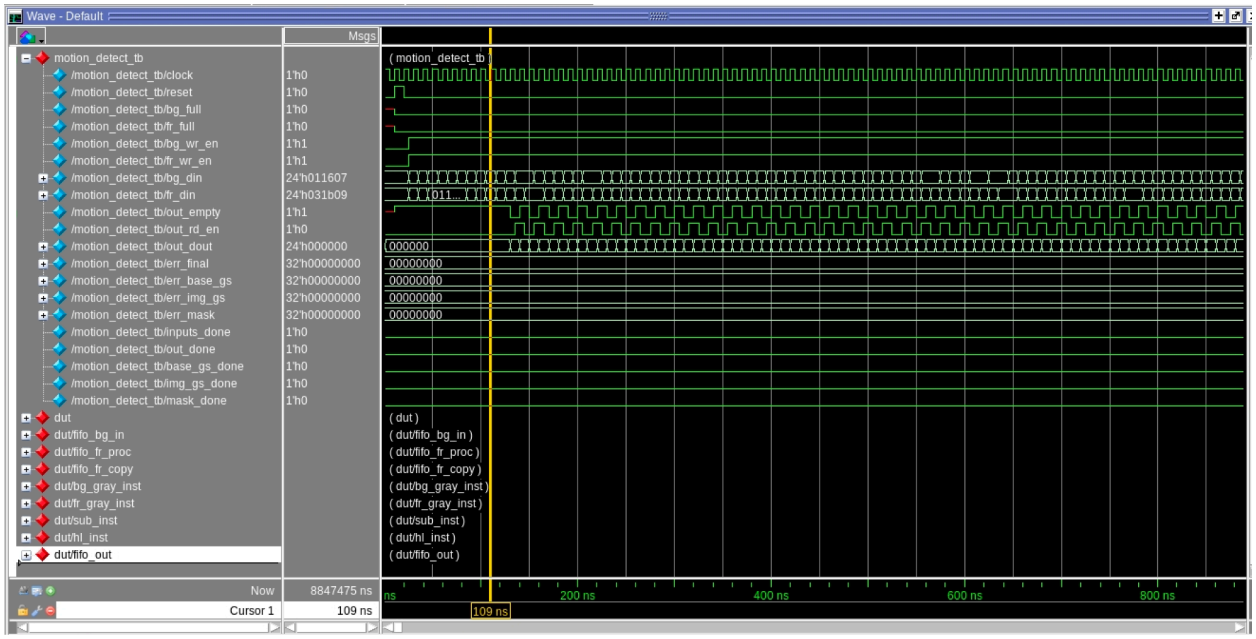
- **Maximum frequency**: The synthesis report estimates a maximum operating frequency of 74.4 MHz.
- **Registers /LUTs/Logic Elements**: The design utilizes a total of 206 registers on the device. It also consumes 567 combinational functions (Logic Elements/LUTs).
- **Memory utilization**: The design uses 122880 memory bits
- **Multipliers (DSPs)**: No Digital Signal Processing blocks implemented
- **Worst path (timing analysis)**: The worst path has a negative slack of -2.016 nanoseconds with a total 13.438 ns delay. This critical timing path begins at fifo_bg_in.fifo_buf / q_b[16] (Output of the Background Input FIFO) and ends at bg_gray_inst.gs[0] / d (Input to a register in the Background Grayscale module) with 23 logic levels.
- **Schematic architecture (RTL)**: This is a streaming architecture with FIFOs used to transfer data into and out of functional blocks and allowing blocks to interact. There were three pipelined paths for data to flow through before converging to a final output. Each functional block consists of an FSM using the 2-process method.

The implemented motion detection system utilizes a streaming hardware architecture to identify moving objects by comparing an image frame against a static background. Using the vector sum and grayscale streaming examples as reference, my design features a modular pipeline with three parallel data paths: background processing, frame processing, and frame copy. The system splits the incoming frame data, converting one path to grayscale for processing while buffering the original color data in a FIFO for later recombination. The background and frame grayscale streams converge at the subtract_background module, where a binary motion mask is created. This mask is then used by the highlight_image module to overlay a red highlight onto the preserved original frame.

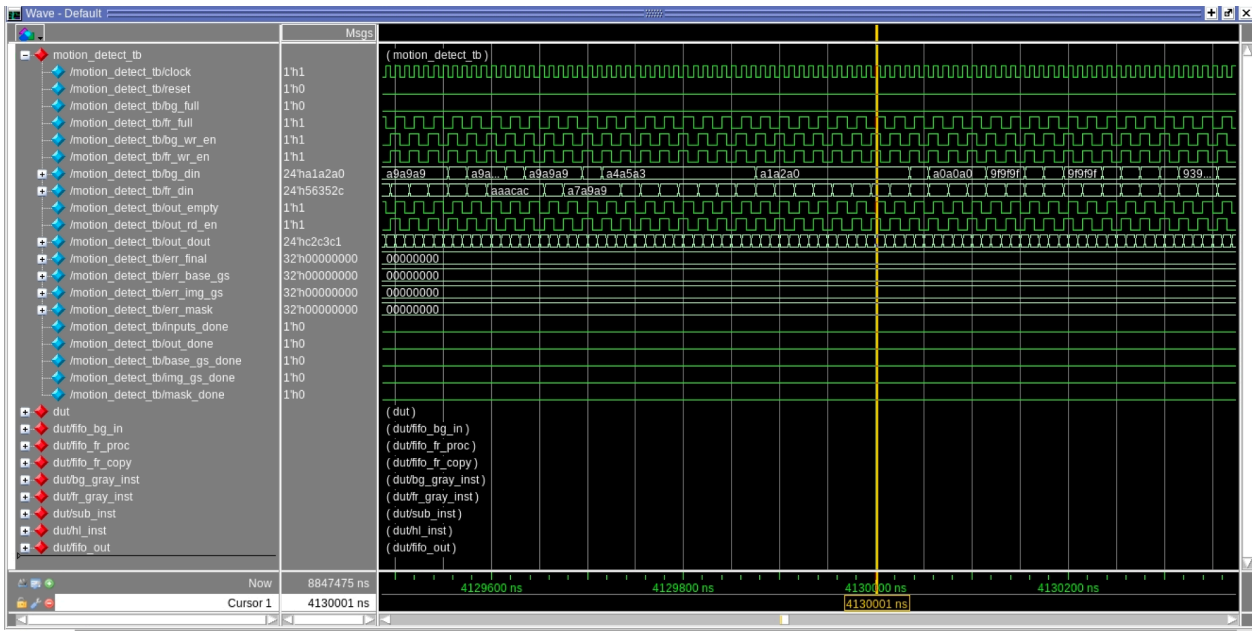
A primary challenge encountered was when running simulation, the top of the output image kept being unprocessed. I first thought this was because the FIFO buffering the original frame was too shallow (64 elements) to accommodate the latency of the parallel processing path so I increased it to 1024. But I was still having the same issues, after looking into it I saw that I had incorrect dimensions in the testbench (720x540 instead of 768x576), which ended the simulation early as the processing was done bottom up

The design successfully met all project requirements through its pipelined, self-clocking architecture. Strict streaming protocols were enforced by encapsulating all inter-module communication within FIFOs, effectively managing data transfer across the diverging and converging paths. Each module was implemented using the 2-process FSM structure. The system achieves O(N) processing time by operating as a continuous pipeline with an initiation interval of one clock cycle per pixel, and bit-true accuracy was verified by comparing the simulation output with the C-generated bmp files and there were zero differences.

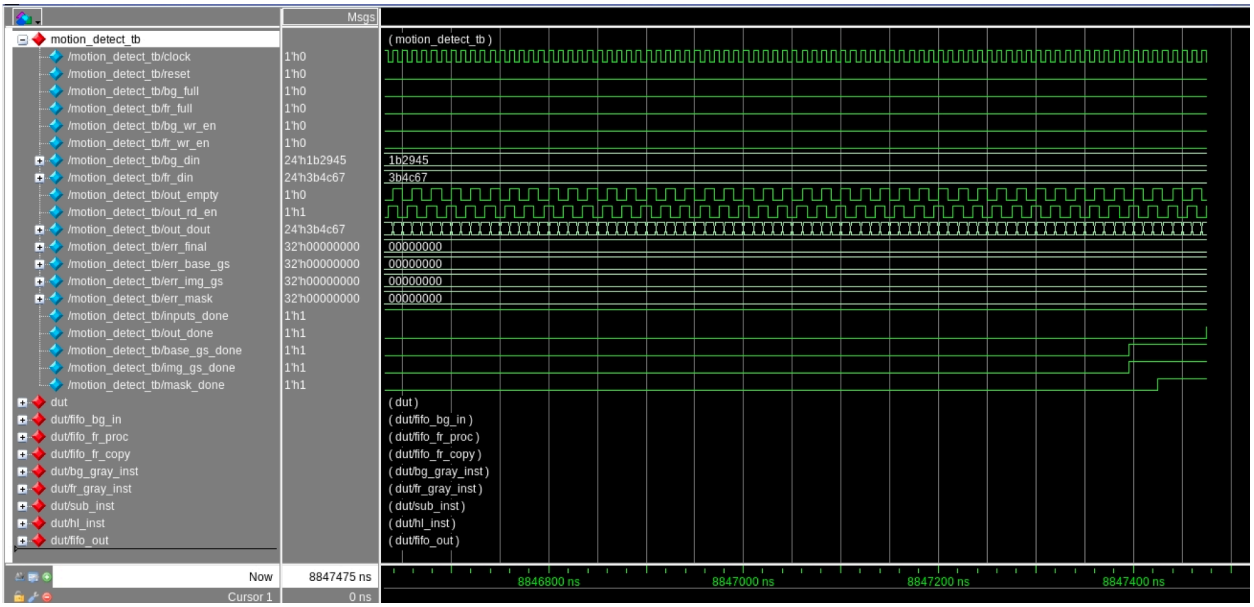
Simulation Start:



Simulation Mid:



Simulation End:



Synthesis Screenshot

Project Settings			
Project Name	motion_detect	Device Name	rev_1: Intel CYCLONE IV E : EP4CE115
Implementation Name	rev_1	Top Module	motion_detect_top
Pipelining	1	Retiming	0
Resource Sharing	1	Fanout Guide	30
Disable I/O Insertion	0	Disable Sequential Optimizations	0
Clock Conversion	1	FSM Compiler	1

Run Status

Job Name	Status				CPU Time	Real Time	Memory	Date/Time
Compile Input (compiler) Detailed report	out-of-date	41	1	0	-	00m:01s	-	1/30/26 9:59 PM
Premap (premap) Detailed report	Complete *	8	2	0	0m:00s	0m:00s	118MB	1/30/26 9:53 PM
Map & Optimize (fpga_mapper) Detailed report	Complete *	133	9	0	0m:03s	0m:03s	155MB	1/30/26 9:53 PM

Area Summary

LUTs for combinational functions (total_luts)	567	Non I/O Registers (non_io_reg)	206
I/O Pins	80	I/O registers (total_io_reg)	0
DSP Blocks (dsp_used)	0 (266)	Memory Bits	122880
Detailed report		Hierarchical Area report	

Timing Summary

Clock Name (clock_name)	Req Freq (req_freq)	Est Freq (est_freq)	Slack (slack)
motion_detect_top|clock	87.5 MHz	74.4 MHz	-2.016
Detailed report		Timing Report View	

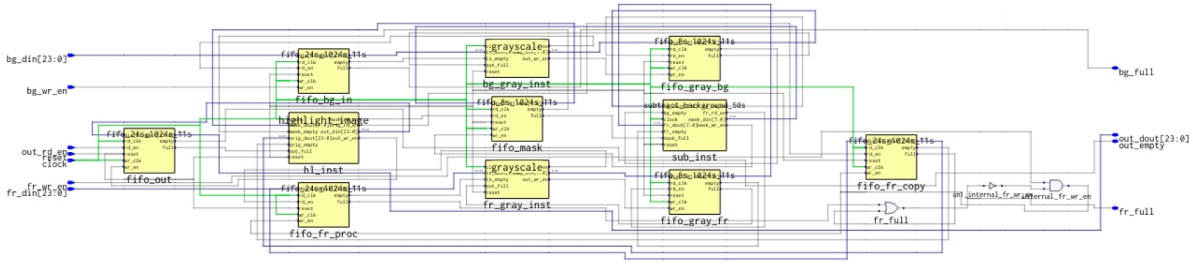
Optimizations Summary

Combined Clock Conversion	1 / 0 more

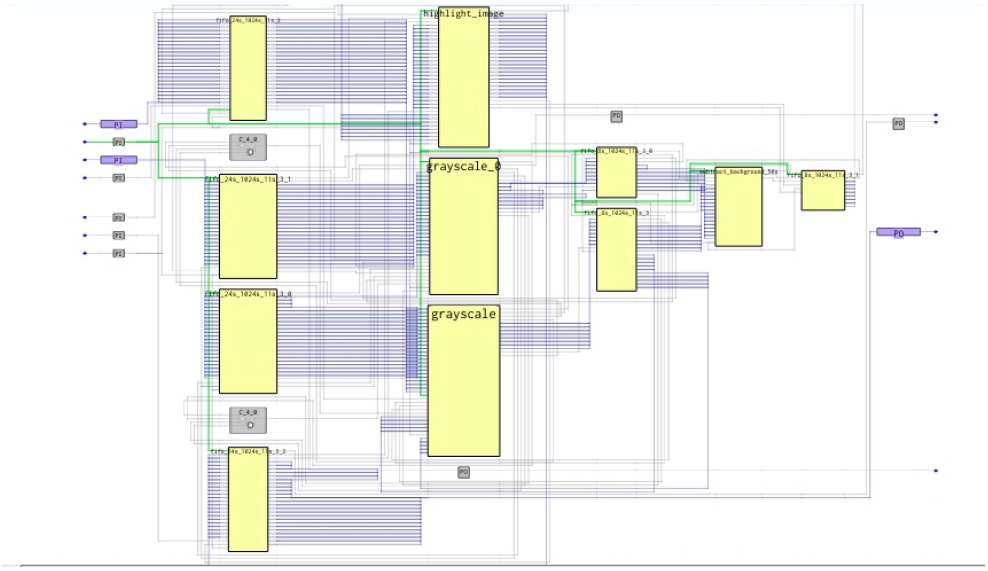
Hierarchical Area Report:

Module name	ATOMS	ARITHMETIC MC	REGISTERS	SYNC RAMS	MACs
motion_detect_top	234	0	206	7	0
fifo_24s_1024s_11s_3	19	0	23	1	0
fifo_24s_1024s_11s_3_0	19	0	23	1	0
fifo_24s_1024s_11s_3_1	18	0	23	1	0
fifo_24s_1024s_11s_3_2	17	0	23	1	0
fifo_8s_1024s_11s_3	12	0	23	1	0
fifo_8s_1024s_11s_3_0	16	0	23	1	0
fifo_8s_1024s_11s_3_1	16	0	23	1	0
grayscale	28	0	9	0	0
grayscale_0	26	0	9	0	0
highlight_image	39	0	25	0	0
subtract_background_50s	22	0	2	0	0

RTL Hierarchical:



Technology Hierarchical:



RTL Flattened: