CE387
Matias Ketema

Assignment 1: Fibonacci:

I mostly followed the template and had to refer to resources because this is my first time using system verilog and synthesizing it. This design uses the two-process method to separate sequential and combinational logic, preventing latches and simplifying timing analysis. Registered outputs and an asynchronous reset are used to prevent glitches, synchronized signals and immediate initialization. The automatic transition from DONE to IDLE ensures the module is immediately ready for following operations.

Simulation Results

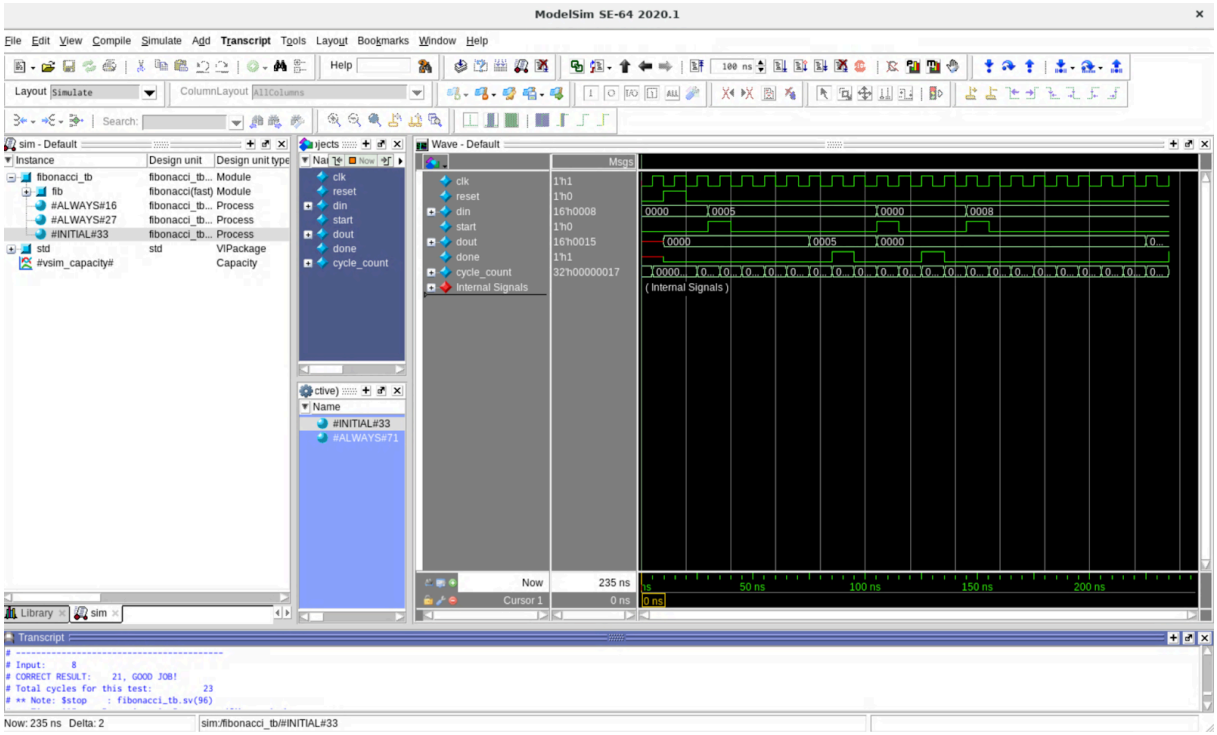
- **Clock cycle count:** 23 cycles got from keeping track in testbench
- **Errors reported:** 0 (Testbench output confirmed "CORRECT RESULT").

Synthesis Results

- **Maximum frequency**: The synthesis report estimates a maximum operating frequency of 189.8 MHz.
- **Registers /LUTs/Logic Elements**: The design utilizes a total of 67 registers on the device. It also consumes 87 combinational functions (Logic Elements/LUTs).
- **Memory utilization**: The design does not use any dedicated memory blocks. The report shows the Total ESB (Embedded System Block) usage is 0 bits.
- **Multipliers (DSPs)**: No Digital Signal Processing blocks were required. The DSP utilization is listed as 0% of the available blocks.
- **Worst path (timing analysis)**: The worst path has a negative slack of -0.790 nanoseconds with a total 5.269 ns delay. This critical timing path begins at the count[0] register and ends at the enable pin of the dout[0] register.
- **Schematic architecture (RTL)**: The architecture consists of a finite state machine with three states. It controls a 16-bit adder datapath to perform the Fibonacci calculations.

SCREENSHOTS (Next Page)

Simulation Screenshot:



Synthesis Screenshots:

Project Settings			
Project Name	proj_1	Device Name	rev_1: Intel CYCLONE IV E : EP4CE6
Implementation Name	rev_1	Top Module	[auto]
Pipelining	1	Retiming	0
Resource Sharing	1	Fanout Guide	30
Disable I/O Insertion	0	Disable Sequential Optimizations	0
Clock Conversion	1	FSM Compiler	1

Run Status

Job Name	Status				CPU Time	Real Time	Memory	Date/Time
Compile Input (compiler) Detailed report	out-of-date	37	1	0	-	00m:03s	-	1/14/26 2:22 AM
Premap (premap) Detailed report	Complete	8	2	0	0m:00s	0m:00s	118MB	1/14/26 2:22 AM
Map & Optimize (fpga_mapper) Detailed report	Complete	13	2	0	0m:00s	0m:01s	120MB	1/14/26 2:22 AM

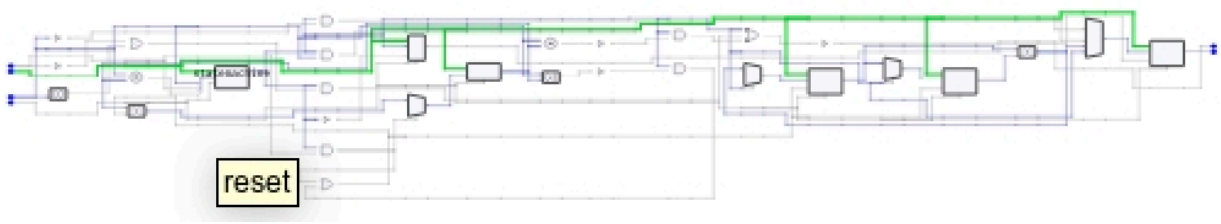
Area Summary			
LUTs for combinational functions (total_luts)	87	Non I/O Registers (non_io_reg)	67
I/O Pins	36	I/O registers (total_io_reg)	0
DSP Blocks (dsp_used)	0 (15)	Memory Bits	0
Detailed report		Hierarchical Area report	

Timing Summary

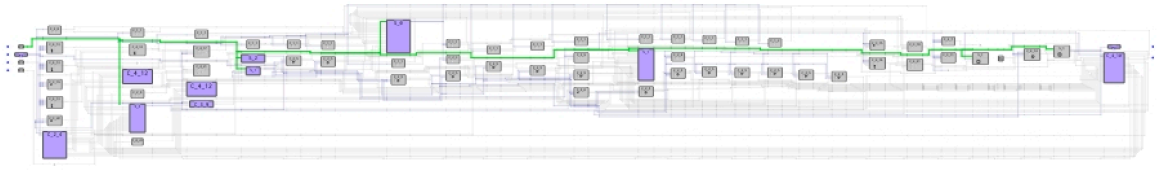
Clock Name (clock_name)	Req Freq (req_freq)	Est Freq (est_freq)	Slack (slack)
fibonacci|clk	223.3 MHz	189.8 MHz	-0.790
Detailed report			

Optimizations Summary				
Combined Clock Conversion	1 / 0 more			

RTL Hierarchical view:



Technology Hierarchical View:



Critical Path View: