PSoC® Creator™
Project Datasheet for Design01G

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Table of Contents

1 Overview

The Cypress PSoC 4 is a family of 32-bit devices with the following characteristics:

- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals such as PWM, UART, SPI and I2C
- Analog subsystem that includes 12-bit SAR ADC, comparators, op amps, CapSense, LCD drive and more
- Several types of memory elements, including SRAM and flash
- Programming and debug system through Serial Wire Debug (SWD)
- High-performance 32-bit ARM Cortex-M0 core with a nested vectored interrupt controller (NVIC)
- Flexible routing to all pins

Figure 1 shows the major components of a typical PRoC BLE series member PSoC 4 device. For details on all the systems listed above, please refer to the PSoC 4 Technical Reference Manual .

Figure 1. PRoC BLE Device Series Block Diagram

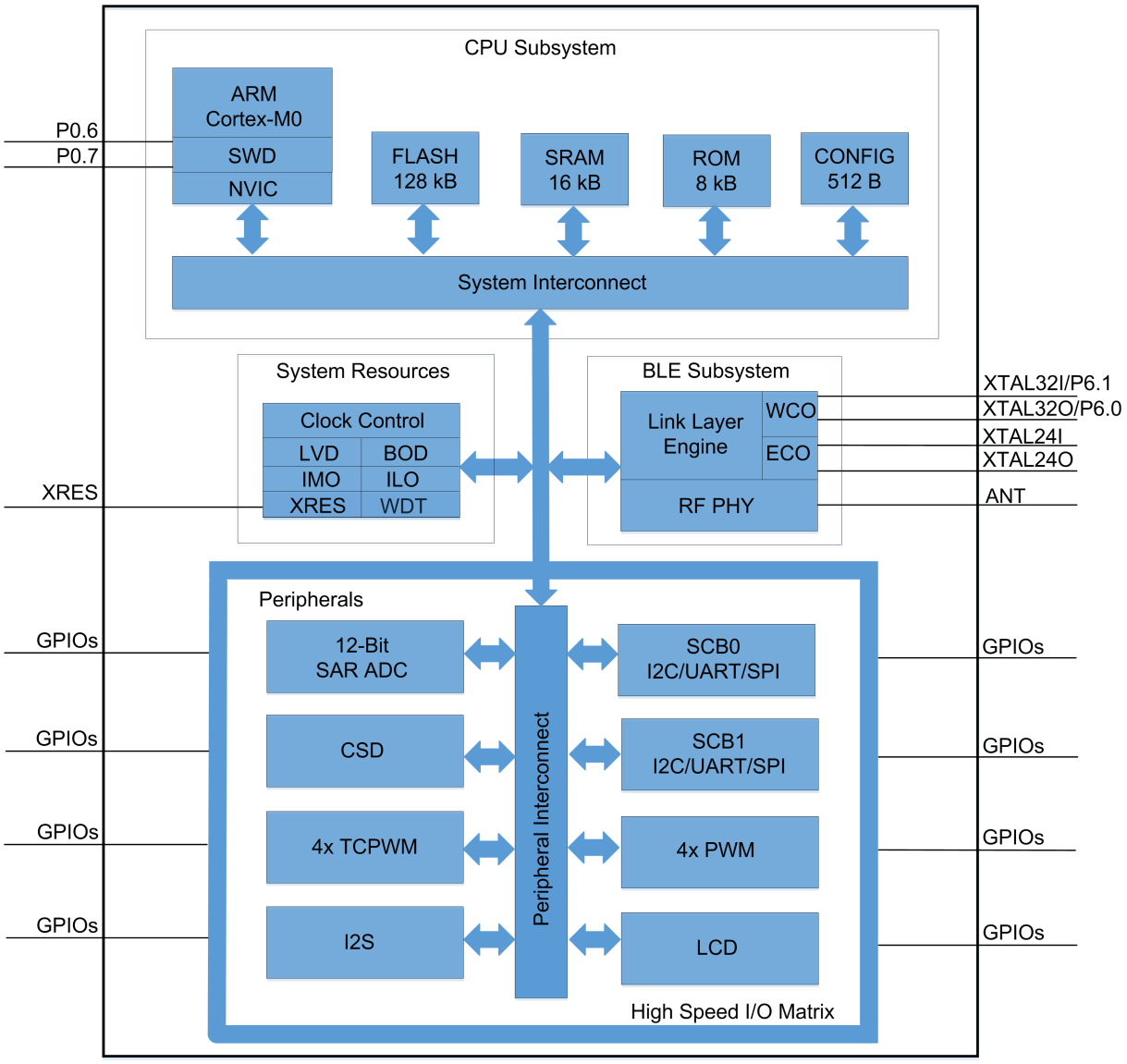


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CYBL10563-56LQXI
Package Name	56-QFN
Family	PSoC 4
Series	PRoC BLE
Max CPU speed (MHz)	48
Flash size (kB)	128
SRAM size (kB)	16
Vdd range (V)	1.9 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

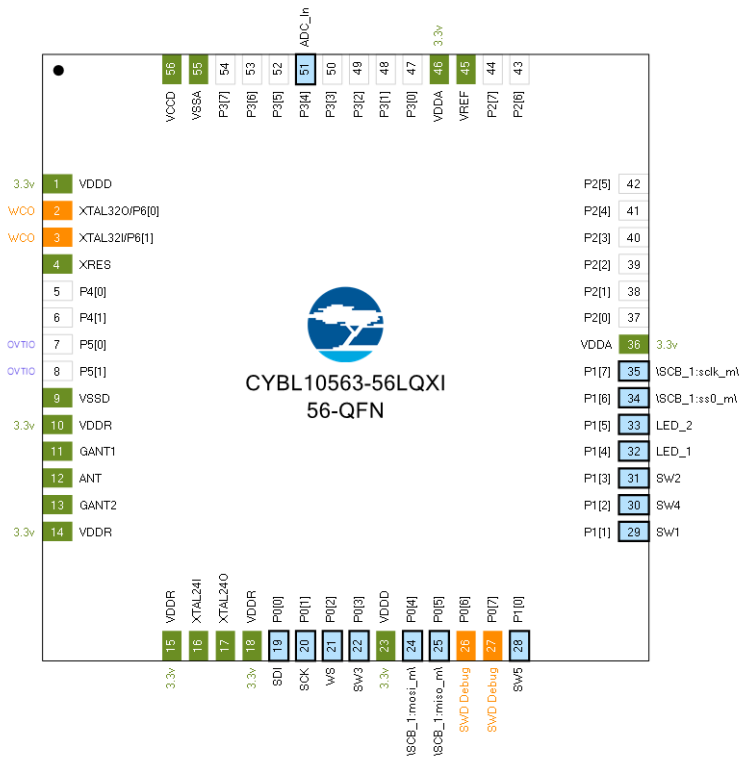
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	1	3	4	25.00 %
Interrupts	3	29	32	9.38 %
IO	19	19	38	50.00 %
Segment LCD	0	1	1	0.00 %
CapSense	0	1	1	0.00 %
Die Temp	0	1	1	0.00 %
Serial Communication (SCB)	1	1	2	50.00 %
BLE	1	0	1	100.00 %
Timer/Counter/PWM	1	3	4	25.00 %
Pre-configured Blocks	1	3	4	25.00 %
SAR ADC	1	0	1	100.00 %
DAC				
7-bit IDAC	0	1	1	0.00 %
8-bit IDAC	0	1	1	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode
1	VDDD	VDDD	Power	
2	XTAL32O/P6[0]	XTAL 32kHz:Xo	Reserved	
3	XTAL32I/P6[1]	XTAL 32kHz:Xi	Reserved	
4	XRES	XRES	Dedicated	
5	P4[0]	GPIO [unused]		
6	P4[1]	GPIO [unused]		
7	P5[0]	OVT IO [unused]		
8	P5[1]	OVT IO [unused]		
9	VSSD	VSSD	Power	
10	VDDR	VDDR	Power	
11	GANT1	GANT1	Dedicated	
12	ANT	ANT	Dedicated	
13	GANT2	GANT2	Dedicated	
14	VDDR	VDDR	Power	
15	VDDR	VDDR	Power	
16	XTAL24I	XTAL24I	Dedicated	
17	XTAL24O	XTAL24O	Dedicated	
18	VDDR	VDDR	Power	
19	P0[0]	SDI	Dgtl In	HiZ digital
20	P0[1]	SCK	Dgtl Out	Strong drive
21	P0[2]	WS	Dgtl Out	Strong drive
22	P0[3]	SW3	Software In/Out	Res pull up
23	VDDD	VDDD	Power	
24	P0[4]	\SCB_1:mosi_m\	Dgtl Out	Strong drive
25	P0[5]	\SCB_1:miso_m\	Dgtl In	HiZ digital
26	P0[6]	Debug:SWD_IO	Reserved	
27	P0[7]	Debug:SWD_CK	Reserved	
28	P1[0]	SW5	Software In/Out	Res pull up
29	P1[1]	SW1	Software In/Out	Res pull up
30	P1[2]	SW4	Software In/Out	Res pull up
31	P1[3]	SW2	Software In/Out	Res pull up
32	P1[4]	LED_1	Software In/Out	OD, DL
33	P1[5]	LED_2	Software In/Out	OD, DL
34	P1[6]	\SCB_1:ss0_m\	Dgtl Out	Strong drive
35	P1[7]	\SCB_1:sclk_m\	Dgtl Out	Strong drive
36	VDDA	VDDA	Power	
37	P2[0]	GPIO [unused]		
38	P2[1]	GPIO [unused]		
39	P2[2]	GPIO [unused]		

Pin	Port	Name	Type	Drive Mode
40	P2[3]	GPIO [unused]		
41	P2[4]	GPIO [unused]		
42	P2[5]	GPIO [unused]		
43	P2[6]	GPIO [unused]		
44	P2[7]	GPIO [unused]		
45	VREF	VREF	Dedicated	
46	VDDA	VDDA	Power	
47	P3[0]	GPIO [unused]		
48	P3[1]	GPIO [unused]		
49	P3[2]	GPIO [unused]		
50	P3[3]	GPIO [unused]		
51	P3[4]	ADC_In	Analog	HiZ analog
52	P3[5]	GPIO [unused]		
53	P3[6]	GPIO [unused]		
54	P3[7]	GPIO [unused]		
55	VSSA	VSSA	Power	
56	VCCD	VCCD	Power	

Abbreviations used in Table 3 have the following meanings:

- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output
- Res pull up = Resistive pull up
- OD, DL = Open drain, drives low
- HiZ analog = High impedance analog

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
P0[0]	19	SDI	Dgtl In	HiZ digital
P0[1]	20	SCK	Dgtl Out	Strong drive
P0[2]	21	WS	Dgtl Out	Strong drive
P0[3]	22	SW3	Software In/Out	Res pull up
P0[4]	24	\SCB_1:mosi_m\	Dgtl Out	Strong drive
P0[5]	25	\SCB_1:miso_m\	Dgtl In	HiZ digital
P0[6]	26	Debug:SWD_IO	Reserved	
P0[7]	27	Debug:SWD_CK	Reserved	
P1[0]	28	SW5	Software In/Out	Res pull up
P1[1]	29	SW1	Software In/Out	Res pull up
P1[2]	30	SW4	Software In/Out	Res pull up
P1[3]	31	SW2	Software In/Out	Res pull up
P1[4]	32	LED_1	Software In/Out	OD, DL
P1[5]	33	LED_2	Software In/Out	OD, DL
P1[6]	34	\SCB_1:ss0_m\	Dgtl Out	Strong drive
P1[7]	35	\SCB_1:sclk_m\	Dgtl Out	Strong drive
P2[0]	37	GPIO [unused]		
P2[1]	38	GPIO [unused]		
P2[2]	39	GPIO [unused]		
P2[3]	40	GPIO [unused]		
P2[4]	41	GPIO [unused]		
P2[5]	42	GPIO [unused]		
P2[6]	43	GPIO [unused]		
P2[7]	44	GPIO [unused]		
P3[0]	47	GPIO [unused]		
P3[1]	48	GPIO [unused]		
P3[2]	49	GPIO [unused]		
P3[3]	50	GPIO [unused]		
P3[4]	51	ADC_In	Analog	HiZ analog
P3[5]	52	GPIO [unused]		
P3[6]	53	GPIO [unused]		
P3[7]	54	GPIO [unused]		
P4[0]	5	GPIO [unused]		
P4[1]	6	GPIO [unused]		
P5[0]	7	OVT IO [unused]		
P5[1]	8	OVT IO [unused]		
XTAL32I/P6[1]	3	XTAL 32kHz:Xi	Reserved	
XTAL32O/P6[0]	2	XTAL 32kHz:Xo	Reserved	

Abbreviations used in Table 4 have the following meanings:

- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output
- Res pull up = Resistive pull up
- OD, DL = Open drain, drives low
- HiZ analog = High impedance analog

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
\SCB_1:miso_m\	P0[5]	Dgtl In
\SCB_1:mosi_m\	P0[4]	Dgtl Out
\SCB_1:sclk_m\	P1[7]	Dgtl Out
\SCB_1:ss0_m\	P1[6]	Dgtl Out
ADC_In	P3[4]	Analog
Debug:SWD_CK	P0[7]	Reserved
Debug:SWD_IO	P0[6]	Reserved
GPIO [unused]	P2[7]	
GPIO [unused]	P2[1]	
GPIO [unused]	P2[6]	
GPIO [unused]	P2[4]	
GPIO [unused]	P2[5]	
GPIO [unused]	P2[2]	
GPIO [unused]	P2[3]	
GPIO [unused]	P3[7]	
GPIO [unused]	P3[5]	
GPIO [unused]	P3[6]	
GPIO [unused]	P4[0]	
GPIO [unused]	P4[1]	
GPIO [unused]	P2[0]	
GPIO [unused]	P3[0]	
GPIO [unused]	P3[1]	
GPIO [unused]	P3[3]	
GPIO [unused]	P3[2]	
LED_1	P1[4]	Software In/Out
LED_2	P1[5]	Software In/Out
OVT IO [unused]	P5[1]	
OVT IO [unused]	P5[0]	
SCK	P0[1]	Dgtl Out
SDI	P0[0]	Dgtl In
SW1	P1[1]	Software In/Out
SW2	P1[3]	Software In/Out
SW3	P0[3]	Software In/Out
SW4	P1[2]	Software In/Out
SW5	P1[0]	Software In/Out
WS	P0[2]	Dgtl Out
XTAL 32kHz:Xi	XTAL32I/P6[1]	Reserved
XTAL 32kHz:Xo	XTAL32O/P6[0]	Reserved

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Disallowed
Heap Size (bytes)	0x80
Stack Size (bytes)	0x0800
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Chip Protection	Open

3.3 System Operating Conditions

Table 8. System Operating Conditions

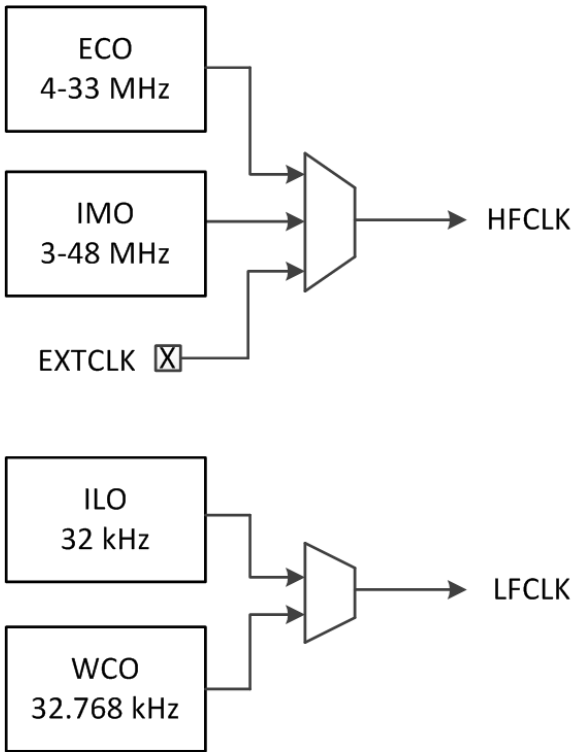
Name	Value
VDDA (V)	3.3
VDDD (V)	3.3
VDDR (V)	3.3
Variable VDDA	True

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources:
  - 3 to 48 MHz Internal Main Oscillator (IMO) ±2% at 3 MHz
  - 4 to 33 MHz External Crystal Oscillator (ECO)
  - 32 kHz Internal Low Speed Oscillator (ILO) output
  - 32.768 kHz Watch Crystal Oscillator (ILO) output
- HFCLK can be generated using an external signal from EXTCLK pin
- Twelve clock dividers, each with 16-bit divide capability:
  - Eight can be used for fixed-function blocks
  - Four can be used for the UDBs

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
PLL1_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
SysClk	NONE	HFClk	? MHz	48 MHz	±2	True	True
PLL0_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
Direct_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
HFClk	NONE	Direct_Sel	48 MHz	48 MHz	±2	True	True
IMO	NONE		48 MHz	48 MHz	±2	True	True
ECO	NONE		24 MHz	24 MHz	±0	True	True
LFClk	NONE	WCO	? MHz	32.768 kHz	±0.015	True	True
WCO	NONE		32.768 kHz	32.768 kHz	±0.015	True	True
ILO	NONE		32 kHz	32 kHz	±60	True	True
RTC_Sel	NONE	None	? MHz	? MHz	±0	True	True
DigSig2	NONE		? MHz	? MHz	±0	False	False
DigSig4	NONE		? MHz	? MHz	±0	False	False
DigSig3	NONE		? MHz	? MHz	±0	False	False
Timer2 (WDT2)	NONE	LFClk	? MHz	? MHz	±0	False	False
DigSig1	NONE		? MHz	? MHz	±0	False	False
ExtClk	NONE		24 MHz	? MHz	±0	False	False
Timer1 (WDT1)	NONE	LFClk	? MHz	? MHz	±0	False	False
Timer0 (WDT0)	NONE	LFClk	? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

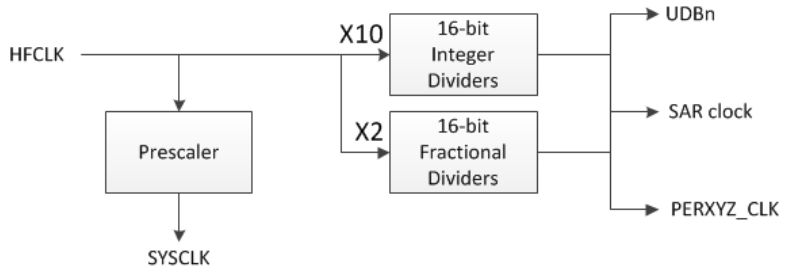


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
SCB_1_SCBCLK	FIXED_-FUNCT-ION	HFClk	16 MHz	16 MHz	±2	True	True
ADC_SAR_-Seq_1_intClock	FIXED_-FUNCT-ION	HFClk	4.28 MHz	4.364 MHz	±2	True	True
Clock_4	DIGITAL	HFClk	512 kHz	510.638 kHz	±2	True	True
BLE_1_LFCLK	NONE	LFClk	32.768 kHz	32.768 kHz	±0.015	True	True
Clock_1	FIXED_-FUNCT-ION	HFClk	32 kHz	32 kHz	±2	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 4 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CySysClkImo API routines
  - CySysClkIlo API routines
  - CySysClkEco API routines
  - CySysClkWco API routines
  - CySysClkWrite API routines

5 Interrupts

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
BLE_1_bless_isr	12	12	3
ADC_SAR_Seq_1_IRQ	15	15	3
isr_1	17	17	3

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 4 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

6 Flash Memory

PSoC 4 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x1FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 128 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- W - Full Protection

For more information on Flash memory and protection, please refer to:

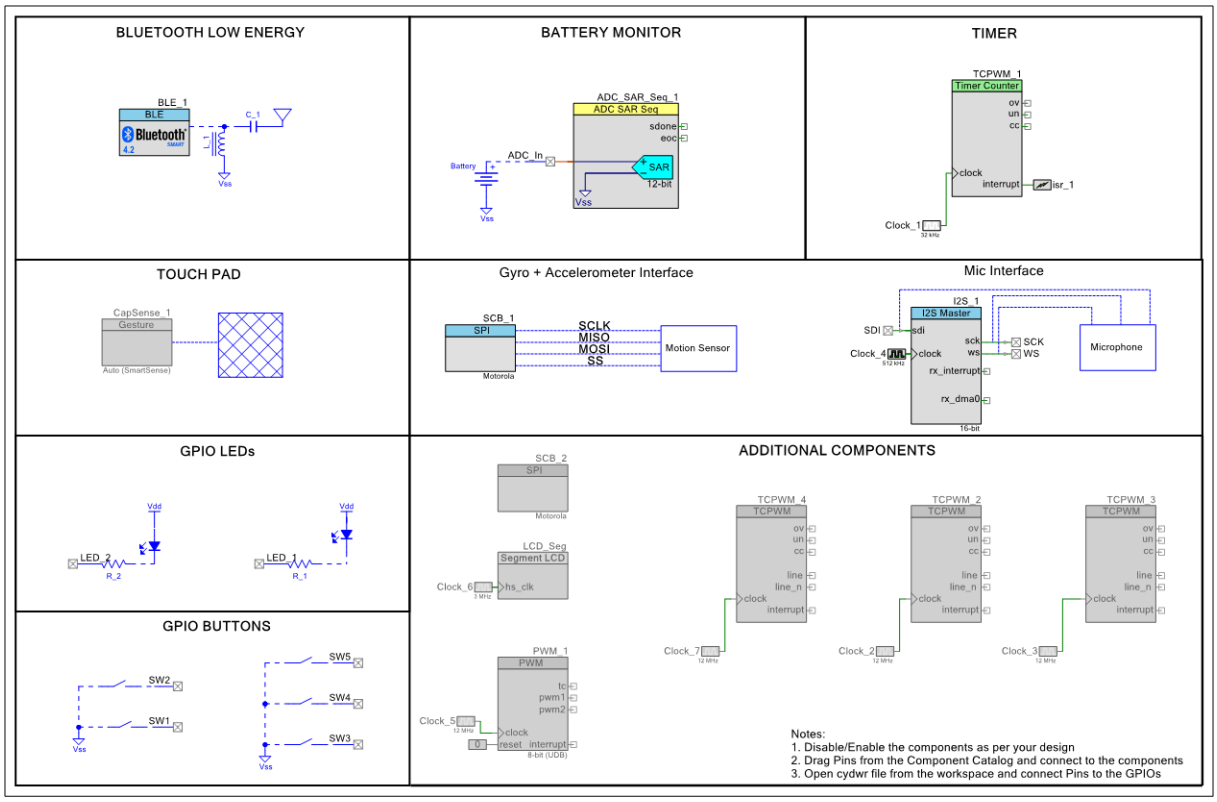
- Flash Protection chapter in the PSoC 4 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CySysFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: PRoC BLE

Figure 5. Schematic Sheet: PRoC BLE



This schematic sheet contains the following component instances:

- Instance ADC_SAR_Seq_1 (type: ADC_SAR_SEQ_P4_v2_50)
- Instance BLE_1 (type: BLE_v3_50)
- Instance I2S_1 (type: I2S_v2_70)
- Instance SCB_1 (type: SCB_P4_v4_0)
- Instance TCPWM_1 (type: TCPWM_P4_v2_10)

8 Components

8.1 Component type: ADC_SAR_SEQ_P4 [v2.50]

8.1.1 Instance ADC_SAR_Seq_1

Description: PSoC 4 Sequencing Successive Approximation ADC
Instance type: ADC_SAR_SEQ_P4 [v2.50]
Datasheet: online component datasheet for ADC_SAR_SEQ_P4

Table 13. Component Parameters for ADC_SAR_Seq_1

Parameter Name	Value	Description
AdcAClock	200	Acquisition time in clock cycles for configuration A.
AdcAdjust	ScanRate	Timing parameter adjustable by the user.
AdcAlternateResolution	8	This parameter sets the alternate ADC resolution to either 8 or 10 bits.
AdcAvgMode	Fixed Resolution	This parameter sets how the averaging mode operates.
AdcAvgSamplesNum	2	This parameter sets the averaging rate for any channel that has its averaging option enabled.
AdcBClock	2	Acquisition time in clock cycles for configuration B.
AdcCClock	2	Acquisition time in clock cycles for configuration C.
AdcChannelsEnConf	1	This bitmask is intended to enable the channels for scanning during runtime.
AdcChannelsModeConf	0	Mode configuration for the channels (0 - Single, 1 - Differential)
AdcClock	Internal	Clock source type.
AdcClockFrequency	4280000	Specifies the internal clock frequency in Hz.
AdcCompareMode	Result < Low_Limit	This parameter sets the condition in which the limit condition will occur.
AdcDataFormatJustification	Right	This parameter sets whether the output data is left or right justified for a 16-bit word. For signed values, the result will be sign extended when configured in right justification mode.
AdcDClock	2	Acquisition time in clock cycles for configuration D.
AdcDifferentialResultFormat	Unsigned	This parameter sets the whether the result from a differential measurement is Signed or Unsigned.
AdcHighLimit	4095	This parameter sets the high limit for a limit compare.

Parameter Name	Value	Description
AdcInjChannelEnabled	false	Determines whether the symbol will display the injection channel.
AdcInputBufGain	Disable	Sets the input buffer gain or disables it.
AdcLowLimit	0	This parameter sets the low limit for a limit compare.
AdcMaxResolution	12	Sets the maximum resolution of the ADC in bits.
AdcSampleMode	FreeRunning	Sampling mode.
AdcSarMuxChannelConfig	0	Channels mode configuration for the multiplexer (0 - Single, 1 - Differential)
AdcSequencedChannels	1	Number of input signals that will be scanned. This excludes the injection channel.
AdcSingleEndedNegativeInput	Vss	Negative input source for single ended operation.
AdcSingleResultFormat	Signed	This parameter sets whether the result from a single ended measurement is Signed or Unsigned.
AdcSymbolHasSingleEn-dedInputChannel	false	Determines whether the configuration contains an external negative input.
AdcVrefSelect	VDDA	The reference voltage that is used for the SAR ADC.
AdcVrefVoltage_mV	1024	The reference voltage value.
rm_int	false	Removes the internal interrupt
User Comments		Instance-specific comments.

8.2 Component type: BLE [v3.50]

8.2.1 Instance BLE_1

Description: Bluetooth Low Energy (BLE)
Instance type: BLE [v3.50]
Datasheet: online component datasheet for BLE

Table 14. Component Parameters for BLE_1

Parameter Name	Value	Description
AutopopulateWhitelist	true	Provides an option to link the whitelist to the bonded device list.
EnableExternalPAcontrol	false	Enables external power amplifier control signal with align with internal PA on time. High active.
EnableExternalPrepWriteBuff	false	Enables application to provide dynamically allocated buffer for prepare write request. The buffer should be allocated and provided after CYBLE_EVT_-MEMORY_REQUEST event from stack.
EnableL2capLogicalChannels	true	Enables L2CAP logical channels support.

Parameter Name	Value	Description
EnableLinkLayerPrivacy	true	Enables LL Privacy 1.2 feature of Bluetooth 4.2.
HalBaudRate	115200	UART baud rate
HalCtsEnable	true	In the HCI mode, the parameter enables the cts output in the UART.
HalCtsPolarity	Active Low	In the HCI mode, the parameter specifies the active polarity of the output cts signal of the UART.
HalRtsEnable	true	In the HCI mode, the parameter enables the rts output in the UART.
HalRtsPolarity	Active Low	In the HCI mode, the parameter specifies the active polarity of the output rts signal of the UART.
HalRtsTriggerLevel	4	In the HCI mode, the parameter specifies the number of entries in the RX FIFO to activate the rts output signal of the UART.
HciMode	UART	Defines the HCI interface.
ImportFilePath		The path to the file shared by another BLE component instance.
KeypressNotifications	false	Provides an option for a keyboard-only device during the LE secure pairing process to send key press notifications when the user enters or deletes a key.
L2capMpsSize	23	The maximum size of payload data that the L2CAP layer is capable of accepting.
L2capMtuSize	23	The maximum SDU size of an L2CAP packet.
L2capNumChannels	1	The number of LE L2CAP connection oriented logical channels required by the application.
L2capNumPsm	1	The number of PSMs required by the application.
LLMaxRxPayloadSize	27	The maximum link layer receive payload size to be used in the design.
LLMaxTxPayloadSize	27	The maximum link layer transmit payload size to be used in the design.
MaxAttrNoOfBuffer	1	Number of buffers can be increased from 1 to 10 to achieve better throughput if attribute mtu > 32.
MaxBondedDevices	4	The maximum number of bonded devices to be supported by this device.

Parameter Name	Value	Description
MaxResolvableDevices	8	The maximum number of peer devices whose addresses should be resolved by this device.
MaxWhitelistSize	8	The maximum number of devices that can be added to the whitelist.
Mode	Profile	Defines the component operating mode.
SharingMode	None	Defines if some parts of code are shared between two BLE components.
StackMode	Release	Determines the internal stack mode. Is used to switch the operation for debugging.
StrictPairing	false	Provides an option to use only the selected security features and doesn't fallback to an unsecure connection if the peer device doesn't support the selected security features.
UseDeepSleep	true	Indicates whether deep sleep mode is used.
User Comments		Instance-specific comments.

8.3 Component type: I2S [v2.70]

8.3.1 Instance I2S_1

Description: I2S is a common interface standard for audio data
Instance type: I2S [v2.70]
Datasheet: online component datasheet for I2S

Table 15. Component Parameters for I2S_1

Parameter Name	Value	Description
ClockSyncMode	true	Specifies whether the input clock is synchronous or asynchronous with respect to the system clock.
DataBits	16	Determines the number of data bits configured for each channel.
Direction	Rx Only	Determines in which directions the component operates.
EnableClipDetect	false	Enables clip detection on the input audio data.
EnableRxByteSwap	false	Determines if the Rx endianness conversion will be performed.
EnableTxByteSwap	false	Determines if the Tx endianness conversion will be performed.
InterruptSource	0	Selects the source of the I2S interrupts.
NegThresholds	-1	Determines the negative thresholds of clip detection.

Parameter Name	Value	Description
NumRxChannels	Stereo	Determines whether the Rx data is for mono, stereo or multi-stereo channels.
NumTxChannels	Stereo	Determines whether the Tx data is for mono, stereo or multi-stereo channels.
PosThresholds	0u	Determines the positive thresholds of clip detection.
RxDataInterleaving	Interleaved	Determines whether the data for the Rx direction is interleaved.
RxDMA_present	Enabled	Sets whether DMA request signals are present for the Rx direction.
StaticBitResolution	true	Determines whether a channel data bits resolution is compile time or can be changed through API calls.
TxDataInterleaving	Interleaved	Determines whether the data for the Tx direction is interleaved.
TxDMA_present	Enabled	Sets whether DMA request signals are present for the Tx direction.
User Comments		Instance-specific comments.
WordSelect	64	Determines the period of a complete sample of both left and right channels.

8.4 Component type: SCB_P4 [v4.0]

8.4.1 Instance SCB_1

Description: Serial Communication Block (SCB)
Instance type: SCB_P4 [v4.0]
Datasheet: online component datasheet for SCB_P4

Table 16. Component Parameters for SCB_1

Parameter Name	Value	Description
EzI2cByteModeEnable	false	When the SCB mode is EZI2C, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
EzI2cClockFromTerm	false	When the SCB mode is EZI2C, this parameter provides a clock terminal to connect a clock outside the component.

Parameter Name	Value	Description
EzI2cClockStretching	true	When the SCB mode is EZI2C, this parameter specifies whether the SCL is stretched while in EZI2C operation.
EzI2cDataRate	100	When the SCB mode is EZI2C, this parameter defines EZI2C Data rate in kbps. The standard data rates are: 100, 400 and 1000 kbps.
EzI2cNumberOfAddresses	1	When the SCB mode is EZI2C, this parameter defines the number of I2C slave addresses that device respond to.
EzI2cPrimarySlaveAddress	8	When the SCB mode is EZI2C, this parameter specifies EZI2C primary 7-bits slave address (MSB ignored).
EzI2cSecondarySlaveAddress	9	When the SCB mode is EZI2C, this parameter specifies EZI2C secondary 7-bits slave address (MSB ignored). Only applicable when EZI2C clock stretching option is set.
EzI2cSubAddressSize	8	When the SCB mode is EZI2C, this parameter specifies the maximum size of the slave buffer that is exposed to the master: 8bits – maximum buffer size is 256 bytes, 16 bits – maximum buffer size is 65535 bytes.
EzI2cWakeEnable	false	When the SCB mode is EZI2C, this parameter enables wakeup from Deep Sleep on I2C address match event.
I2C Bus Voltage	3.3	When the SCB mode is I2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus. Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2C Bus Voltage	3.3	When the SCB mode is EZI2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus. Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.

Parameter Name	Value	Description
I2cAcceptAddress	false	When the SCB mode is I2C, this parameter specifies whether to accept the match slave address in RX FIFO or not. All slave matched addresses are ACKed. The user has to register the callback function to handle accepted addresses. This feature has to be used when more than one address support is required.
I2cAcceptGeneralCall	false	When the SCB mode is I2C, this parameter specifies whether to accept the general call address. The general call address is ACKed when accepted and NAKed otherwise. The user has to register the callback function to handle the general call address.
I2cByteModeEnable	false	When the SCB mode is I2C, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cClockFromTerm	false	When the SCB mode is I2C, this parameter provides a clock terminal to connect a clock outside the component.
I2cDataRate	100	When the SCB mode is I2C, this parameter specifies the data rate in kbps. The standard data rates are: 100, 400 and 1000 kbps.
I2cExternIntrHandler	false	When the SCB mode is I2C, this parameter specifies whether the I2C interrupt handler is configured in SCB_I2CInit(). This parameter is intended to be used by the PM/SM bus component. The modification parameter default value causes I2C mode failures.
I2cManualOversampleControl	true	When the SCB mode is I2C, this parameter specifies the method of calculating the oversampling as manual or automatic.

Parameter Name	Value	Description
I2cMode	Slave	When the SCB mode is I2C, this parameter defines the I2C operation mode as: Slave, Master, Multi-Master or Multi-Master-Slave.
I2cOvsFactor	16	When the SCB mode is I2C, this parameter defines the oversampling factor of SCBCLK.
I2cOvsFactorHigh	8	When the SCB mode is I2C, this parameter defines the high oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cOvsFactorLow	8	When the SCB mode is I2C, this parameter defines the low oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cSlaveAddress	8	When the SCB mode is I2C, this parameter specifies the I2C 7-bits slave address (MSB ignored).
I2cSlaveAddressMask	254	When the SCB mode is I2C, this parameter specifies the I2C Slave address mask. Bit value 0 – excludes bit from address comparison. Bit value 1 – the bit needs to match with the corresponding bit of the I2C slave address.
I2cWakeEnable	false	When the SCB mode is I2C, this parameter enables wakeup from Deep Sleep on an I2C address match event.
ScbMisoSdaTxEnable	true	This parameter defines the availability of the spi_miso_i2c_-sda_uart_tx pin.
ScbMode	SPI	This parameter defines the mode of operation for the SCB component.
ScbMosiSclRxEnable	true	This parameter defines the availability of the spi_mosi_i2c_-scl_uart_rx pin.
ScbRxWakeIrqEnable	false	This parameter defines the availability of the spi_mosi_i2c_-scl_uart_rx_wake pin.
ScbSclkEnable	false	This parameter defines the availability of the sclk pin.
ScbSs0Enable	false	This parameter defines the availability of the ss0 pin.
ScbSs1Enable	false	This parameter defines the availability of the ss1 pin.
ScbSs2Enable	false	This parameter defines the availability of the ss2 pin.

Parameter Name	Value	Description
ScbSs3Enable	false	This parameter defines the availability of the ss3 pin.
Show EZI2C Terminals	false	When the SCB mode is EZI2C, this parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins.
Show I2C Terminals	false	When the SCB mode is I2C, this parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins.
Show SPI Terminals	false	When the SCB mode is SPI, this parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins or SmartIO component.
Show UART Terminals	false	When the SCB mode is UART, this parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins or SmartIO component.
Slew Rate	Fast	When the SCB mode is EZI2C, this parameter specifies the slew rate settings of the I2C pins. For devices supporting GPIO Over-Voltage Tolerance (GPIO_OVT) pins, I2C FM+ options should be used when I2C data rate is greater than 400 kbps. This option also requires the I2C bus voltage to be defined.Refer to the Device Datasheet to determine which pins are GPIO_OVT capable.
Slew Rate	Fast	When the SCB mode is I2C, this parameter specifies the slew rate settings of the I2C pins. For devices supporting GPIO Over-Voltage Tolerance (GPIO_OVT) pins, I2C FM+ options should be used when I2C data rate is greater than 400 kbps. This option also requires the I2C bus voltage to be defined. Refer to the Device Datasheet to determine which pins are GPIO_OVT capable.

Parameter Name	Value	Description
SpiBitRate	1000	When the SCB mode is SPI, this parameter specifies the Bit rate in kbps (up to 8000 kbps); the actual rate may differ based on available clock frequency and component settings. This parameter has no effect if the Clock from terminal parameter is enabled.
SpiBitsOrder	MSB First	When the SCB mode is SPI, this parameter defines the bit order as: MSB first or LSB first.
SpiByteModeEnable	false	When the SCB mode is SPI, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiClockFromTerm	false	When the SCB mode is SPI, this parameter provides a clock terminal to connect a clock outside the component.
SpiFreeRunningSclk	false	When the SCB mode is SPI, this parameter specifies the SCLK generation by the master as: gated or free running (continuous). Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiInterruptMode	None	When the SCB mode is SPI, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an interrupt outside the component.
SpiIntrMasterSpiDone	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_M. SPI_DONE interrupt source. SCB.INTR_M. SPI_DONE: all data are sent into TX FIFO and the TX FIFO and the shifter register are emptied. Only applicable for SPI Master mode.

Parameter Name	Value	Description
SpiIntrRxFull	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.FULL interrupt source. SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
SpiIntrRxNotEmpty	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.
SpiIntrRxOverflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
SpiIntrRxTrigger	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by SpiRxTriggerLevel.
SpiIntrRxUnderflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.UNDERFLOW interrupt source. SCB.INTR_RX.UNDERFLOW trigger condition: attempt to read from an empty RX FIFO.
SpiIntrSlaveBusError	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_SLAVE.BUS_-ERROR interrupt source. SCB.INTR_SLAVE.BUS_-ERROR trigger condition: slave select line is deselected at an unexpected time in the SPI transfer. Only applicable for SPI Slave mode.
SpiIntrTxEmpty	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.EMPTY interrupt source. SCB.INTR_TX.EMPTY trigger condition: TX FIFO is empty.

Parameter Name	Value	Description
SpiIntrTxNotFull	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.NOT_FULL interrupt source. SCB.INTR_TX.NOT_FULL trigger condition: TX FIFO is not full. There is at least one entry to put data.
SpiIntrTxOverflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.OVERFLOW interrupt source. SCB.INTR_TX.OVERFLOW trigger condition: attempt to write to a full TX FIFO.
SpiIntrTxTrigger	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.TRIGGER interrupt source. SCB.INTR_TX.TRIGGER trigger condition: remains active until TX FIFO has fewer entries than the value specified by SpiTxTriggerLevel.
SpiIntrTxUnderflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.UNDERFLOW interrupt source. SCB.INTR_TX.UNDERFLOW trigger condition: attempt to read from an empty TX FIFO.
SpiLateMisoSampleEnable	false	When the SCB mode is SPI, this parameter enables late sampling of the MISO line by the master.
SpiMedianFilterEnable	false	When the SCB mode is SPI, this parameter applies a digital 3 tap median filter to the SPI input line.
SpiMode	Master	When the SCB mode is SPI, this parameter selects SPI mode of operation as: Slave or Master.
SpiNumberOfRxDataBits	8	When the SCB mode is SPI, this parameter specifies the number of data bits inside the SPI byte/word for RX direction.
SpiNumberOfSelectLines	1	When the SCB mode is SPI, this parameter defines the number of slave select lines. The SPI Slave has only one slave select line. The SPI Master has up to 4 lines.
SpiNumberOfTxDataBits	8	When the SCB mode is SPI, this parameter define the number of data bits inside the SPI byte/word for TX direction.

Parameter Name	Value	Description
SpiOvsFactor	16	When the SCB mode is SPI, this parameter defines the oversampling factor of SCBCLK.
SpiRemoveMiso	false	When the SCB mode is SPI, this parameter removes the MISO pin.
SpiRemoveMosi	false	When the SCB mode is SPI, this parameter removes the MOSI pin.
SpiRemoveSclk	false	When the SCB mode is SPI, this parameter removes the SCLK pin.
SpiRxBufferSize	8	When the SCB mode is SPI, this parameter defines the size of the RX buffer.
SpiRxOutputEnable	false	When the SCB mode is SPI, this parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
SpiRxTriggerLevel	7	When the SCB mode is SPI, this parameter defines the number of entries in the RX FIFO to control the SCB.INTR_-RX.TRIGGER interrupt event or RX DMA trigger output.
SpiSclkMode	CPHA = 0, CPOL = 0	When the SCB mode is SPI, this parameter defines the serial clock phase (CPHA) and polarity (CPOL).
SpiSs0Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 0. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSs1Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 1. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSs2Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 2. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.

Parameter Name	Value	Description
SpiSs3Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 3. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSubMode	Motorola	When the SCB mode is SPI, this parameter defines the sub mode of the SPI as: Motorola, TI(Start Coincides), TI(Start Precedes), or National Semiconductor.
SpiTransferSeparation	Continuous	When the SCB mode is SPI, this parameter defines the type of SPI transfers separation as: continuous or separated.
SpiTxBufferSize	8	When the SCB mode is SPI, this parameter defines the size of the TX buffer.
SpiTxOutputEnable	false	When the SCB mode is SPI, this parameter enables the TX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
SpiTxTriggerLevel	0	When the SCB mode is SPI, this parameter defines the number of entries in the TX FIFO to control the SCB.INTR_-TX.TRIGGER interrupt event or TX DMA trigger output.
SpiWakeEnable	false	When the SCB mode is SPI, this parameter enables wakeup from Deep Sleep on slave select event.
UartByteModeEnable	false	When the SCB mode is UART, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartClockFromTerm	false	When the SCB mode is UART, this parameter provides a clock terminal to connect a clock outside the component.

Parameter Name	Value	Description
UartCtsEnable	false	When the SCB mode is UART, this parameter enables the cts input. Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartCtsPolarity	Active Low	When the SCB mode is UART, this parameter specifies active polarity of an input cts signal. Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartDataRate	115200	When the SCB mode is UART, this parameter specifies the Baud rate in bps (up to 1000 kbps); the actual rate may differ based on available clock frequency and component settings. This parameter has no effect if the Clock from terminal parameter is enabled.
UartDirection	TX + RX	When the SCB mode is UART, this parameter enables RX or TX direction or both simultaneously.
UartDropOnFrameErr	false	When the SCB mode is UART, this parameter defines whether the data is dropped from RX FIFO on a frame error event.
UartDropOnParityErr	false	When the SCB mode is UART, this parameter determines whether the data is dropped from RX FIFO on a parity error event.
UartInterruptMode	None	When the SCB mode is UART, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an interrupt outside component.
UartIntrRxBreakDetected	false	This parameter enables the RX break detection interrupt source to trigger the interrupt output.
UartIntrRxFrameErr	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FRAME_-ERROR interrupt source. SCB.INTR_RX.FRAME_-ERROR trigger condition: frame error in received data frame.

Parameter Name	Value	Description
UartIntrRxFull	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FULL interrupt source. SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
UartIntrRxNotEmpty	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.
UartIntrRxOverflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
UartIntrRxParityErr	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.PARITY_-ERROR interrupt source. SCB.INTR_RX.PARITY_-ERROR trigger condition: parity error in received data frame.
UartIntrRxTrigger	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by UartRxTriggerLevel.
UartIntrRxUnderflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.UNDERFLOW interrupt source. SCB.INTR_RX.UNDERFLOW trigger condition: attempt to read from an empty RX FIFO.
UartIntrTxEmpty	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.EMPTY interrupt source. SCB.INTR_TX.EMPTY trigger condition: TX FIFO is empty.
UartIntrTxNotFull	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.NOT_FULL interrupt source. SCB.INTR_TX.NOT_FULL trigger condition: TX FIFO is not full. There is at least one entry to put data.

Parameter Name	Value	Description
UartIntrTxOverflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.OVERFLOW interrupt source. SCB.INTR_TX.OVERFLOW trigger condition: attempt to write to a full TX FIFO.
UartIntrTxTrigger	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.TRIGGER interrupt source. SCB.INTR_TX.TRIGGER trigger condition: remains active until TX FIFO has fewer entries than the value specified by UartTxTriggerLevel.
UartIntrTxUartDone	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.UART_DONE interrupt source. SCB.INTR_TX.UART_DONE trigger condition: all data are sent in to TX FIFO and the transmit FIFO and the shifter register are emptied.
UartIntrTxUartLostArb	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.UART_ARB_-LOST interrupt source. SCB.INTR_TX.UART_ARB_-LOST trigger condition: UART lost arbitration, the value driven on the TX line is not the same as the value observed on the RX line. This event is useful when the transmitter and the receiver share a TX/RX line. Only applicable for UART SmartCard mode.
UartIntrTxUartNack	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.UART_NACK interrupt source. SCB.INTR_TX.UART_NACK trigger condition: UART transmitter received a negative acknowledgement. Only applicable for UART SmartCard mode.
UartIntrTxUnderflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.UNDERFLOW interrupt source. SCB.INTR_TX.UNDERFLOW trigger condition: attempt to read from an empty TX FIFO.

Parameter Name	Value	Description
UartIrdaLowPower	false	When the SCB mode is UART, this parameter enables the low power receiver option. Only applicable for UART IrDA mode.
UartIrdaPolarity	Non-Inverting	When the SCB mode is UART, this parameter inverts the incoming RX line signal. Only applicable for UART IrDA mode.
UartMedianFilterEnable	false	When the SCB mode is UART, this parameter applies a digital 3 tap median filter to the UART input line.
UartMpEnable	false	When the SCB mode is UART, this parameter enables the UART multi-processor mode. Only applicable for UART Standard mode.
UartMpRxAcceptAddress	false	When the SCB mode is UART, this parameter define whether to put the matched UART address into RX FIFO. Only applicable for UART multi-processor mode.
UartMpRxAddress	2	When the SCB mode is UART, this parameter defines the UART address. Only applicable for UART multi-processor mode.
UartMpRxAddressMask	255	When the SCB mode is UART, this parameter defines the address mask in multi-processor operation mode. Bit value 0 – excludes bit from address comparison. Bit value 1 – the bit needs to match with the corresponding bit of the UART address. Only applicable for UART multi-processor mode.
UartNumberOfDataBits	8 bits	When the SCB mode is UART, this parameter defines the number of data bits inside the UART byte/word.
UartNumberOfStopBits	1 bit	When the SCB mode is UART, this parameter defines the number of Stop bits.
UartOvsFactor	12	When the SCB mode is UART, this parameter defines the oversampling factor of SCBCLK.
UartParityType	None	When the SCB mode is UART, this parameter applies UART parity check as Odd or Even or discards the parity entirely.

Parameter Name	Value	Description
UartRtsEnable	false	When the SCB mode is UART, this parameter enables the rts output. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRtsPolarity	Active Low	When the SCB mode is UART, this parameter specifies active polarity of the output rts signal. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRtsTriggerLevel	4	When the SCB mode is UART, this parameter specifies the number of entries in the RX FIFO to activate the rts output signal. When the receiver FIFO has fewer entries than the UartRtsTriggerLevel, an rts output signal is activated. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRxBreakWidth	11	This parameter specifies the break width in bits.
UartRxBufferSize	8	When the SCB mode is UART, this parameter defines the size of the RX buffer.
UartRxOutputEnable	false	When the SCB mode is UART, this parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
UartRxTriggerLevel	7	When the SCB mode is UART, this parameter defines the number of entries in the RX FIFO to trigger control the SCB.INTR_RX.TRIGGER interrupt event or RX DMA trigger output.
UartSmCardRetryOnNack	false	When the SCB mode is UART, this parameter defines whether to send a message again when a NACK response is received. Only applicable for UART SmartCard mode.
UartSubMode	Standard	When the SCB mode is UART, this parameter defines the sub mode of UART as: Standard, SmartCard or IrDA.
UartTxBufferSize	8	When the SCB mode is UART, this parameter defines the size of the TX buffer.

Parameter Name	Value	Description
UartTxOutputEnable	false	When the SCB mode is UART, this parameter enables the TX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
UartTxTriggerLevel	0	When the SCB mode is UART, this parameter defines the number of entries in the TX FIFO to control the SCB.INTR_-TX.TRIGGER interrupt event or TX DMA trigger output.
UartWakeEnable	false	When the SCB mode is UART, this parameter enables the wakeup from Deep Sleep on start bit event. The actual wakeup source is RX GPIO. The skip start UART feature allows it to continue receiving bytes.
User Comments		Instance-specific comments.

8.5 Component type: TCPWM_P4 [v2.10]

8.5.1 Instance TCPWM_1

Description: 16-bit Timer Counter PWM (TCPWM)
Instance type: TCPWM_P4 [v2.10]
Datasheet: online component datasheet for TCPWM_P4

Table 17. Component Parameters for TCPWM_1

Parameter Name	Value	Description
PWMCompare	65535	The initial value for the comparison register when in the PWM mode
PWMCompareBuf	65535	The initial value for the second comparison register when in the PWM mode
PWMCompareSwap	Disable swap	Determines whether the PWM swap check box is enabled or disabled
PWMCountMode	Level	Determines whether the PWM counter counts at level detection or in various modes of edge detection
PWMCountPresent	false	Determines if the PWM count signal is present and controls the visibility of the count pin
PWMDeadTimeCycle	0	Sets the number of cycles of dead time insertion
PWMInterruptMask	Terminal count mask	The mask used for enabling the interrupt bit in the PWM mode
PWMKillEvent	Asynchronous	Selects whether a PWM kill event is synchronous or asynchronous to the input clock

Parameter Name	Value	Description
PWMLinenSignal	Direct Output	Selects whether the PWM line_n signal is inverted or is directly output
PWMLineSignal	Direct Output	Selects whether the PWM line signal is inverted or is directly output
PWMMode	PWM	Selects one of the three PWM modes - PWM, PWM with dead time insertion, or Pseudo random PWM
PWMPeriod	65535	The initial value for the period register when in the PWM mode
PWMPeriodBuf	65535	The initial value for the second period register when in the PWM mode
PWMPeriodSwap	Disable swap	Enables swap between the PWM period and period_buf registers
PWMPrescaler	0	Defines the prescaler used to divide the TCPWM clock to create the counter clock
PWMReloadMode	Rising edge	Determines whether the PWM reload signal is accepted at level detection or in various modes of edge detection
PWMReloadPresent	false	Determines whether the PWM reload signal is present and controls its pin visibility
PWMRunMode	Continuous	Selects between continuous and one shot run mode for the PWM
PWMSetAlign	Left align	Selects the alignment of the PWM waveform to be either left, right, center or asymmetrically aligned
PWMStartMode	Rising edge	Determines whether the PWM start signal is accepted at level detection or in various modes of edge detection
PWMStartPresent	false	Determines whether the PWM start signal is present and controls its pin visibility
PWMStopEvent	Don't stop on Kill	Selects whether to kill the PWM on a stop signal or not
PWMStopMode	Rising edge	Determines whether the PWM stop signal is accepted at level detection or in various modes of edge detection
PWMStopPresent	false	Determines whether the PWM stop signal is present and controls its pin visibility
PWMSwitchMode	Rising edge	Determines whether the PWM switch signal is accepted at level detection or in various modes of edge detection
PWMSwitchPresent	false	Determines whether the PWM switch signal is present and controls its pin visibility

Parameter Name	Value	Description
QuadEncodingModes	x1 Encoding mode	Selects one of the three quadrature decoder modes – x1, x2, or x4 encoding mode
QuadIndexMode	Rising edge	Determines whether the Quadrature Decoder index signal is accepted at level detection or in various modes of edge detection
QuadIndexPresent	false	Determines whether the Quadrature Decoder index signal is present and controls its pin visibility
QuadInterruptMask	Terminal count mask	The mask used to configure which Quadrature Decoder event causes an interrupt
QuadPhiAMode	Level	Determines whether the Quadrature Decoder PhiA signal is accepted at level detection or in various modes of edge detection
QuadPhiBMode	Level	Determines whether the Quadrature Decoder PhiB signal is accepted at level detection or in various modes of edge detection
QuadStopMode	Rising edge	Determines whether the Quadrature Decoder stop signal is accepted at level detection or in various modes of edge detection
QuadStopPresent	false	Determines whether the Quadrature Decoder stop signal is present and controls its pin visibility
TCCaptureMode	Rising edge	Determines whether the Timer/Counter capture signal is accepted at level detection or in various modes of edge detection
TCCapturePresent	false	Determines whether the Timer/Counter capture signal is present and controls its pin visibility
TCCompare	31	The initial value for the comparison register when in the Timer/Counter mode
TCCompareBuf	65535	The initial value for the second comparison register when in the Timer/Counter mode
TCCompareSwap	Disable swap	Determines whether the Timer/Counter swap check box is enabled or disabled
TCCompCapMode	Capture Mode	Selects whether the Timer/Counter capture or the compare mode is enabled
TCCountingModes	Counts up	Selects the count direction of the counter

Parameter Name	Value	Description
TCCountMode	Level	Determines whether the Timer/Counter count signal is accepted at a level detect or at various modes of edge detection
TCCountPresent	false	Determines whether the Timer/Counter count signal is present and controls its pin visibility
TCInterruptMask	Terminal count mask	The mask used to determine which Timer/Counter event causes an interrupt
TCPeriod	32	The initial value for the Timer/Counter period register
TCPrescaler	0	Selects the prescaler value to apply to the Timer/Counter clock
TCPWMCapturePresent	false	Determines whether the Unconfigured capture signal is present and controls its pin visibility
TCPWMConfig	Timer Counter	Selects the TCPWM mode - Unconfigured, Timer/Counter, PWM, or Quadrature Decoder
TCPWMCountPresent	false	Determines whether the Unconfigured count signal is present and controls its pin visibility
TCPWMReloadPresent	false	Determines whether the Unconfigured reload signal is present and controls its pin visibility
TCPWMStartPresent	false	Determines whether the Unconfigured start signal is present and controls its pin visibility
TCPWMStopPresent	false	Determines whether the Unconfigured stop signal is present and controls its pin visibility
TCReloadMode	Rising edge	Determines whether the Timer/Counter reload signal is accepted at level detection or in various modes of edge detection
TCReloadPresent	false	Determines whether the Timer/Counter reload signal is present and controls its pin visibility
TCRunMode	Continuous	Selects whether the counter runs continuously or one shot
TCStartMode	Rising edge	Determines whether the start signal is accepted at level detection or in various modes of edge detection

Parameter Name	Value	Description
TCStartPresent	false	Determines whether the Timer/Counter start signal is present and controls its pin visibility
TCStopMode	Rising edge	Determines whether the Timer/Counter stop signal is accepted at level detection or in various modes of edge detection
TCStopPresent	false	Determines whether the Timer/Counter stop signal is present and controls its pin visibility
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 4 register map is covered in the PSoC 4 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 4 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 4 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines