Carleton University

ELEC 4700 A

Assignment- 4: Circuit Modelling

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PART 1

The primary part of the assignment involves using the given circuit to determine the G and C matrices. Moreover, DC and AC simulations were performed on the circuit.

The following differential equations were obtained for the circuit using KCL:

$$V_1 = V_{in} \qquad (1)$$

$$G_1(V_2 - V_1) + C_1\frac{d(V_2 - V_1)}{dt} + I_l = 0 \qquad (2)$$

$$G_3V_3 - I_l = 0 \qquad (3)$$

$$G_3V_3 - I_3 = 0 \qquad (4)$$

$$G_4(V_0 - V_4) + G_0V_0 = 0 \qquad (5)$$

$$V_2 - V_3 - L\frac{dI_l}{dt} = 0 \qquad (6)$$

$$V_4 - aI_3 = 0 \qquad (7)$$

The matrix G for the network can be seen below:

```
G =

    1.0000         0         0         0         0         0         0
   -1.0000    1.5000         0         0         0    1.0000         0
         0         0    0.1000         0         0   -1.0000         0
         0         0    0.1000         0         0         0   -1.0000
         0         0         0  -10.0000   10.0010         0         0
         0    1.0000   -1.0000         0         0         0         0
         0         0         0    1.0000         0         0 -100.0000
```

Figure 1. G Matrix

The matrix C for the network can be seen below:

```
Cm =

         0         0         0         0         0         0         0
   -0.2500    0.2500         0         0         0         0         0
         0         0         0         0         0         0         0
         0         0         0         0         0         0         0
         0         0         0         0         0         0         0
         0         0         0         0         0   -0.2000         0
         0         0         0         0         0         0         0
```

Figure 2. C Matrix

The vector F for the network can be seen below:

```
F =

    10
     0
     0
     0
     0
     0
     0
```

Figure 3. F Vector

These matrices and vector were used to describe the network using:

$$C\frac{dV}{dt} + GV = F \qquad (8)$$

$$(G + j\omega C)V = F(\omega) \qquad (9)$$

For the DC case, the matrix C can be ignored, thus the network can simply be solved for GV = F. The input voltage was swept from -10V to 10V and the V_0 and V_3 voltages were plotted as a function of the input voltage as can be seen below:

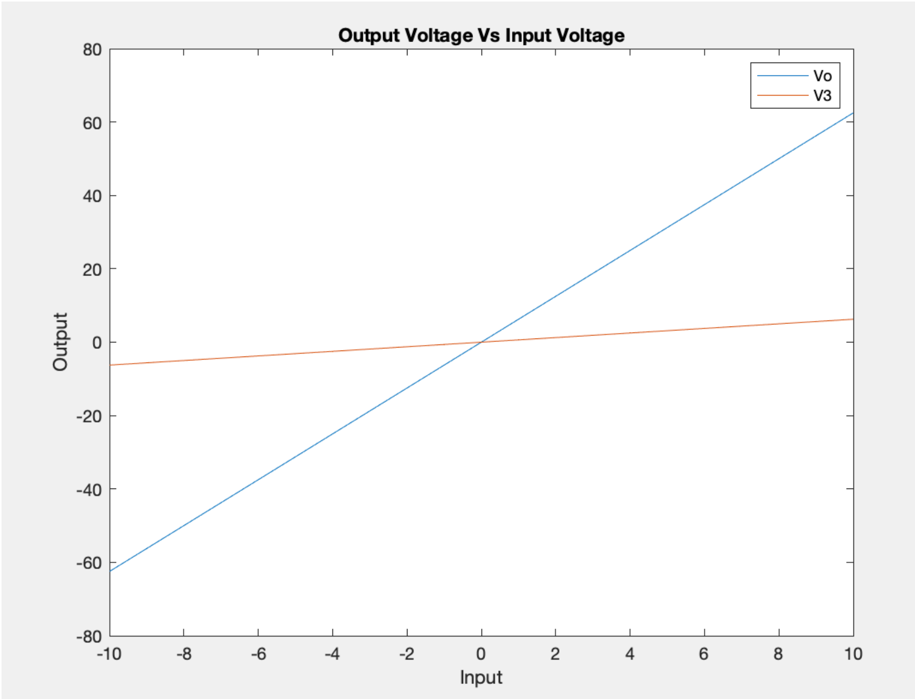

Figure 4. Plot of DC Sweep of Input Voltage for Vo and V3

For the AC case, the output voltage along with the gain was plotted as a function of the frequency as can be seen below:

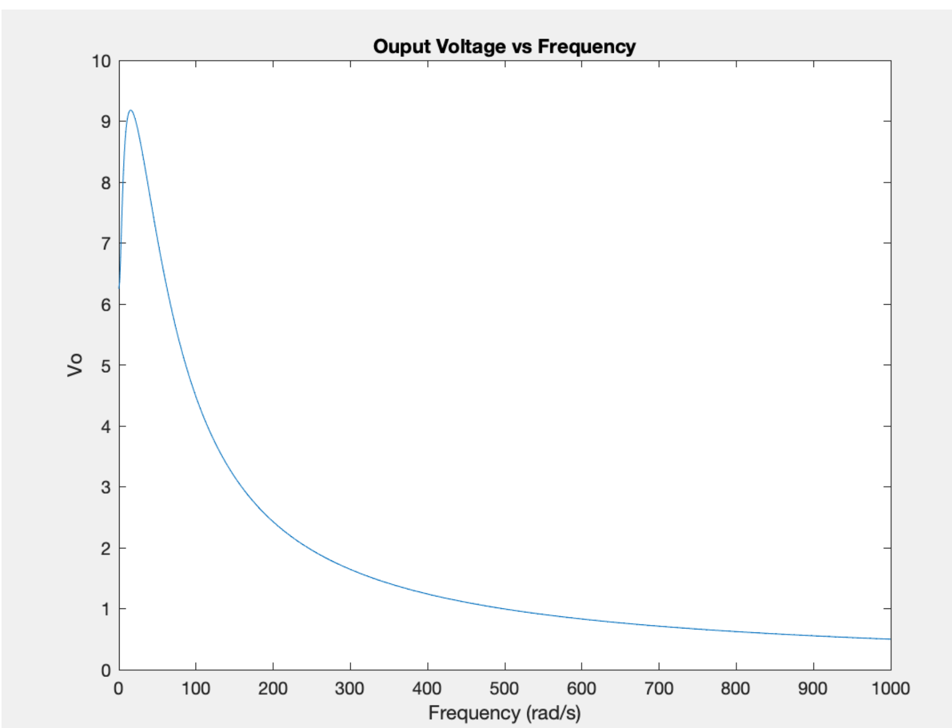

Figure 5. Plot of Output Voltage vs Frequency

For the AC case, the gain as a function of random perturbations on C was determined using a normal distribution and plotted. Moreover, the histogram of the gain was performed as can be seen below:

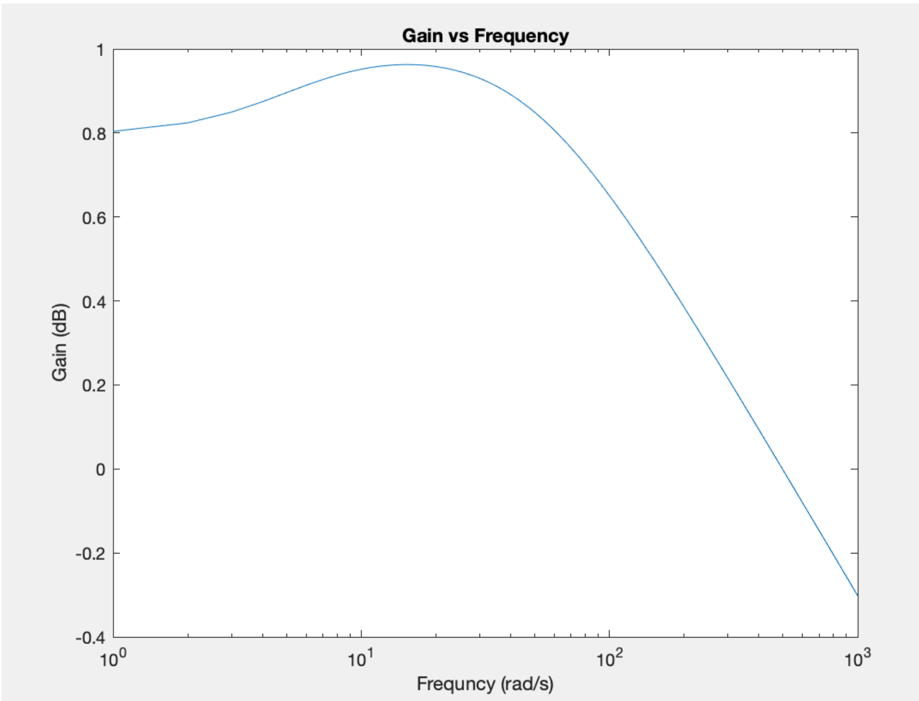

Figure 6. Plot of Gain svs Frequency

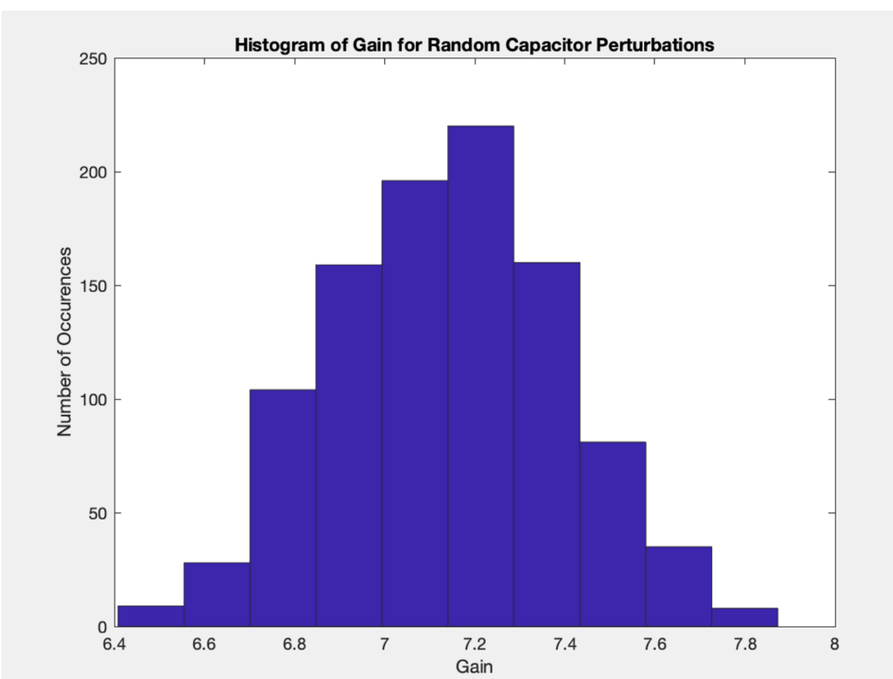

Figure 7. Histogram of Gain for Random Capacitor Perturbations

PART 2

The secondary part of the assignment involves performing a transient simulation of the given circuit. This circuit was simulated for a step input that transitions from 0 to 1 at 0.03s, a sinusoidal input with frequency of 33Hz, and a gaussian pulse with a magnitude of 1, std dev. of 0.03s and a delay of 0.06s. This can be seen below:

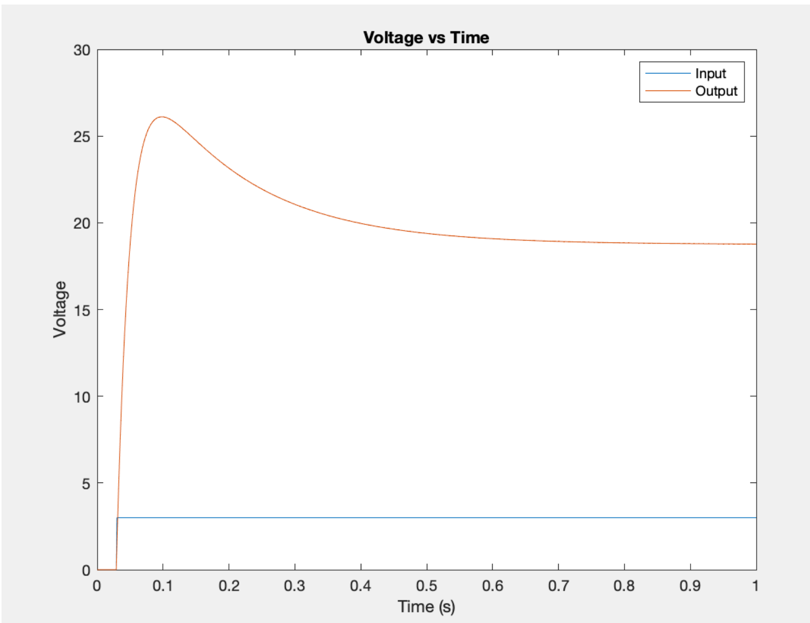

Figure 8. Plot of Input and Output Voltage for Step Input

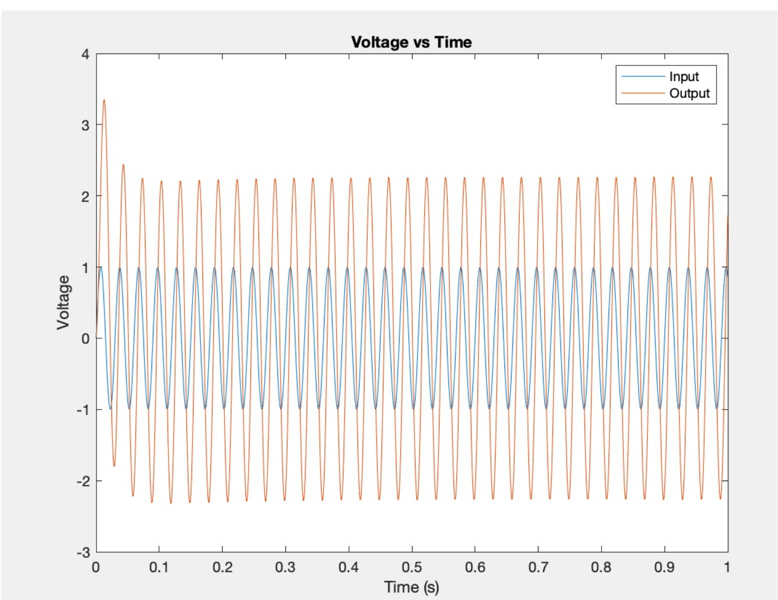

Figure 9. Plot of Input and Output Voltage for Sinusoidal Input

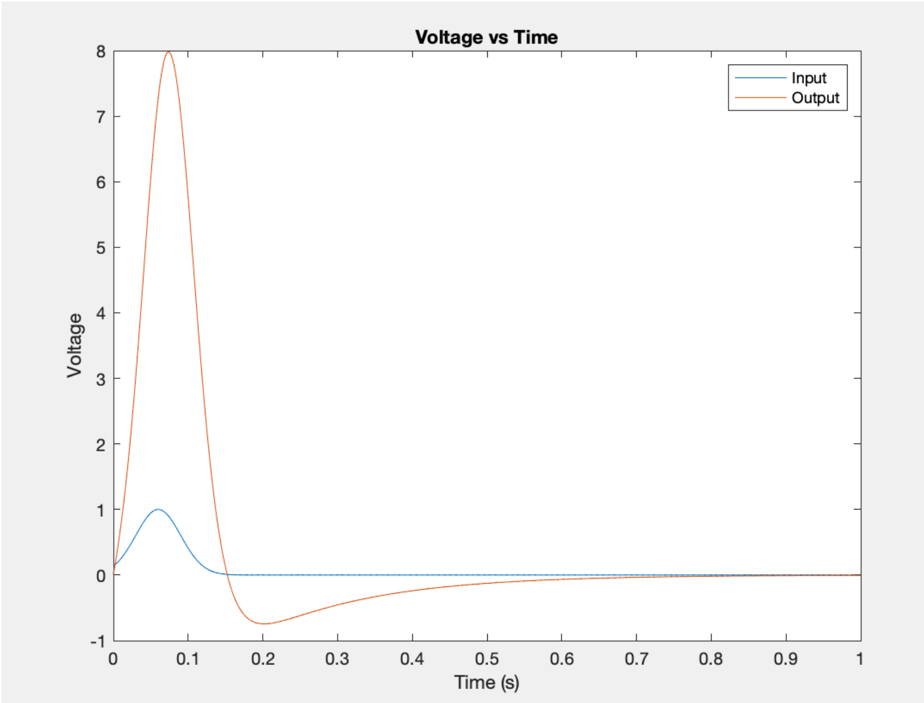

Figure 10. Plot of Input and Output Voltages for Gaussian Pulse

The Fourier Transform of the input and output signals were used in order to obtain the frequency response as can be seen below:

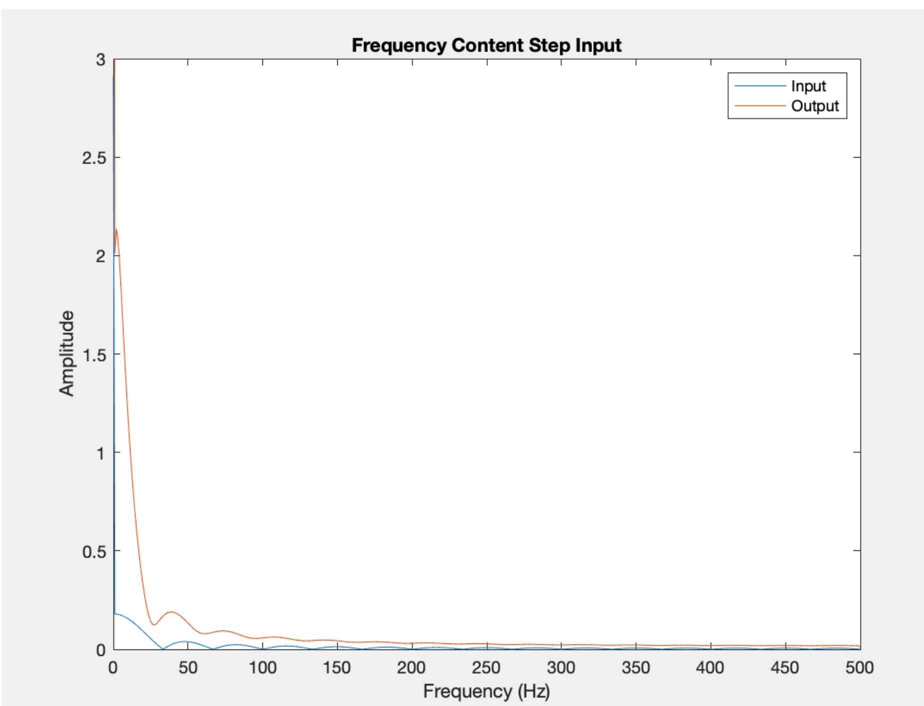

Figure 11. Plot of Frequency Content of Input and Output Voltage for Step Input

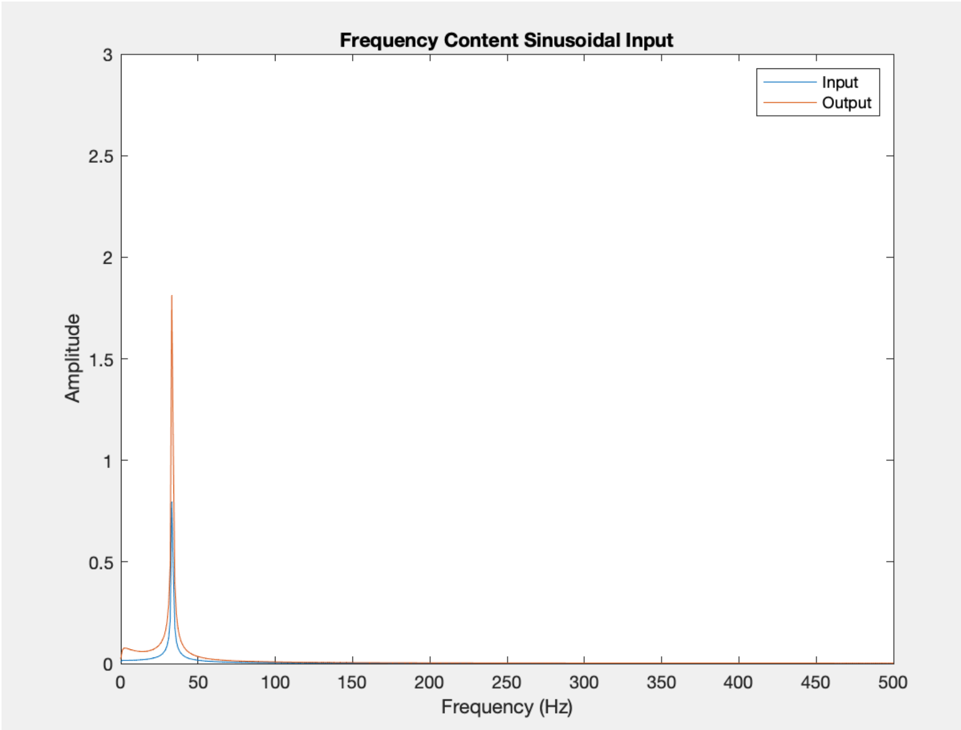

Figure 12. Plot of Frequency Content of Input and Output Voltage for Sinusoidal Input

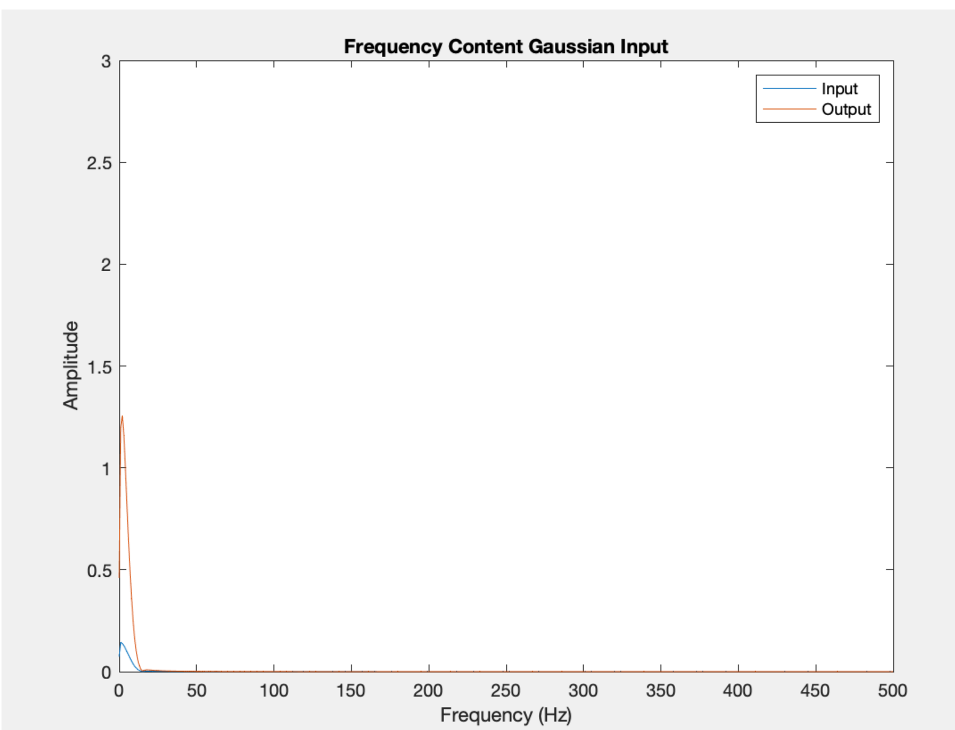

Figure 13. Plot of Frequency Content of Input and Output Voltage for Gaussian Pulse

PART 3

The third part of the assignment involves improving the circuit by adding a noise current source (In) and a capacitor (Cn), to bandlimit the noise in parallel with R3.

The added capacitor (Cn) produces an updated C matrix for the network can be seen below:

```
Cm =

         0         0         0         0         0         0         0
   -0.2500    0.2500         0         0         0         0         0
         0         0    0.0000         0         0         0         0
         0         0         0         0         0         0         0
         0         0         0         0         0         0         0
         0         0         0         0         0   -0.2000         0
         0         0         0         0         0         0         0
```

Figure 14. Updated C Matrix

The input and output voltage signals with noise using the gaussian excitation, along with its frequency response, was plotted as can be seen below:

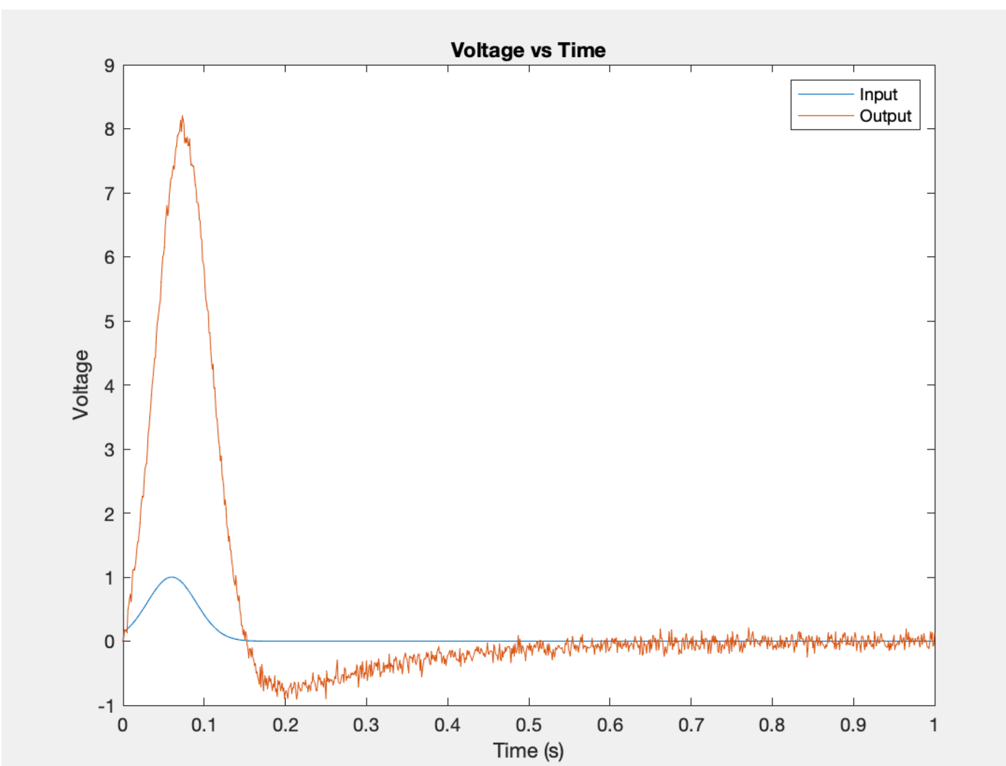

Figure 15. Plot of Input and Output Voltage with Noise for Gaussian Pulse

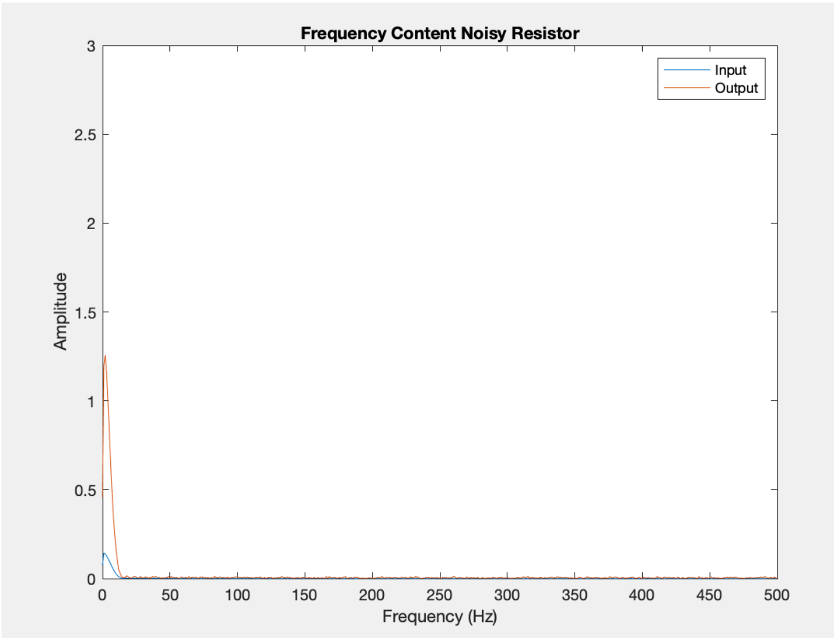

Figure 16. Plot of Frequency Content for Input and Output Voltage with Noise for Gaussian Pulse

The value of the added capacitor (Cn) was varied in order to see the effects on its bandwidth. The different capacitor values used were Cn = 0, Cn = 0.001, and Cn = 0.1 and the resulting input and output voltages were plotted as can be seen below:

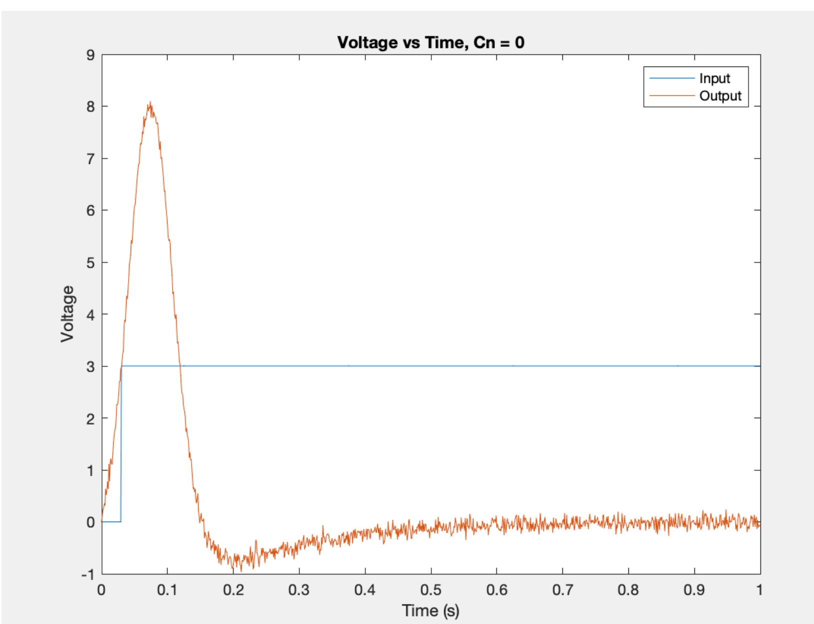

Figure 17. Plot of Input and Output Voltage with Noise for Gaussian Pulse (Cn = 0)

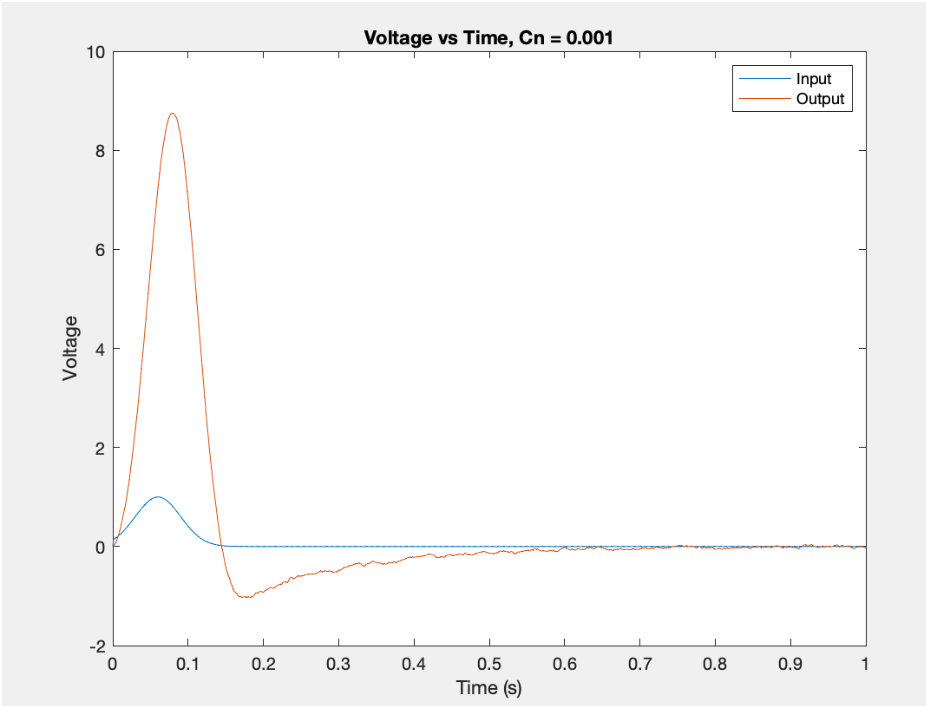

Figure 18. Plot of Input and Output Voltage with Noise for Gaussian Pulse (Cn = 0.001)

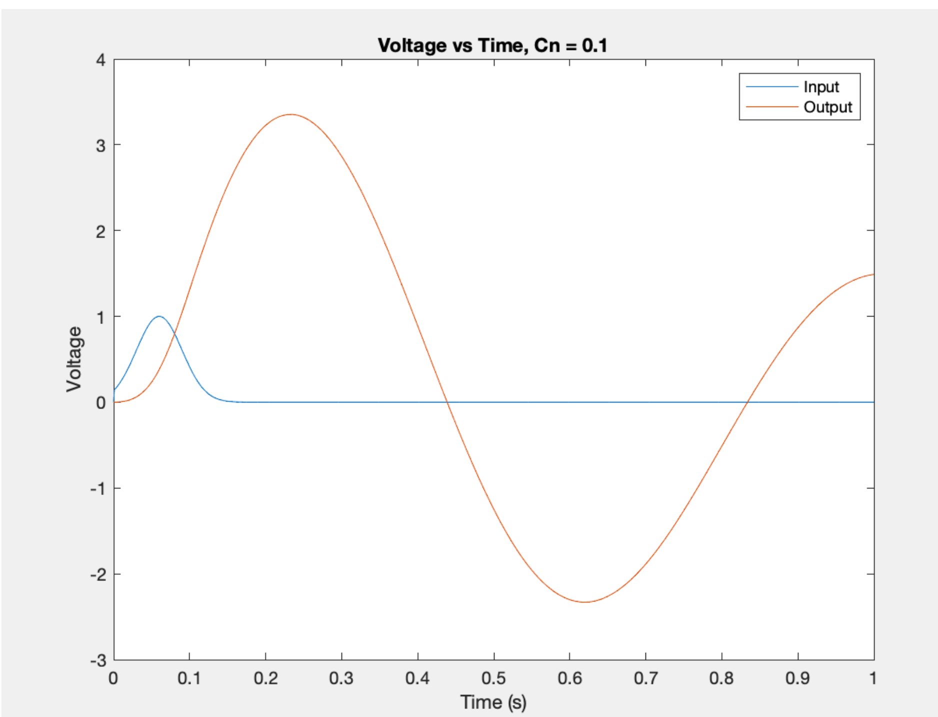

Figure 19. Plot of Input and Output Voltage with Noise for Gaussian Pulse (Cn = 0.1)

The results from Figure 17, 18, and 19 show that the noise is reduced with higher capacitor values; however, once a capacitor strength threshold is reached, the signal becomes distorted.

The time step (dt) was varied in order to see the effects on the simulation. The different time steps used were dt = 0.003 and dt = 0.01. The resulting input and output voltages were plotted as can be seen below:

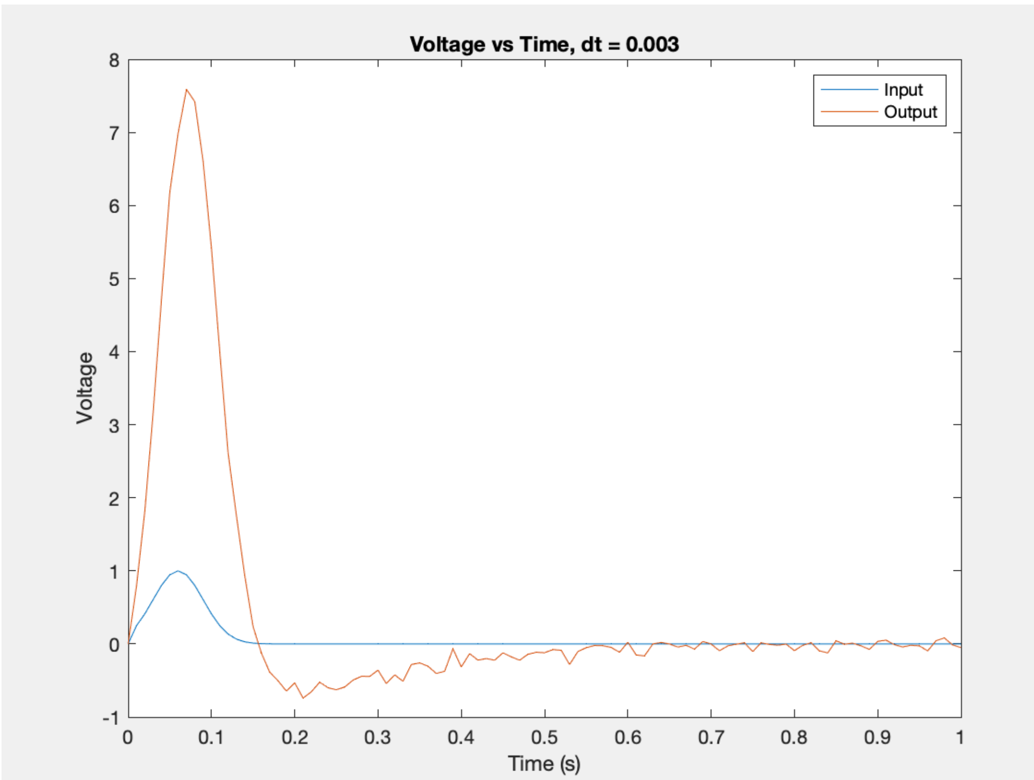

Figure 20. Plot of Input and Output Voltage with Noise for Gaussian Pulse (dt = 0.003)

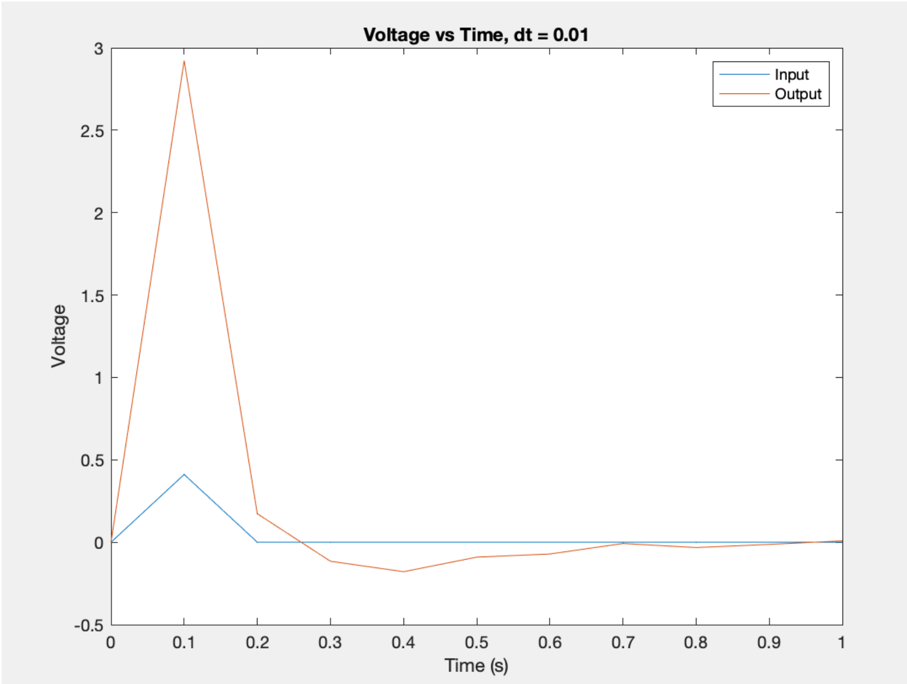

Figure 21. Plot of Input and Output Voltage with Noise for Gaussian Pulse (dt = 0.01)

The results from Figure 20 and 21 show that the larger the time step, the more inaccurate the signal becomes. Therefore, the Finite Difference approximation is inversely proportional to the step size.

PART 4

The final part of the assignment involves describing the steps necessary to implement non-linearity to the network and the subsequent changes that need to be made to the simulator.

In order to implement non-linearity to the network, a column vector would need to be added to the left side of the matrix equation and this would result in a change to the differential equations:

$$V_1 = V_{in} \qquad (10)$$

$$G_1(V_2 - V_1) + C_1\frac{d(V_2 - V_1)}{dt} + I_l = 0 \qquad (11)$$

$$G_3V_3 - I_l = 0 \qquad (12)$$

$$G_3V_3 - I_3 = 0 \qquad (13)$$

$$G_4(V_0 - V_4) + G_0V_0 = 0 \qquad (14)$$

$$V_2 - V_3 - L\frac{dI_l}{dt} = 0 \quad (15)$$

$$V_4 - (aI_3 + bI_3^2 + cI_3^2 = 0 \quad (16)$$

In order to apply this change to the simulator, G(7,7) = 1 and B(V)(7) = aI3 + bI3^2 + cI3^3. Moreover, since a non-linear system cannot be solved through Gaussian Elimination method, the Newton-Raphson method would have to be used to solve the system.