Electronic Design Project

Final Report

3-Lead Wireless ECG

ECG Live! ®

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Abstract

This document presents an overview of the design process undertaken, as well as the project specifications in the design and implementation of a low cost wearable ECG system. A detailed explanation of the various modules of the design and their implementations is provided. Each module was successfully simulated and then implemented.

There exists a demand for such systems as current implementations are complex to use, high in cost and inaccessible to the vast majority of South Africans. The system design aims to provide solutions to the problems encountered in acquiring from the body, as well as providing remote transmission, of ECG data. Two separate devices have been constructed to achieve the overall goal.

A remote device is attached to the person being monitored. The remote device acquires the raw ECG data from the Leads which are placed in predefined areas of the body. The necessary filter requirements (for ECG frequency band selection) and formatting of filtered ECG data (for transmission) both occur in the DSPic microcontroller which is present in the mobile unit. The data is transmitted wirelessly using a low-cost RF Transceiver.

A second Data acquisition unit is connected to USB port of a P.C. The unit has a second transceiver to receive and decode the data received from the remote unit. The data is then transmitted via the USB to the P.C for display. A user friendly graphical interface (GUI) was constructed using Visual Basic 6.0 enterprise edition. The GUI allows for the monitoring of real time ECG data. A database was implemented using MS Access 2000. This allowed for storage of the ECG data.

The report provides a theoretical section on the 3-Lead ECG as well as how the heart generates the ECG signal. The design is then dissected into various models which are discussed individually. A separate section is provided on the integration of these modules.

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List of Abbreviations

D.C	Direct Current (A)
EMF	Electromotive Force
A.C	Alternating Current (V_{RMS})
P.C	Personal Computer
GUI	Graphical User interface
IA	Instrumentation Amplifier
IC	Integrated Circuit
MIPS	Millions instruction per Second
p-p	peak to peak
ISR	Interrupt Service Routine
RF	Radio Frequency

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1. Introduction

An ECG is used to measure the electrical activity of the heart treated as a vector quantity. It measures the rate and regularity of heartbeats, the position of the various chambers, the existence of any damage to the heart and the effects of drugs and devices used to regulate the heart.

The potential created by the heart wall contraction spreads electrical currents from the heart throughout the body. The spreading electrical currents create different potentials at different points on the body. Leads are placed on the body in several pre-determined locations to provide information about heart conditions. The cardiac signal, typically 5 mV peak to peak, is an AC signal with a bandwidth of 0.05 Hz to 100 Hz (Section 4). The ECG signal is characterized by six peaks and valleys labeled with successive letters of the alphabet P, Q, R, S, T, and U (Figure 1).

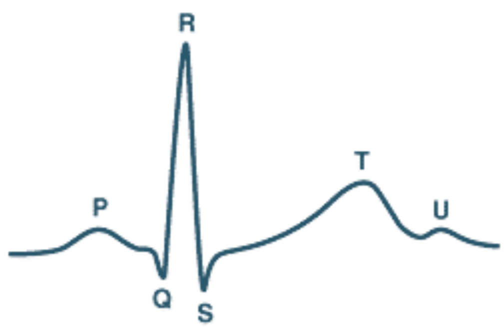


Figure 1: Typical ECG waveform[18]

The proposed design involves the implementation of a wearable three lead wearable ECG system. The primary objective is to keep the cost of the design as low as possible while still achieving industry standard performance. Two other constraints have been placed on the design:

- All signal conditioning and processing be done using a suitable processor.
- Wireless transmission be implemented using a suitable R.F transceiver.

Currently there are various wireless applications being employed in the health care industry. The most common are wireless pulse oxymetry, measuring the oxygen content in the blood. Another example is wireless temperature sensors in which the patient swallows a small transponder that will constantly transmit the body's core temperature.

2. The Heart

2.1. The Activity of the Heart

The main purpose of the heart is to pump blood throughout the body. The heart is divided into four chambers; the right atrium, right ventricle, left atrium and left ventricle. The right side of the heart delivers deoxygenated (carbonated) blood from the body to the lungs, and the left side of the heart delivers oxygenated blood from the lungs to the body.

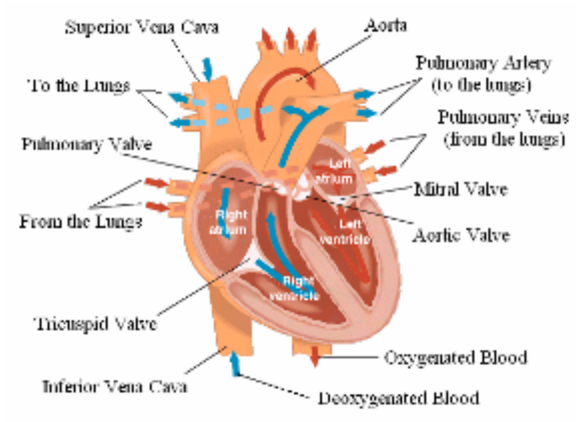


Figure 2: The Cross-Section of the Heart[14]

Deoxygenated blood enters the Right Atrium of the heart. The atria contract and push the blood into the Right Ventricle. The ventricles then contract and push the blood out of the heart, and thus to the lungs. The oxygenated blood from the lungs is returned to the Left Atrium. The Atria again contract and push the blood through into the Left Ventricle. The Ventricles again contract and push the blood to all parts of the body.

An electrical impulse is necessary to cause the heart to contract. The Sinoatrial Node (SA Node) is responsible for producing these impulses. The impulse from the SA node stimulates the atrial muscles causing both atria to contract and blood to flow into the ventricles.

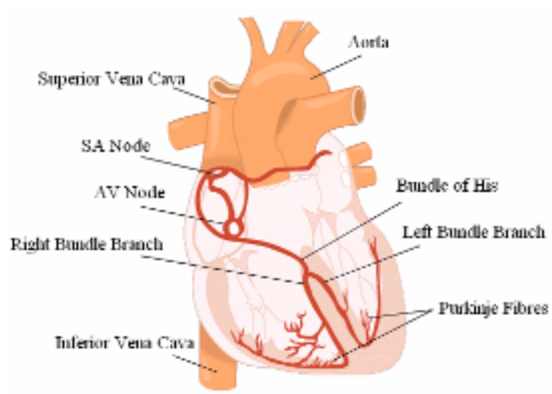


Figure 3: Electrical Conduction Path of the Heart[14]

The signal then reaches the Atrioventricular Node (AV Node) where it is naturally delayed to allow the atria to contract and fill the ventricles with blood. The signal continues down to a thick bundle of nerve fibres known as the Bundle of His. The bundle branches out to the left and right and terminate in tiny fibres known as Purkinje Fibres. These distribute the impulse to the cells of the heart muscle causing ventricular stimulation.

2.2. Depolarisation and Repolarisation

A resting heart is polarised; there is a balance of charge in and out of each cell within the heart muscle, and no electricity flows. A cell at rest has a negative charge. As a stimulus occurs, positive ions enter the cell, changing the charge to positive. This is depolarisation and occurs in every cell of the heart muscle, causing the fibres to shorten. The shortening of the heart muscle fibres causes the heart muscle to contract. The positive ions are pumped out of the cell, returning it to its normal shape, thus relaxing the heart muscle. This return of the cells to a polarised or resting state is known as Repolarisation.

The chemical make-up of the body allows the potential change, which occurs during depolarisation and repolarisation, to be transmitted and measured at the skin surface. The ECG is able to read this electrical activity which is displayed as waveforms; P, Q, R, S, T and U. Figure 4 illustrates the different waveforms for each of the specialized cells found in the heart.

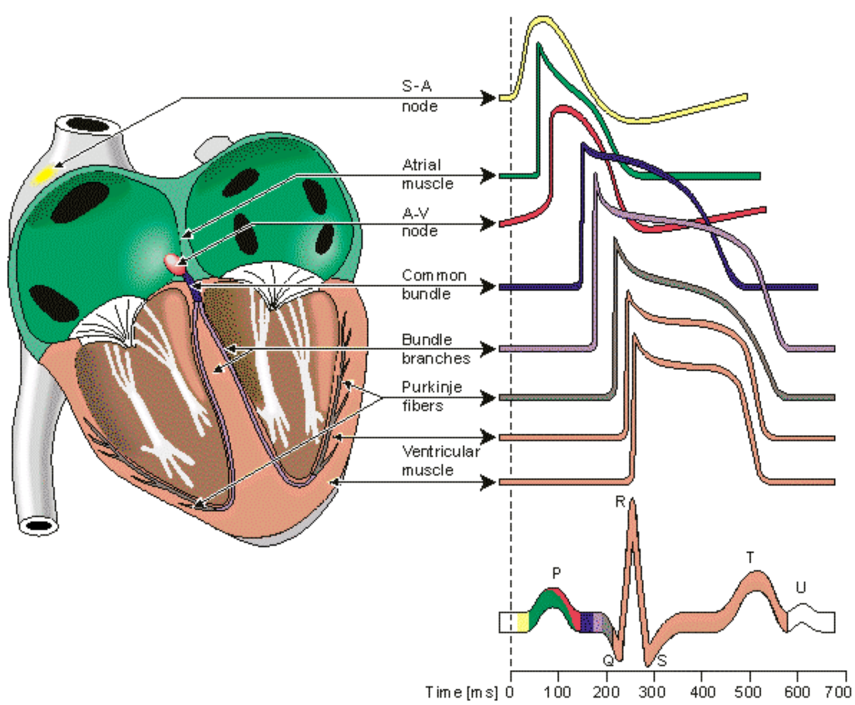


Figure 4: Electrophysiology of the Heart[15]

3. The Three Lead ECG

The electrical activity can be represented as a dipole (a vector between two point charges). The placement of the electrodes on the body determines the view of the vector as a function of time. Figure 5 represents the most basic form of the electrode placement which is based on Einthoven's triangle. This theoretical triangle is drawn around the heart with each apex of the triangle representing where the fluids around the heart connect electrically with the limbs. Lead I measures the differential potential between the right and left arms, Lead II between the right arm and left leg, and Lead III between the left arm and left leg.

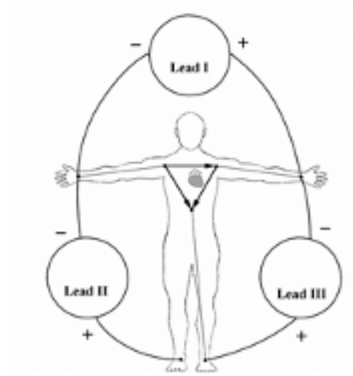


Figure 5: The Three Leads[16]

Einthoven's law also states that the value of any point of the triangle can be computed as long as values for the other two points are known. This point is crucial in the implementation of the design. It simplifies the overall analogue design and reduces the component count (and most importantly cost) as only two differential amplifiers are required. If any two leads (of the three lead ECG) are generated using the front end hardware the third lead may be generated entirely by software by simply subtracting (or adding) the two leads obtained from the analogue front end. The equations presented below verify the above statement. The Einthoven limb leads (standard leads) are defined in the following way:

Lead I: $V_I = \varphi l - \varphi r$ (1) φl = potential at the left arm

Lead II: $V_{II} = \varphi f - \varphi r$ (2) φr = potential at the right arm

Lead III: $V_{III} = \varphi f - \varphi l$ (3) φf = potential at the left foot

Manipulation of the above results yields:

$$\text{Lead I} + \text{Lead III} = \varphi l - \varphi r + \varphi f - \varphi l = \varphi f - \varphi r = \text{Lead II}$$

Similarly:

$$\text{Lead II} - \text{Lead I} = \text{Lead III}$$

4. ECG Frequency Bandwidth

The bandwidth of the ECG signal was critical in the Design of the entire system. The ECG bandwidth dictates key implementation aspects such as sampling rates and filter Bandwidths.

Research into the frequency components of the ECG waveform yielded a paper published by the Cardiovascular Research Laboratory at NASA on the spectral analysis of the ECG waveform [7]. The paper highlights the frequency components of an ECG signal for healthy adult males aged between 20 and 23. The paper yielded the following information:

- Amplitude information extends only to 200 Hz
- Waveform duration information lies below 60 Hz.

However the paper specified that the data was only valid for healthy males in the specified age group and that the frequency components in children especially, would differ considerably. A second paper labeled 'Minimum Bandwidth Requirements for Recording of Paediatric Electrocardiograms' [9] monitored 200 infants in their study of determining the maximum frequency components of the ECG signal. The study was carried out by passing the raw ECG signal through filters of varying bandwidths while employing a sampling frequency of 1500Hz. The signals were than processed using Matlab. The results of study showed that in 95% of test subjects a 150Hz filter bandwidth was sufficient to adequately represent the ECG. However the optimal filter Bandwidth was selected to be 250Hz (where the filter bandwidth refers to the Low pass filter cut-off frequency). The majority of studies on ECG spectral analysis concentrate on the higher end of the spectral analysis. Reference [10] and [8] however highlight the lower frequency component to be 0.05Hz. No indication however was given of how this value was obtained. Since Athletes typically have lower heart rates than the average person, a simple calculation was done to see if the 0.05Hz cut-off frequency was adequate in measuring the Athletes ECG signal. Assuming an athlete to have a heart rate of 32beats/min (Lance Armstrong, Tour De France Champion had a resting heart rate of 32beats/min at the peak of his powers [11]) this corresponds to a frequency of:

$$\frac{\frac{32beats}{\min}}{\frac{60\sec}{\min}} = \frac{32beats}{60\sec} = 0.53Hz$$

From the above result it can be seen that the ECG signal has frequency components below 1Hz.

5. ECG Interference Sources

As mentioned previously the ECG signals are typically in the millivolt range, and are hence susceptible to large amounts of interference, from a variety of sources. The interference sources can be divided into 3 distinct groups:

- Noise originating from sources external to the patient
- Interference originating from the patient
- Unwanted Potentials as well as interference originating from patient-electrode contact.

5.1. Noise originating from sources external to the patient

5.1.1. Electrostatic Sources

When a charged body is brought up close to an uncharged one, an equal & opposite charge develops on the uncharged body. For example if an unearthed body is close to any electronic device that is connected to the mains supply voltage, the body will develop a surface charge of equal & opposite potential even though no current is flowing between the two bodies. This phenomenon is commonly known as ESD (Electrostatic Discharge). ESD has been well documented in the recent past and extends a lot further than this particular case. The process of electron transfer as a result of two objects coming into contact with each other and then separating is known as 'triboelectric charging'. As the mains potential has a frequency of 50 Hz, the induced potential will also have this frequency. Other sources of electrostatic charge include the operating table, other persons, electronic equipment.

5.1.2. Electromagnetic Induction

An interference that occurs in the vicinity of wires carrying AC currents. Due to the generation of a magnetic field by the flow of a current, all conductors carrying mains currents are surrounded by electromagnetic fields. The South African Department of Public Works has published a document [5] categorizing the uninterrupted power supply in South Africa. The document states that mains supply is at a frequency of 50Hz with a tolerance of 2Hz i.e. The frequency may be anywhere in the range of 48Hz – 52Hz. The 50 Hz mains interference is a difference in potential, relative to ground, that is impressed upon any patient/subject in proximity to the wire carrying alternating (50Hz) main supply current; the patient takes on a potential that is neither that of ground, nor that of the mains, but rather, somewhere in between. Since the mains current is fluctuating (AC), the induced voltage of the subject is also fluctuating. The effect is however minimised by the fact that the electromagnetic field generated by the live wire is to a large degree cancelled out by the neutral cable flowing adjacent to the live cable but in the opposite direction.

5.2. Noise originating from the patient

An electromyogram (EMG) measures the electrical activity of muscles at rest and during contraction. Analysis of the EMG [6] shows that the frequency (Hz) components of both the EEG & ECG both lie within the same band. The EMG signal however is typically five times larger (up to 30mV) than that of the ECG signal. Muscular activity (especially shivering) can lead to large interference in any ECG signal since they occupy the same frequency band.

5.3. Noise originating from patient-electrode contact

ECG electrodes do not act as a passive non-invasive conductor. The placement of any metal adjacent to an electrolytic solution (gel on ECG pads combined with surface of skin) produces an electrochemical half-cell, similar to (although a lot less complex) than that of a battery, resulting in potentials on the surface of the skin. If a differential amplifier is connected to a pair of such electrodes it will amplify any difference in potentials. Ideally if the cells are identical the output will be zero. If the potentials however are not identical, any difference between the two electrodes will be amplified. Additionally, the small current produced by the offset potential may result in polarisation. Polarisation of the electrode will further distort any signal.

6. Feasibility Study

A crucial aspect of the design process was determining the feasibility of a Low-Cost wireless ECG system. In a country were health care is constantly under the spotlight, it seemed obvious to validate if a niche market was present in South African health care system for a Low-Cost ECG device.

The health care system in South Africa consists of a large public sector which provides medical care (facilities, personnel and medication) to the vast majority of the population. Public health care cost consumes annually, 62 billion rand (Roughly 10%) of the government's total budget. Public Health care however is currently desperately under resourced with people in the rural areas finding it very difficult to travel to hospitals and clinics which are largely based in the larger metropolis and there surrounding areas.

In a recent attempt to make health care more accessible to the underprivileged, the department of health has decided to launch a fleet of mobile health clinics that are set up in large ambulance type vehicles. Massive revamps have also been ordered on existing clinics and rural hospitals that do not meet department standards. A low cost easily manoeuvrable ECG machine is one of the key requirements for these clinics to deliver an adequate and accurate service to persons using this service.

The low cost ECG apparatus also finds potential use in the private health care sector. Pharmacies and General Practitioners (G.P) may also provide ECG tests to their customers and patients for early detection of possible heart conditions. The device may also be used by private nurses who provide medical care to patients in their homes.

Although low cost is the primary objective for the project, low power consumption and ease of use by both patient and doctor is also a key requirement.

Current ECG systems make patient monitoring cumbersome and difficult. The ECG leads are frequently dislodged from the patient by persons in the examining or operating room. This causes serious complications because in an operating scenario it appears to the monitoring station that the patient is going into cardiac arrest. Another issue inherent within the currently employed ECG system is the obstructive nature of wires and leads decreasing mobility of doctors and nurses. A solution to this would be to design an ECG that utilises wireless data transmission as much as possible to eliminate the need for wires.

7. Functional Specifications

The following are the functional specifications for the ECG:

- To provide a real time 3-lead ECG trace on a P.C.
- A simple intuitive GUI that may be used by a person with no medical background.
- Transmission of data from remote unit is initiated from the GUI.
- Easy setup and installation of entire system.
- Two separate units. A portable unit that is attached to the person being monitored. A second unit interfaces directly to the P.C and acquires data that is being transmitted wirelessly.
- The portable device is light weight, compact and unobtrusive.
- User plugs P.C unit into USB port for reception of data.
- Visual feedback is provided to the user/s on the portable device via an LED to inform user that the ECG portable unit has been switched on. An additional pair of LED's is provided to indicate the successful reception and transmission of ECG data.
- A simple but concise manual will be provided on the operation of the device.

7.1. UML Case Diagram

A Use Case Diagram was used to develop the requirements of the ECG from the veiw of the user, i.e the doctor, nurse or in some cases the patient. The purpose of the ECG from the user is to observe the ECG trace and store it for later viewing. If the trace is not visable, the possible problems are included in the diagram.

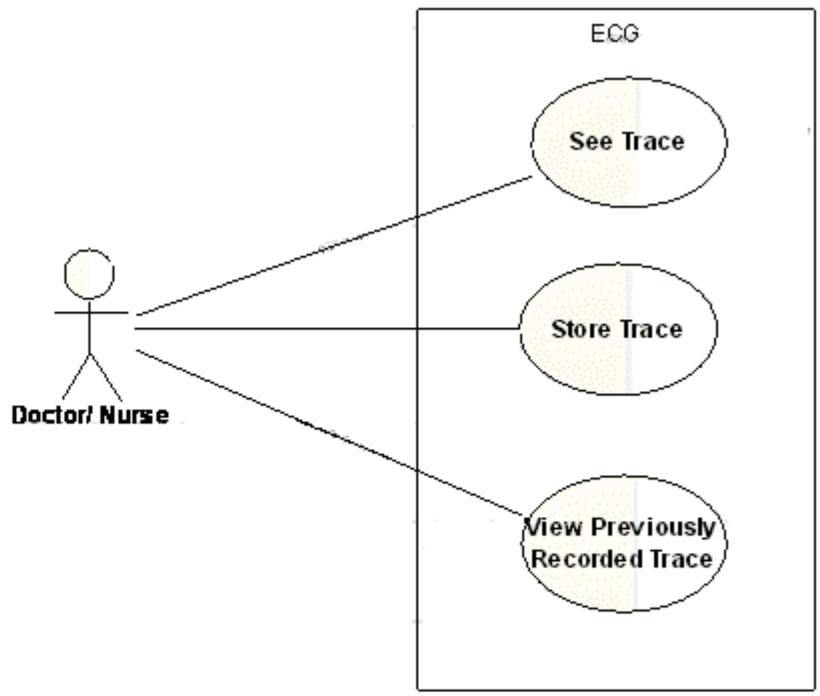


Figure 6: The UML Use Case Diagram

8. Non-Functional Specifications

As mentioned previously the design is broken down into two components. A mobile unit is attached to the person being monitored. A second unit is attached to the P.C.

At the core of the mobile unit is a low cost Digital Signal Processor (DSP), the DSPic30F3012. The DSPic is responsible for processing the raw ECG data acquired from the analogue front end hardware, before aligning the data for transmission. The primary purpose of choosing such a high performance processor is to perform all the necessary filtration in the digital domain thus reducing the overall size, power consumption, efficiency and cost of the mobile device.

The ECG leads interface directly to mobile unit's analogue circuitry. Peripheral components are added between the patient and circuitry to maximize impedance seen by the circuit and hence decrease overall current flow through to the patient. The analogue front end will use the typical approach employed by the majority of current ECG designs with an instrumentation amplifier (IA) and a right leg common-mode feedback op amp.

The use of digital filters was a constraint placed on the design. The implementation utilizes Infinite Impulse Response (IIR) to perform the necessary ECG frequency band selection.

The filtered ECG signal is transmitted via SPI (Serial Peripheral Interface) to a radio frequency (RF) Transceiver, (provides the wireless link from the portable unit to base station.).

The P.C unit receives the data (Corresponding Transceiver). A microcontroller is required to decode the received R.F signal. It will then communicate with the P.C via USB plotting the resultant ECG traces on the P.C screen using a custom written Visual Basic 6.0 application (VB6). Communication is achieved between VB6 and the P.C unit by using the MSCOMM control.

9. System Requirements

The host PC with the following minimum requirements will be used as the data acquisition and display unit:

- Microsoft Windows 98 or higher.
- Intel Pentium II 300MHz processor or equivalent.
- 32MB RAM.
- 21MB available hard disk space.
- USB 1.1 Compliant
- An Available USB port

Thy system requirements are derived from the minimum requirements for USB 1.1 and Visual Basic. The final implementation with the MSComm plug-in is 20.3MB. However the memory requirements are largely dependant on the size of the database, which varies for different scenarios.

10. System Block Diagram

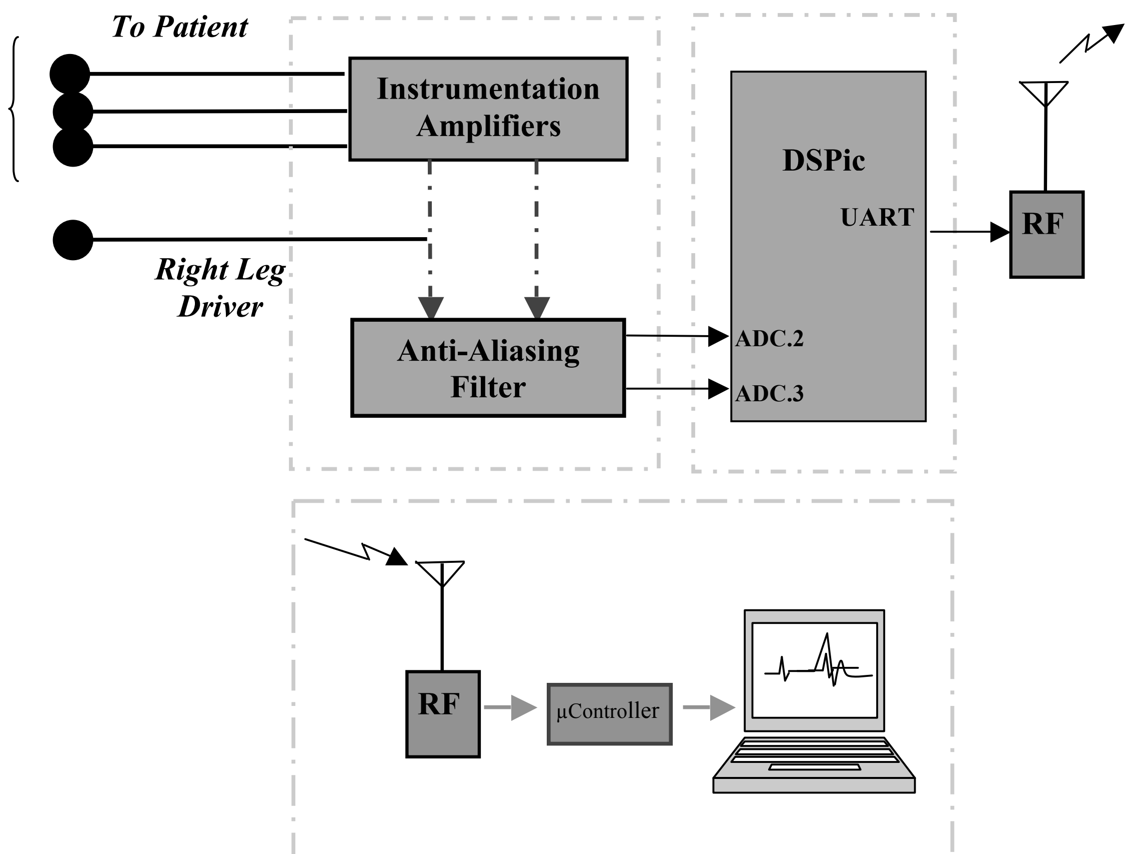


Figure 7: System Block Diagram

11. Wearable ECG Hardware

The wearable ECG system can be divided into different modules, that when integrated produces the final product. Hence this section discusses the hardware modules associated with the wearable ECG.

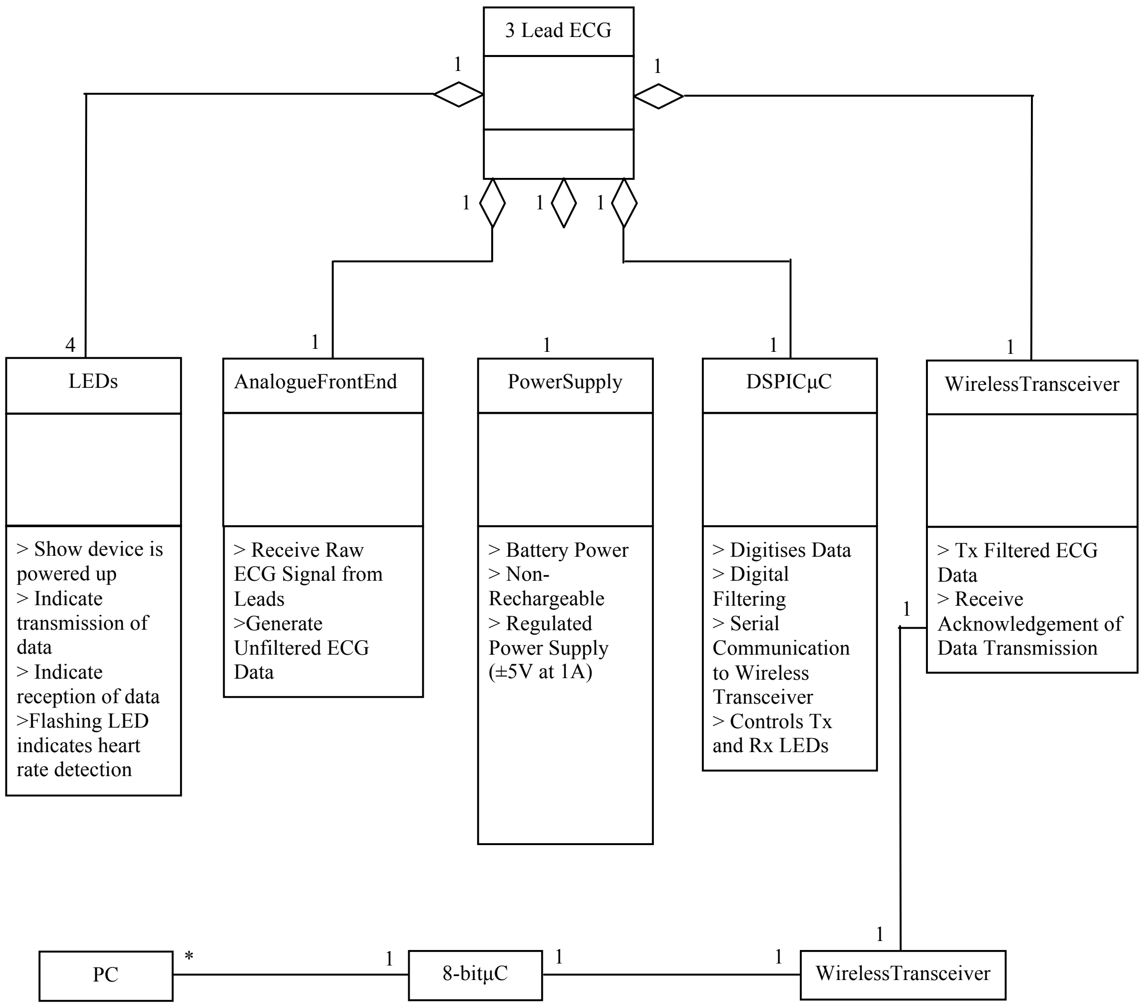


Figure 8: Hardware Module Description

The above diagram above illustrates the hardware structure of the entire system and briefly lists the role that each constituent plays.

11.1. DSPIC30F3012 16-Bit Microcontroller

An 8-bit microcontroller could not be used as the implementation required intensive computations. Furthermore a microcontroller that supported simple DSP instructions such as multiply and accumulate (MAC) and floating point operations was required. Additionally the microcontroller required the following peripherals:

- At least 2 ADC channels
- UART
- 2 × I/O pins

Options from both Analogue Devices and Texas Instruments were investigated along with the DSPic option. Table 1 below highlights the 3 options that were investigated. The cost criterion includes the cost of a compiler and development board. This largely dictated the choice in processor as the project had to be within budgetary constraints. The DSPic rated highly on this criterion as the compiler was provided by Microchip for free. As performance is often measured in MIPS this criterion was also considered. Here again DSPic surpassed its competitors. The MIPS rating was twice that of its nearest competitor.

		High Performance Microcontroller					
		DSPic		MSP430		ADuC842	
Criteria	Weighting	Rating	Score	Rating	Score	Rating	Score
Cost	4	5	20	2	8	1	4
MIPS	5	4	20	2	10	2	10
Memory	2	5	10	1	2	3	6
Total			50		20		20

Table 1: Scoring Matrix for the 16-bit Microcontroller

All the initial development was done on the 40Pin DSPic30F4013. On completion it was evident that a 40 pin microcontroller was not necessary as most of its peripherals and I/O pins were not in use. Using a smaller microcontroller would also lower the overall power consumption in the design. The 18 pin DSPic30F3012 was selected for the final implementation. The 30F3012 met all the requirements as well as having a typical input current of 5.8mA as compared to the 7.1mA with the 30F4013.

11.1.1. Analogue to Digital Converter

The DSpic30F3012 has a single onboard 12 bit Analogue to digital Converter Peripheral. The microcontroller has 7 ADC channels with a 16 word result buffer. These channels are all multiplexed to the same converter. As with most microcontrollers only a single channel can be converted at a time. The implementation may select from as few as 1 to as many as 16 sample buffer locations to be filled between interrupts. To maximise efficiency the implementation generates an interrupt after 16 samples have been written to the buffer. The DSPic ADC however allows for a greater degree of control with respect to sample acquisition time, conversion time and interrupts.

11.1.2. Programmable Serial USART

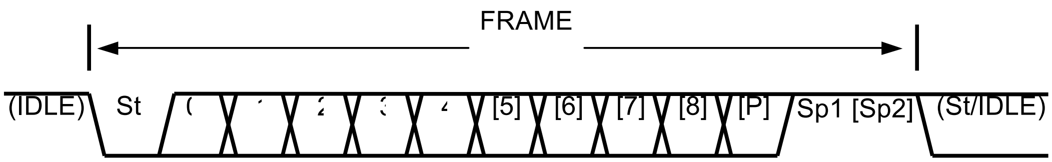
Serial Communication involves the transmission of multiple data bits over a single wire. The Universal Synchronous and Asynchronous serial Receiver and Transceiver (USART) of the DSPIC30F3012 microcontroller is used to asynchronously communicate with the wireless transceiver.

Important features of the DSPIC30F3012 USART

- Full Duplex Operation
- Synchronous and Asynchronous Operation
- High Resolution BAUD Rate Generator
- Frame Error Detection
- Noise filtering including False Start Bit Detection
- Three interrupts: Receive Complete, Transmit Complete, and Transmit Data Register Empty

Frame Format

A serial frame is defined to be one character of data bits, with synchronisation bits and an optional parity bit.



IDLE: No transmission on communication lines
St: Start Bit. Always low
(n): Data Bits. Bits within brackets are optional
P: Parity Bit (Optional)
Sp: Stop Bit

Figure 9: Frame Structure for the transmission of 1 character [1]

11.3. Aerocomm AC4486 wireless transceiver

A low cost wireless solution was required in the implementation. Wireless modules that utilize the Zigbee and Bluetooth protocols are high in cost and hence fall out of the scope of the project. Various single I.C solutions were investigated. The modules that were investigated are highlighted in table 2 below.

		Wireless Transceiver					
		Cypress Wireless USB		Nordic NRF905		Aerocomm AC4486	
Criteria	Weighting	Rating	Score	Rating	Score	Rating	Score
Cost	5	4	20	5	25	4	20
Data Rate	5	3	15	3	15	4	20
Total			35		40		40

Table 2: Scoring Matrix for the Wireless Transceiver

Initially the Nordic NRF905 wireless transceiver was selected for the design. However implementation of the transceiver proved to be a problem as they were very sensitive to voltage variations. Two transceivers were destroyed during the implementation phase. A more robust alternative was sought that met the necessary criteria. Investigation yielded the AC4486 transceiver; although slightly higher in cost the transceiver met all other requirements. An additional feature was internal surge protection which made the option seem a lot more attractive after the misfortune encountered with the NRF905.

The Aerocomm AC4486 is a cost-effective, high performance transceiver. It employs an asynchronous TTL scheme communications. Communications include both system and configuration data. The transceiver supplies data for transmission to other transceivers and may be used to implement a star topology network. Configuration data is stored in on-board EEPROM. All RF system data transmission/reception is performed by the transceiver. For one to one data transmission the transceiver may be programmed once at design time with the necessary configuration settings.

11.3.1. Power Supply

A ± 5V power supply was required to power up the mobile unit. Both the microcontroller and the wireless transceiver required a +5V supply for operation. The Analogue front end however required a dual rail supply (± 5V).

The prototype system was powered using an external D.C source (Bread Board). Prior to the design of the Power Supply the current consumption of each component was measured. The measured results together with the typical and absolute maximum ratings are tabulated below.

Quantity	Device	Supply Voltage	Measured Current	Peak Current	Average Current
2	AD620	5V	2.3mA	2.6mA	1.8mA
3	OPO7	5V	2.31mA	3.3mA	2.34mA
3	TLO84	5V	4.2mA	5.4mA	4.2mA
1	DSPic30F3012	5V	0.77mA	8mA	5.8mA
1	AC4486	5V	6.8mA	9mA	7mA
			16.38mA	28.3mA	21.14mA

Table 3: Current Measurement

The current at the output of he 7905 regulator was measured to be 22mA (on the bread board.

The major factor influencing the design of power supplies is regulator topology.

11.3.1.1. Regulator Topology

The three popular topologies are:

- switching regulators
- Linear Regulators
- Switched Capacitor

Switched Capacitor topology is typically used in applications that require peak currents less than 150mA [17]. Placing these devices in parallel however, effectively doubles there output current. Single chip solutions are readily available. Most voltage inverter regulators utilise this topology.

The table below provides a comparison between switching and linear regulators.

Type	Switching	Linear
Operation	Step Up, Step Down, Invert	Step Down
Complexity	High	Low
Cost	High	Low
External Components	High	Low
Ripple/Noise	High	Low

Table 4: Comparison of Switching and Linear Regulators

The primary benefit of the switching regulator topology is their ability to boost (step up) any input voltage. They are highly efficient reaching efficiencies of up to 90% [17]. This reduces the overall cell (battery) count required in portable applications. This is a key motivating factor in the design of any battery powered device as the physical dimensions of the battery is critical to the overall size of the device. The foremost deciding factor was based on the requirement of a low noise power supply as the ECG signal is susceptible to various kinds of interference. Since a clean ECG trace is the primary requirement of the design, linear regulators were selected.

11.3.1.2. Power Supply Implementation

A 9V Duracell battery is used in the implementation of the power supply (Appendix D)

11.3.1.2.1. Voltage Inversion Using Switched Capacitor I.C

Two charge pump regulators were selected to generate the required negative voltage. The ICL7660 was used for this purpose. The devices were placed in parallel halving there overall output resistance hence doubling their output current capability. The output current from the implementation was measured to be 38 mA at voltage of -8.59V. The implementation followed the outline in the datasheet. The schematic is presented in Appendix D.

11.3.1.2.2. ±5V Regulated power supply

The 7805, 7905 regulators were used in the implementation. They are both able to supply 1A of current. The power supply is simulated using electronics work bench (Appendix D). Both regulators are loaded until breakdown in the simulation. The 7805 is successfully able to deliver 910mA before breakdown. The 7905 however only supplied 632mA. However this is more than sufficient for the purpose of the design.

11.4. Analogue Front End

The ECG device must be able to deal with extremely weak signals obtained from the electrodes. These signals are typically in the range of 0.5 mV to 5.0 mV [8]. Furthermore the signal is coupled with a D.C component of up to ±300 mV [8] which results from the electrode-skin contact, plus a common-mode component of up to 1.5 V [8] , resulting from the potential between the electrodes and ground.

The analogue interface circuitry uses the typical approach employed in most commercially available ECG systems. The front-end circuitry uses an instrumentation amplifier (I.A) and a right leg common-mode feedback op amp, which is commonly referred to as a ' right leg driver '.

11.4.1. Differential Amplification

The ECG leads interface directly to the inputs of the differential amplifier. Since the ECG signal is in the millivolt range, a highly sensitive differential amplifier is required for ECG measurement. The differential amplifier is required to perform the necessary subtraction of various potentials on the surface of the body. This subtraction action is required to generate the three lead vectors. Any of the three lead vectors may be generated in hardware by simply connecting the appropriate part of the body to the inputs of the differential amplifier. Further noise reduction techniques however will have to be employed at the output of the differential amplifier to obtain noise free ECG trace. The amplifier is also required to provide amplification to these millivolt range signals while strongly attenuating signals common to both inputs. CMRR describes the ability of a differential amplifier to reject interfering voltages (V_{CM}), common to both inputs, and to amplify only the difference between the inputs. Various types of circuits have been used in the implementation of differential amplifiers, but the most popular design is the configuration shown in figure 10 [4] above. Operational amplifiers OA1 and OA2 provide infinite input impedance while simultaneously passing the common mode voltage

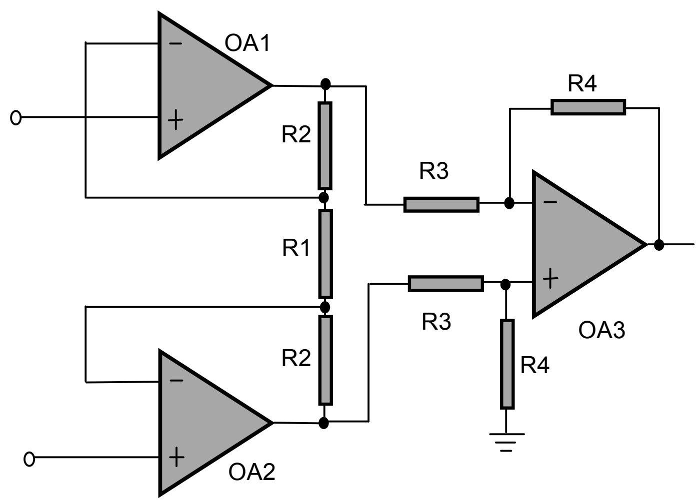


Figure 10: Three Operational Amplifier Differential Amplifier

through and amplifying the differential voltage. Its differential gain A_d, and common mode gain A_c, are given by the following equations:

$$A_d = \left(\frac{1}{2} + \frac{R_2}{R_1}\right)\left(\frac{R_{4,top}}{R_{3,bottom}} + \frac{R_{4,top}}{R_{3,top}}\left(\frac{R_{4,bottom}}{R_{3,bottom} + R_{4,bottom}}\right) + \frac{R_{4,bottom}}{R_{3,bottom} + R_{4,bottom}}\right) \tag{4}$$

$$A_c = \left(1 + \frac{R_{4,top}}{R_{3,top}}\right)\left(\frac{1}{1 + \frac{R_{3,bottom}}{R_{4,bottom}}}\right) - \left(\frac{R_{4,top}}{R_{3,top}}\right) \tag{5}$$

The configuration utilizes three op-amps. The circuit's optimal performance in terms of stability, differential gain and high common mode rejection ratio (CMRR) are difficult to compete with when using other discrete component implementations.

Accuracy in matching of the resistors is an important consideration in the design of a discrete component differential amplifier. The slightest error in the matching of resistances $R_{3,top}$ $R_{3,bottom}$, and $R_{4,top}$, $R_{4,bottom}$ in the discrete implementation (figure 9) results in unwanted common-mode amplification. Assuming we use 1% resistors:

$$\frac{R_{3,top}}{R_{4,top}} = (1 - \varepsilon)\left(\frac{R_{3,bottom}}{R_{4,bottom}}\right) \tag{6}$$

Or

$$R_{3,top} = (1 - \varepsilon)R_{3,bottom} \tag{7}$$

with

$$R_{4,top} = R_{4,bottom} \tag{8}$$

Substituting the above results into equation 5 yields the unwanted common mode gain which is given by:

$$A_c = \frac{-\varepsilon R_{4,top}}{R_{3,top} + R_{4,bottom}} \tag{9}$$

Where ε represents the percentage error present in the resistors.

11.4.2. Differential Amplifier Design

The characteristics of the discrete differential amplifier (Figure 10) may be improved by combining the three individual amplifiers in to a single IC, commonly known as an Instrumentation Amplifier. Instrumentation Amplifiers such as the AD620 and INA114 with input impedances in the range of 10GΩ/pF, vastly outperform the discrete component implementation discussed in the previous section. The AD620 draws a maximum supply current of 1.3mA [3] as compared to a general purpose JFET operational amplifier such as the OP07 which draws 20mA [2] per chip, resulting in a total supply current of 60mA for the configuration shown in Figure 9. Table 3 illustrates some key characteristics of three different instrumentation Amplifiers. Large scale VLSI integration ensures that the resistors within these Instrumentation Amplifier are matched to within 0.1% thus reducing common-mode gain (Equation 9).

IA Type	AD620	AMP01	INA114
CMR(Gain=100)	130dB	125dB	115dB
Accuracy	0.15%	0.18%	0.18%
Noise	9nV/Hz	10nV/Hz	11nV/Hz
Power Requirements	1.3mA	4.8mA	2.2mA
Input Current	0.5nA	4nA	2nA

Table 5: Instrumentation Amplifier Comparison [2],[3],[4]

Although other options were investigated the AD620 was selected as it was the only instrumentation amplifier that was readily available. It also satisfied the budgetary constraints of the design.

The AD620 requires only a single external gain-setting resistor; the gain equation is given by:

$$Gain = 1 + \frac{49.4k}{R_G} \tag{10}$$

Figure 11 illustrates the AD620 connection scheme utilized in the implementation. This method was utilized because two separate amplifiers needed to be interfaced to the right leg common-mode driver. Two 22k resistors are placed in parallel with the gain resistor. The right leg driver interface is at the centre of these two resistors. The two 22k resistor modify the gain equation. The gain of the AD620 is given by:

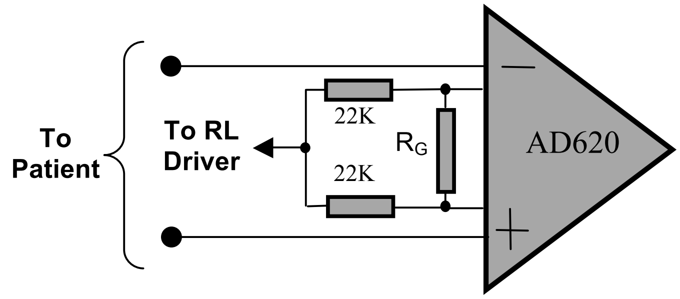


Figure 11: AD620 Instrumentation Amplifier [8]

$$Gain = 1 + \frac{49.4k}{R_G} + \frac{49.4k}{2} \times \frac{1}{22k} \quad (11)$$

The AD620 has a maximum gain of 1000 [2] ideally we would like to set the gain here to some maximum value thus eliminating the requirements for an additional gain stage prior to microcontroller stage. The gain selection of the AD620 is however critical to the design of the entire system. The gain must be set such that output saturation of the ±5V power supply does not occur. As mentioned above the maximum input is ±5 mV plus a variable normal-mode dc offset of up to ±300 mV [8]. By setting the gain resistor to 6.2k it ensures that the maximum output swing is 3.07V i.e. Gain = 10. The gain was verified by grounding the negative input and passing waves of varying amplitude into the amplifier while observing both the input and output waves on an oscilloscope.

11.4.3. Anti-Aliasing Low-pass Filter

An anti-aliasing Low-Pass filter is required to band limit the incoming ECG signal prior to digitization. Once the converted ECG signal is "Contaminated" with Aliased Noise, it takes time and memory within the processor to eliminate the noise. Furthermore it eliminates the effects of overdriven signals that usually occur beyond the bandwidth of the filter. The anti-aliasing low-pass analogue filter is placed immediately before the ADC.

The three most popular filter types are the Butterworth, Bessel and Tschebyscheff. Listed below are the key characteristics of these filters:

- The Butterworth coefficients, optimize the pass-band for maximum flatness
- The Tschebyscheff coefficients, sharpening the transition from pass-band into the stop-band
- The Bessel coefficients, linearise the phase response up to f_C.

11.4.4. Anti-Aliasing Low-pass Filter Design

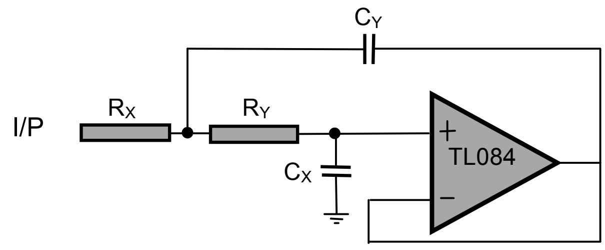


Figure 12: Sallen key Low-pass Filter

The anti-aliasing filter cut-off frequency (f_C) is set to the highest ECG frequency component of interest (f_{max}) so that $f_C = f_{max}$. As mentioned previously a maximum frequency component of 250Hz is present in the representation of ECG signals. The filter was hence designed to have a cut-off frequency of 250Hz. The Sallen and Key active filter configuration was preferred to the Multiple Feedback due to its less component count. The Butterworth filter was selected due to its pass-band flatness. Since the ECG signal is so small in magnitude, any ripple in the pass-band would only further attenuate the signal making its recovery more difficult. A simple fourth order low-pass filter was designed for this purpose. Figure 12 shows a second order low-pass filter block. Two of these are cascaded to form the fourth order filter. The calculation of the component values along with the corresponding bode plot is present in the Appendices (A1).

11.5. Removing the D.C Offset Component

Initially the output of the differential amplifier was interfaced directly to the Anti-aliasing filter with out removing the D.C offset component. Observing the signal at the output of the filter while using this configuration showed that the signal ranged anywhere between 45mV – 3.7V. This was unacceptable as the 45mV signal was too small to be adequately represented digitally with a 12 bit Analogue to Digital Converter (See Resolution). Simply adding a gain stage would cause the output to saturate if it fell in the volt range. Since the magnitude of this signal could not be reliably predicted it was decided that the DC offset component be removed. This was achieved by simply placing a 100µF capacitor, at the output of the differential amplifier. Observing the output of the filter after placing the capacitor yields an output ranging from24-63mV.

11.6. Signal Offset and Gain stage

The DSPic's on board Analogue to Digital converter peripheral is uni-polar, i.e. it cannot digitize signals below ground level. For this reason the signal being input to the DSPic must be level shifted. The DSPic

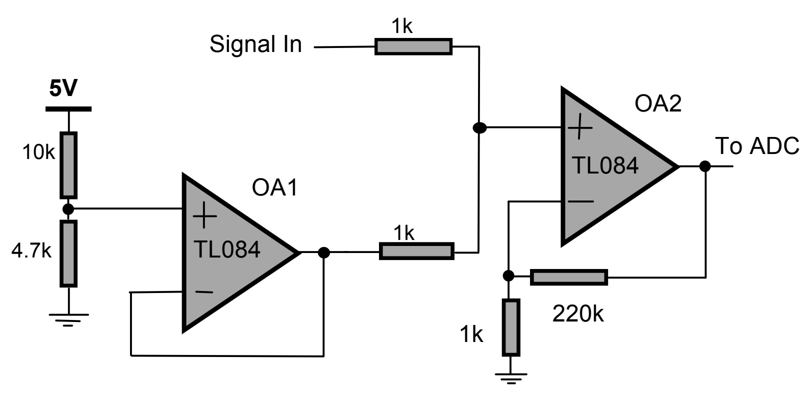


Figure 13: Gain and Offset Stage using 2 op-amps

runs of a 3.3V supply. This requires that the input to the DSPic be within the 0-3.3V range. The 10k and 4.7k resistors form a voltage divider. The output of the divider is given by:

$$\frac{4.7k}{4.7k+10k}\times 5V = 1.59V$$

The output of OA1 is simply a buffered version of the voltage divider. The operational amplifier is utilized as it has very high input impedance. This ensures that no resistive loading occurs on the input signal.

Operational amplifier OA2 is configured in the non-inverting summer configuration. The circuit has a total gain of 48. The filtered signal is simply added to the output of OA1 which causes it to be centred at 1.59V.

11.7. The Right-Leg Common mode feedback circuit

The purpose of this circuit is to provide an inverted version of the common-mode interference to the user's right leg, with the intention of cancelling out the interference. Additionally it serves as a virtual ground, for the ECG signal. The operational amplifier utilized in this circuit is the OP07 which is a low power, high precision junction field effect transistor (JFET) operational amplifier with an extremely high CMRR of about 106 dB minimum. A common sense point is established in order to drive this amplifier, also known as a force amplifier. The output from the circuit passes current through the user until the net sum output from the differential amplifier is zero. The amplifier is given a low pass cut off frequency of 100Hz by setting resistor R_{hf} and capacitor C_{LP} (R_{LP} = 12k C_{LP} = 100nF).

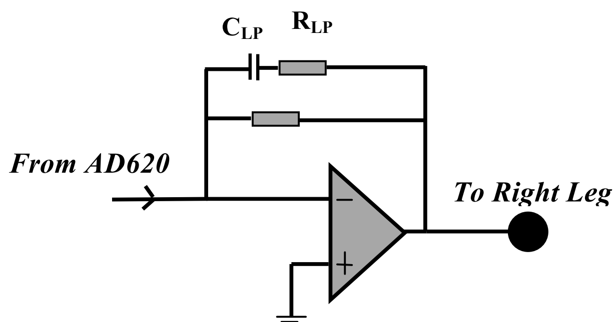


Figure 14: Right Leg Driver

11.8. DC Restoration Amplifier

Due to the sensitivity of the AD620 Instrumentation amplifier, the output of the amplifier is highly susceptible to any variation in contact resistance between the

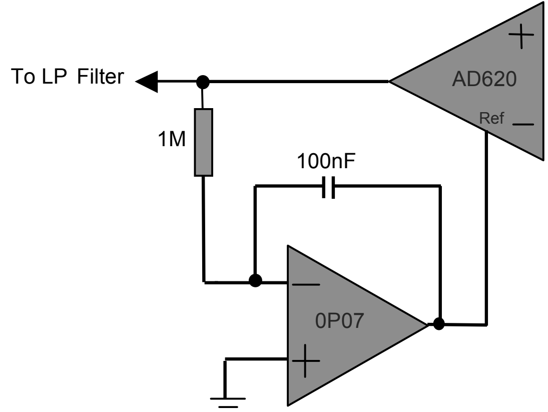


Figure 15: AD620 with DC Restoration Scheme

skin and electrode. This condition results in a deviation of the D.C content of the amplified differential signal and manifests itself as a drift in the baseline of the ECG signal. This phenomenon is often referred to as baseline wander. The problem is overcome by utilizing an analog integrator scheme highlighted in Figure 15. The integrator scheme integrates the dc content of the 10× amplified Raw ECG signal and feeds it back to the reference pin of theAD620. The feedback action allows the AD620 to maintain a constant DC level at the output, regardless of the change in skin contact resistance.

11.9. Results and Analysis of the Analogue Front End

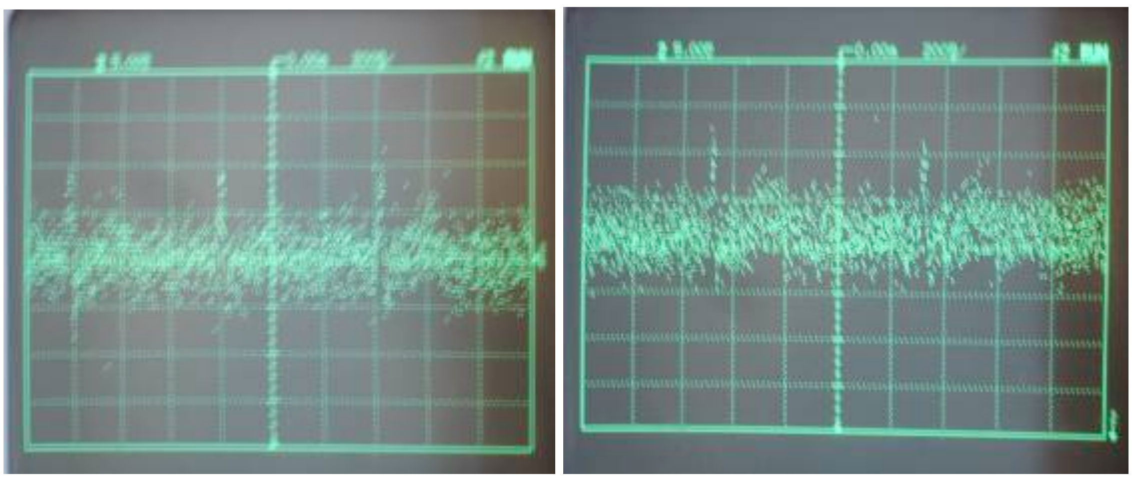


Figure 16(a): Lead1 Signal Prior to Offset and Amplification stage
Figure 16(b): Lead1 Signal prior to Offset and Amplification stage with D.C. Blocking Cap Removed

The output of the Low pass filter prior to the offset and gain stage was measured using an oscilloscope. Figure 16(a) illustrates the Lead1 ECG signal. The signal is approximately 20mV p-p and is centred at 0V. The Instrumentation amplifier gain was set to ten, which implies that the raw signal prior to amplification of the ECG is 2mVp-p. The 2mVp-p signal falls within the typical ECG signal range. This result was required in the Design of The GUI. To highlight the effect of the D.C offset component in the signal the D.C blocking capacitor was removed. Figure 16(b) illustrates the Lead1 ECG signal with the capacitor removed. The ECG signal is now centred at 77mV. This highlights the necessity of the blocking capacitor.

FT232RL

The Ft232RL I.C converts serial Data to the USB protocol. The driver create a virtual comport on the P.C that allow serial communication via USB. The host unit interfaces to the P.C via the FT232Rl. The royalty free drivers may be downloaded from the site FTDI site

12. Microcontroller Firmware

All the DSPic30F3012 Hardware modules discussed previously are utilized in the Microcontroller Firmware implementation. The Firmware is also broken down into various modules. This was done to ensure that the various functions could be reused. It also simplified the debugging process considerably.

The design, simulation and Implementation of the IIR digital filter are included in this section, as they are implemented in the DSPic30F3012.

Figure 17 highlights the process undertaken in the main method of the programme. All the highlighted modules have been successfully implemented.

The implementation utilises the USART to transmit filtered Data to the AC4486 wireless transceiver.

The Call_Filter() block represents the function which performs the necessary filter action. The filters are all made up of IIR type. The main method waits for the ADC ISR to set the Do_Filter flag which is set when new data is available to be filtered.
The transceiver ready function formats data into a packet and employs a simple Ack/Nack communication Structure.

However due to space considerations protocol the Communication protocol structure is discussed in detail in the GUI section of the report

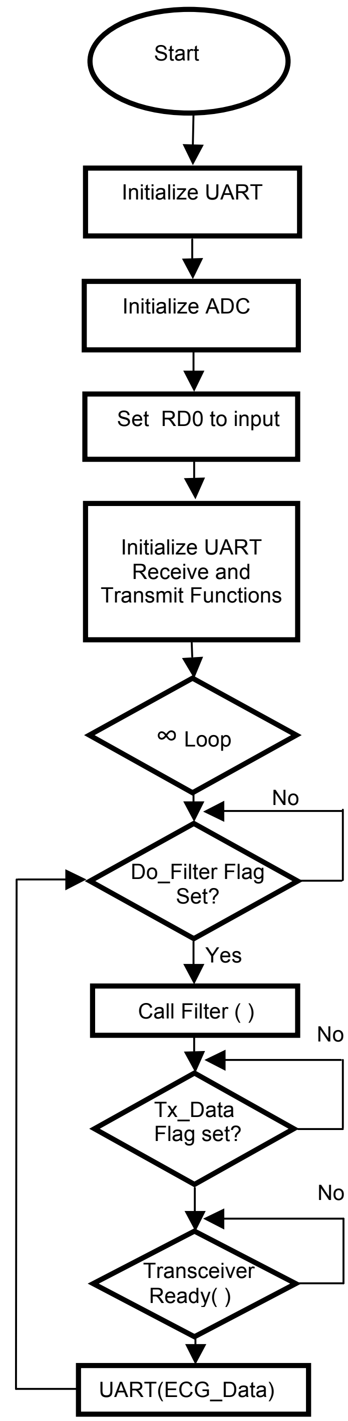


Figure 17: DSPic Microcontroller Main Method

12.1. Analogue to Digital Converter Initialization

The sampling rate must conform to Nyquist sampling theorem which states:

"For a band-limited (Finite Bandwidth) signal with maximum frequency f_{max}, the equally spaced sampling frequency f_s must be greater than twice of the maximum frequency f_{max}, i.e.,

$$f_s \geq 2 \cdot f_{max}$$

In order for the signal be uniquely reconstructed without aliasing" [12].

The frequency $2 \cdot f_{max}$ is called the Nyquist sampling rate. f_{max} is commonly referred to as the Nyquist frequency. For the ECG system $f_{max} = 250$Hz. The sampling frequency therefore needs to be set to a minimum of 500Hz. The ADC sampling frequency however is set up to be 8 KHz. This is due to the DSP algorithm that is required to filter the raw ECG data.

12.1.1. ADC Sampling Frequency

The first major operation is to take a sample of an analog input and hold that sample for analysis. The sample is then held in the sample and hold amplifier. Sufficient time must be given to the converter to capture an accurate representation of the signal. The A/D will then analyze the output of the sample-and-hold amplifier and convert the information into a digital number. The DSPic30F4013 datasheet [13] specifies that the conversion time be set to a minimum of 10µs.

ADCS bits together with the SAMC bits (figure 18) in the ADCON3 register set the acquisition time and the peripheral clock period. The total sample time (T_{SAMP}) may be defined as:

$$T_{SAMP} = T_{ACQ} + T_{CONV} \qquad (12)$$

A sampling frequency of 8 KHz correlates to a sample time of 125µs (T_{SAMP} = 125µs). Where T_{CONV} is the time required for the ADC to complete a conversion. T_{ACQ} is defined as the total acquisition time. The ADCS bits in the ADCON3 register define the ADC clock period which is denoted as T_{AD} where:

$$T_{AD} = \frac{T_{CY}(ADCS + 1)}{2} \qquad (13)$$

T_{CY} in equation (13) represents the DSPic instruction cycle time. The DSPic is being driven using an external crystal of frequency 7.3728MHz. This corresponds to instruction cycle time:

$$T_{CY} = \frac{1}{f_{CRYSTAL}} = \frac{1}{7.3728 \times 10^6} = 135.6ns \quad (14)$$

The only constraint in setting the sampling frequency is the minimum conversion time. The datasheet however recommends that the acquisition time be set as high as the application allows, thus ensuring accurate representation of the signal. As mentioned above the SAMC bits in the ADCON3 register (figure 18) defines the sample acquisition time. Setting The SAMC bits to a maximum of 31, yields a T_{ACQ}:

$$T_{ACQ} = 31 \times T_{AD} \quad (15)$$

The ADC requires 14 ADC clock periods to complete a conversion. The total conversion period T_{CONV} is given by:

$$T_{CONV} = 14 \times T_{AD} \quad (16)$$

Substituting (15) and (16) into (13) yields:

$$T_{SAMP} = 45 \times T_{AD} = 125\ \mu s \quad (17)$$

Or

$$T_{AD} = 2.78\mu s \quad (18)$$

Substituting (18) into (13) and rearranging for ADCS yields an ADCS value of 40.

ADCON3 Register

-	-	-	SAMC<4:0>				
bit15	14	13	12	11	10	9	bit8

ADRC	-	ADCS<5:0>					
bit7	6	5	4	3	2	1	bit0

Figure 18: ADCON3 Register with ADCS and SAMC bits[13]

12.3. ADC Interrupt Service Routine

As mentioned above the ADC is set up to sample at a rate of 8 KHz. An interrupt however is only generated after all 16 buffer levels have been full. The two channels are stored in successive slots in the buffer.

The interrupt service routine provides a simple averaging function. It reads the 8 available values per channel and takes an average. The quantized value is the passed to the digital filter. The above action makes new values available to the filter every 1ms. This was done in the hope that it would smooth the signal. Figure 19 represents the ADC ISR Flow chart.

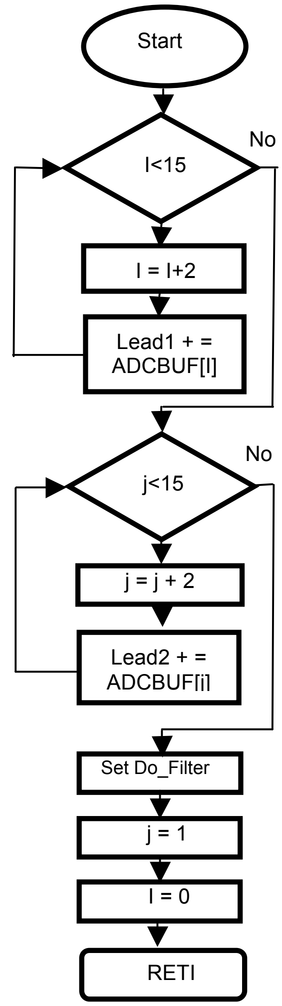


Figure 19: ADC ISR

12.4. Serial USART

As mentioned previously the UART function is utilized for Transmission of filtered data to the AC4486 transceiver. Figures 20 and 21 represent the flow chart for the custom written, receive and transmit Functions

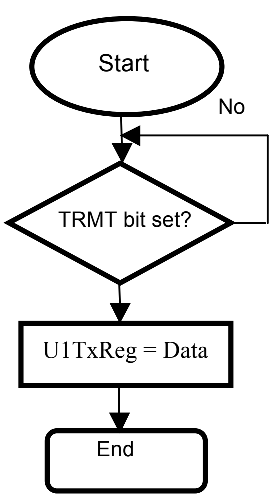


Figure 20: UART Transmit Function

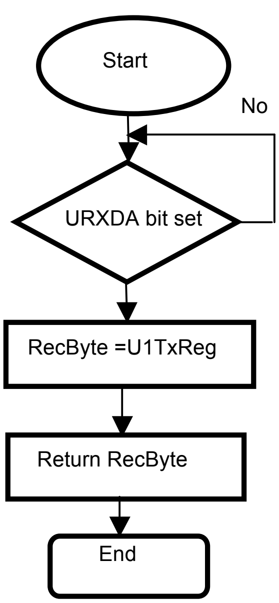


Figure 21: UART Receive Function

12.5. Digital Filters

Digital filters are required to perform the necessary frequency band selection. The analogue front end has blocked out the D.C component. The implementation employs a low-pass and notch filter. A simple function was written in Matlab to generate an ECG trace. The user can input the frequency of interference, and call the function when ever an ECG trace is required. The function was used in the verification of the design.

12.5.1. Digital IIR Notch Filter

The notch filter is required to remove 50Hz interference present from the mains supply (section 5). The filter is first specified in the Analogue Domain and then transformed into the digital domain using the bilinear transformation method.

For the purpose of the wearable ECG, a second second-order digital notch filter having a notch frequency at 50Hz and a 3-dB notch bandwidth of 6Hz (Due to tolerance levels of mains frequency) is required. The sampling frequency employed is 1000Hz. The normalised angular notch frequency ω_0 and the normalised angular 3-dB bandwidth B_ω are therefore given by

$$\omega_0 = 2\pi\left(\frac{50}{1000}\right) = 0.1\pi, \qquad \mathrm{B}_\omega = 2\pi\left(\frac{6}{1000}\right) = 0.012\pi.$$

Substituting these values in equations B6-1 and B6-2 (Appendix B), we arrive at

$$\alpha = 0.96299, \qquad \beta = 0.95106.$$

Then, substituting the above values in equation B4, we arrive at the desired transfer function

$$G(z) = \frac{0.981495 - 1.86692z^{-1} + 0.981495z^{-2}}{1 - 1.86992z^{-1} + 0.96299z^{-2}},$$

whose gain and pole-zero plot are plotted in figure 20b and 20d respectively. Figure 20a represents an ECG signal with 50Hz interference superimposed onto it. The signal is generated using the ecgplusint( ) function. Finally figure 20c represents the effect of using the above transfer function on the ECG signal with 50Hz interference.

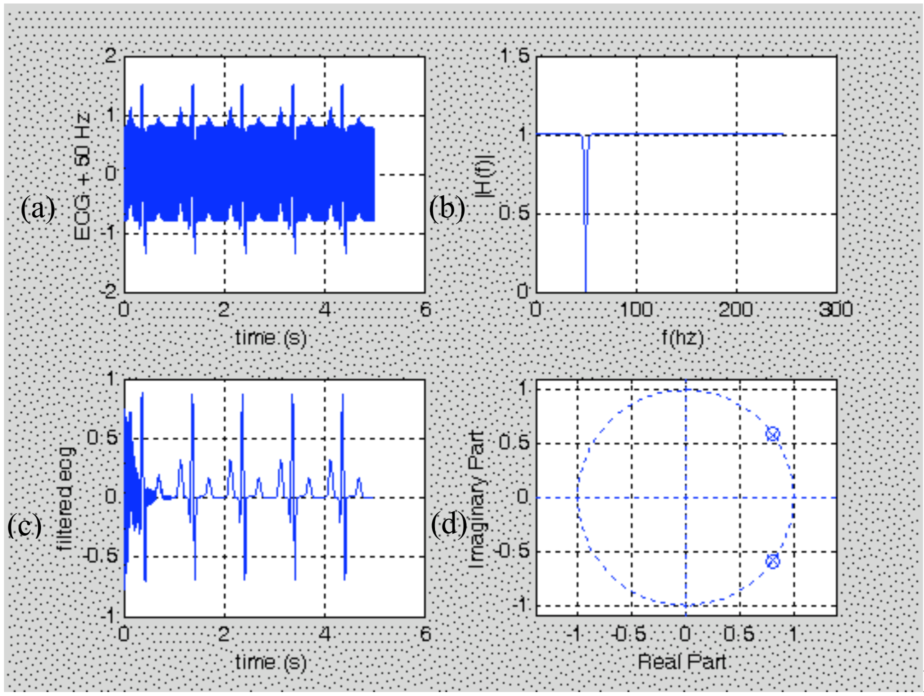


Figure 22(a): Unfiltered ECG Signal
Figure 22(b): Notch Filter Magnitude Response
Figure 22(c): Filtered ECG Signal
Figure 22(d): Pole-Zero Diagram

The derived transfer function is then converted to a recursive algorithm (difference equation).

$$G[n] = 0.981495 \times x[n] - 1.86692 \times x[n-1] + 0.981495 \times x[n-2] + 1.5164 \times g[n-1] - 0.96299 \times g[n-2]$$

Where n represents the current input or output.
This equation is then implemented on the processor using C code.

12.5.2. Low Pass 4th order IIR Filter

The Matlab function butter() was used in the design of the low pass filter. The function designs an Nth order low pass, digital Butterworth filter and returns the filter coefficients in length N+1 vectors B (numerator) and A (denominator). The coefficients are listed in descending powers of z. The cut-off frequency W_n must be $0.0 < W_n < 1.0$, with 1.0 corresponding to half the sample rate. This function was used as it reduced development time significantly. Various filter Bandwidth options while varying the order could also be tested.

The code snippet below uses the butter() function to generate the necessary coefficients for a second order Butterworth filter with a 100Hz cut-off frequency. The ecgsig() function is then employed to generate a an ECG signal with 200Hz interference (figure 24a). The generated ECG signal is then filtered using convolution and the resultant trace is plotted (figure 24b). Finally figure 24c tests the filter as it will be programmed on the DSPic30F4013.

```
% IIR filter
% Initialization
fs=1000; %sampling frequency, 1000 Hz
%
%       Low-pass filter second order

% fc=100Hz ; fs=1000Hz ; fs/2=500Hz ; Wn=fc/(fs/2)=100Hz/500Hz=0.2
[b,a] = butter(2,0.2);        % 2nd order low-pass filter fc=100Hz

% Generate noisy ECG signal (200Hz interference)
[ecgsig]=ecgplusint(4,200,0.8,0);
% filter the noisy ecg signal using convolution
new_sig=filter(b,a,ecgsig);
figure(2);
subplot(221);
plot((1:length(ecgsig))/fs,ecgsig);grid on;zoom on;
xlabel('time (s)');
ylabel('ECG + 200 Hz');
subplot(222);
plot((1:length(new_sig))/fs,new_sig);grid on;zoom on;
xlabel('time (s)');
ylabel('filtered ecg');

        %Checking that filter as it will be programmed
% Fc = 100Hz
% a = 1.0000   -1.1430    0.4128
% b = 0.0675    0.1349    0.0675

filter_signal=zeros(1,length(ecgsig));
filtered_signal(1)=0;
filtered_signal(2)=0;
for i=3:length(ecgsig),
   filtered_signal(i)=b(1)*ecgsig(i)+b(2)*ecgsig(i-1)+b(3)*ecgsig(i-2)-a(2)*filtered_signal(i-1)-a(3)*filtered_si
end
subplot(223);
plot((1:length(filtered_signal))/fs,filtered_signal,'r');grid on;zoom on;
```

Figure 23: Matlab Code for 4th Order Low Pass IIR Filter

The transfer function generated from the above code snippet needs to be converted to a recursive algorithm.

The transfer function for the Low pass filter H(z) is given by:

$$H(z) = \frac{0.0675 - 0.1349z^{-1} - 0.0675z^{-2}}{1 + 1.143z^{-1} - 0.4128z^{-2}}$$

Converting this to a recursive algorithm:

$$H[n] = 0.0675 \times x[n] - 0.1349 \times x[n-1] - 0.0675 \times x[n-2] - 1.143 \times g[n-1] - 0.4128 \times g[n-2]$$

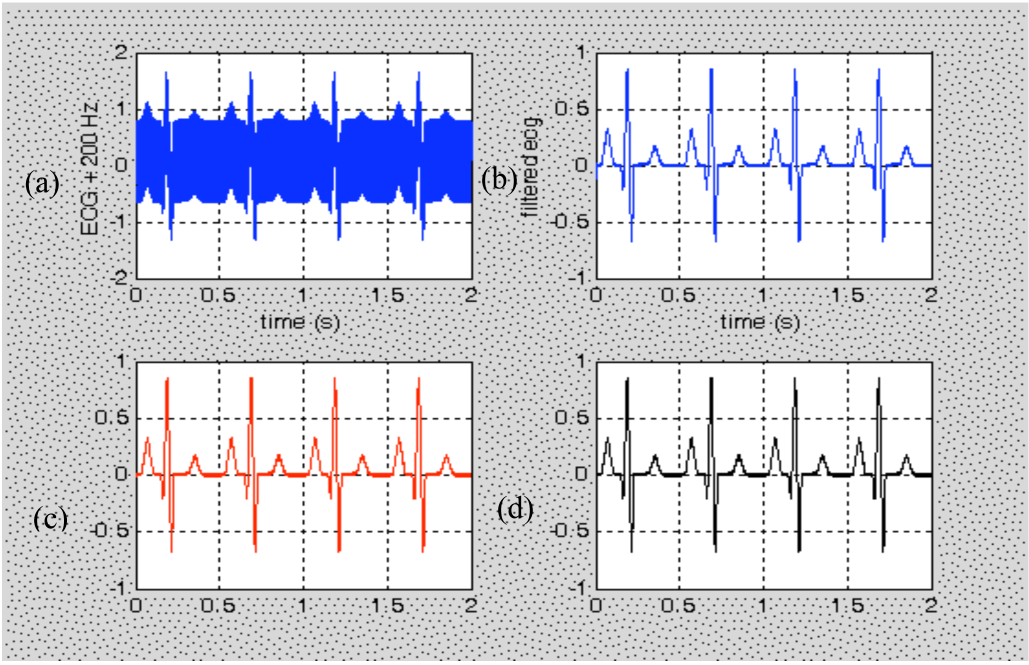


Figure 24: Simulation Results of 4th order low-pass IIR Filter

12.5.3. DSPic30F3012 Implementation of IIR Digital Filters

Figure 25 below illustrates the actual C code implementation (Call_Filter function) on the DSPic30F3012. Initially the filter was implemented using a for/loop structure. However this caused a slight yet noticeable delay between the two filtered signals. This proved to be a problem in the generation of the third Lead Vector.

The duration to run a single iteration of the filter was also of importance as the filter computations needed to be completed before new data became available from the analogue to digital converter. Also sufficient time was needed for successful transmission of data. The stopwatch tool in the Microchip C30 compiler was used to measure the exact duration of the filter implementation. **The total time for a single iteration was 209µs. This value is critical in the calculation of the data rate requirements.**

```
Low1[0] = (0.0675*raw1[0]-0.1349*raw1[1]-0.0675*raw1[2]-1.143*Low1[1]-0.0675*Low1[2])
Low2[0] = (0.0675*raw1[0]-0.1349*raw1[1]-0.0675*raw1[2]-1.143*Low2[1]-0.0675*Low2[2])
Notch10[0] = (0.982*Low11[0] -1.867*Low1[1] + 0.981*Low1[2] +1.516*Notch10[1] -0.96299*Notch10[2]);
Notch20[0] = (0.982*Low2[0] -1.867*Low2[1] + 0.981*Low2[2] +1.516*Notch20[1] -0.96299*Notch20[2]);

raw1[2] = raw1[1];
raw1[1] = raw1[0];
raw2[2] = raw2[1];
raw2[1] = raw2[0];
Low1[2] = Low1[1];
Low1[1] = Low1[0];
Low2[2] = Low2[1];
Low2[1] = Low2[0];
Notch10[2] = Notch10[1];
Notch20[2] = Notch20[1];
Notch10[2] = Notch10[1];
Notch20[2] = Notch20[1];
Notch10[1] = Notch10[0];
Notch20[1] = Notch20[0];
```

Figure 25: C code implementation of Digital Filters

12.5.4. Results and Analysis of Digital Filters

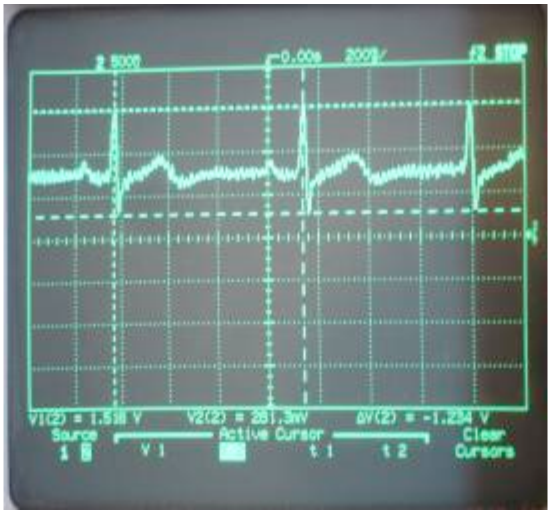
The DAC4814 was utilized in verifying the output of the digital filter. The 12 bit DAC has a serial interface. The device was chosen due to availability and familiarity. A DAC was used as the signal needed to be properly categorized and measured prior to the implementation of the GUI. Both 12 bit and 8 bit resolution was experimented with.

Lead	Lead I	Lead II
V_{MAX}	1.516V	1.61V
V_{MIN}	281mV	93.75mV
V_{P-P}	1.234V	1.52V
Frequency	1.21Hz	1.2Hz
Heart Rate	72 Bpm	72 Bpm

Table 6: Lead Vector Characteristics

Figure 26(a) represents the Lead I signal. Lead I was output using 12bit resolution. Lead II was output using 8 bit Resolution. Table 6 highlights the individual characteristics of each wave.

The peak to peak voltage of Lead II is greater than Lead I. This conforms to standard (Healthy) ECG signals. The frequency component is almost identical as they should be. However there is still an element of interference in the measured results as compared to the simulated results. This stems from the manner in which the simulated results are generated. The custom written ecgplusint( ) function only allows a single frequency of interference to be input, which is non-ideal in a real world situation.



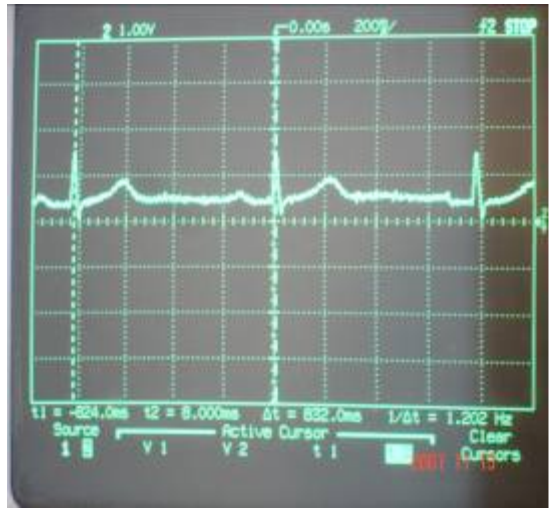


Figure 26(a): Filtered Lead I output with 12 bit resolution

Figure 26 (b) Filtered Lead II output with 8 bit resolution

13. Wireless Communication

Filtered ECG data obtained from the mobile unit is to be transmitted wirelessly to the host unit attached to the P.C. The Aerocomm AC4486 wireless transceiver was selected for this purpose. PIN 7 of the transceiver triggers low when data is ready to be written to the transceiver.

For one to one data transmission the configuration settings may be programmed once at design time into the transceivers onboard EEPROM memory. A single transceiver must be configured as a Server and there may be multiple Clients. The ECG Live! Implementation has the server attached to the Host unit. This allows for later development of possibly implementing a wireless network of multiple ECG (or other medical devices) units connected to a single Host unit. To establish synchronisation between transceivers, the Server emits a beacon. Upon detecting this beacon, the Client transceiver establishes an RF link.

13.1. Minimum Data Rate Requirements

Figure 27 below highlights the packet structure of data to be transmitted to the Host unit.

0xF0	Lead 1	Lead 2	0x0F	Checksum XOR

Figure 27: ECG Live! Packet structure

A total of 5 packet bytes plus a start byte of 255 must be transmitted prior to new data becoming available from the Analogue to Digital converter. Furthermore a "resend on error" capability must be employed to ensure reliable communication. The design only employs a single resend capability. Due to the robust protocol already implemented in the transceiver firmware this low-level protocol is deemed sufficient.

For single resend capability a total of 13 (12 packet bytes + 1 for Nack reception) bytes must be sent within prior to new data becoming available.

The total time to receive 2 data bytes from the ADC is 2ms. The filter iteration however requires 209µs to complete. This leaves

$$2\text{ms} - 209\mu\text{s} = 1.79\text{ ms}$$

for transmission of data. The resulting data rate is hence:

$$\text{Minimum Data Rate} = \frac{13 \times 8}{1.79ms} \approx 57900 \text{ bit/s}$$

The interface Data Rate is hence set to a maximum of 115200 bits/s. The R.F data rate however is fixed at 64Kbits/s

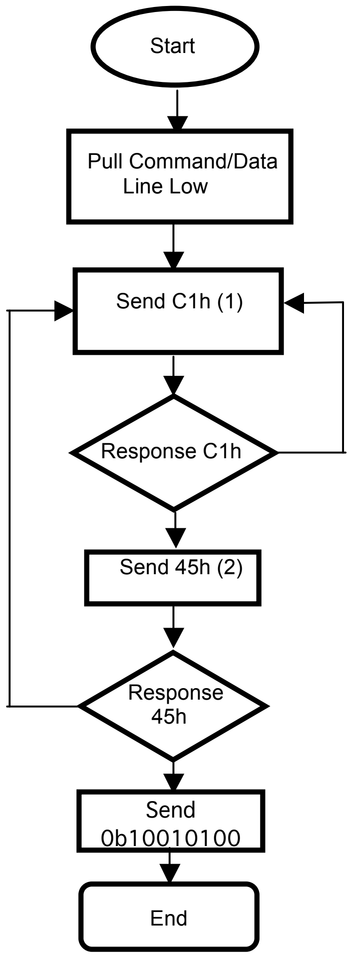
13.2. AC4486 Initialization

The transceiver is programmed by interfacing it to the P.C directly via a MAX232 I.C. The command/data pin on the transceiver is pulled low manually (connected to ground). A low level on the command/data pin allows configuration data to be written to the transceiver. The Brae terminal programme is used to send the configuration data bytes to the transceiver and view its response. Variable interface data rates may be configured in the transceiver. However the RF data throughput is constant.

The transceivers were configured with the following parameters:

- 8 data bits, 1 stop bit, No parity,
- Half Duplex operation
- Streaming Mode
- Interface Data rate of 115200 bits/s

Figure 28 below illustrates the process undertaken in programming the transceiver. The flow chart indicates the process undertaken in writing the necessary data to one of the configuration registers. The same process is undertaken when writing data to the second command register. All sent commands are sent manually using the Brae terminal programme. Two registers must be configured for operation Command0 and API control. The contents of the registers and there respective addresses are have been placed in the Appendices (C).



1. C1h command notifies transceiver that data is to be written. If the command is echoed back it has been received successfully by the transceiver.

2. EEPROM address that data is to be written to. (Command 0 register in this case)

3. Data written to address specified in (2) above

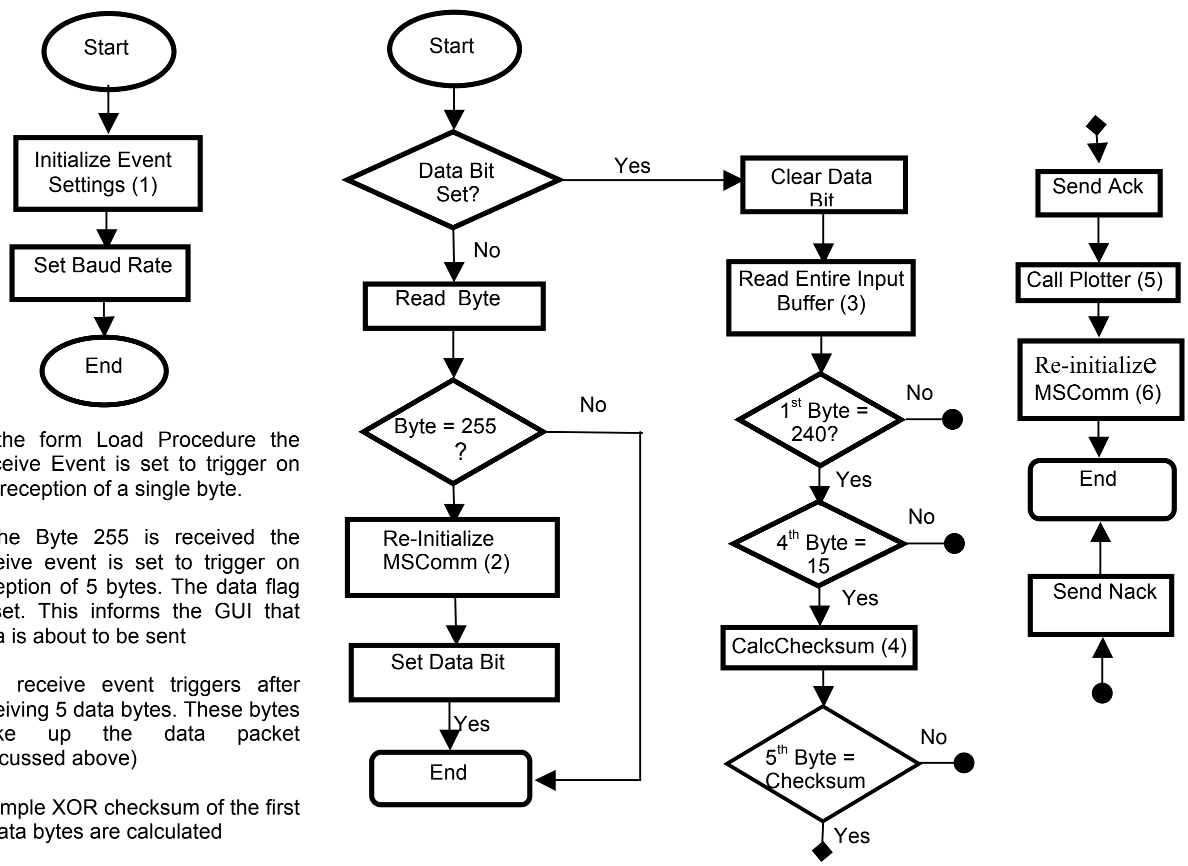
Figure 28: Programming Methodology of Wireless Transceiver

14. Visual Basic 6.0 Graphical User Interface (GUI)

A simple intuitive GUI is implemented for the display of the ECG data. The GUI is implemented using visual basic 6.0 Enterprise Edition.

14.1. MSComm Control

The MSComm ActiveX control is used to communicate between the Host Unit via USB and The P.C. The figure 29 illustrates the communication process between the Host and the GUI.



1. In the form Load Procedure the Receive Event is set to trigger on the reception of a single byte.
2. If the Byte 255 is received the receive event is set to trigger on reception of 5 bytes. The data flag is set. This informs the GUI that data is about to be sent
3. The receive event triggers after receiving 5 data bytes. These bytes make up the data packet (discussed above)
4. A simple XOR checksum of the first 4 Data bytes are calculated
5. Data is then Passed to Plotter Function (and Stored to a database) depending on user requirements.
6. MSComm is reinitialized to trigger on 1 Byte. It waits for 255

Figure 29: MSComm Communication Protocol

14.1.1 Com Port Settings

As mentioned previously the FT232RL driver creates a virtual Com Port. The port number however is dependant on the USB port selected. The initial idea was to automatically detect port selected by the user, however research into this showed that it is rather complex as it involved compiling code that interfaced directly to the windows registry. Hence the user is required to check the port settings under the Windows Device Manager prior to connection. The settings tab in the GUI (Figure 30) allows the user to select the appropriate port.

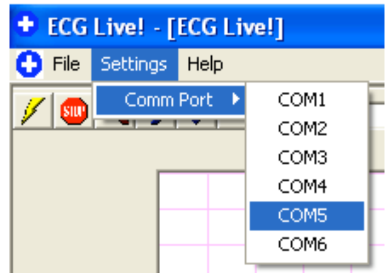


Figure 30: Com Port Settings Tab

14.2. GUI Functionality

The GUI employs a multiple form Interface (MDI). On start-up the parent form is loaded. An additional four forms (known as child forms) are linked to the parent form. The various possible options are highlighted in figure op below. Each option in the menu file with the exception of exit, loads one of the "child" forms. The exit option exits the application.

Figure 31: Parent Form menu file

14.2.1. Live Trace

The Live Trace option is utilised if no storage of ECG data into the Database is required. Each lead vector is plotted in its corresponding picture box no storage of data takes place. A toolbar was designed to provide the functionality present in most commercially available ECG products.

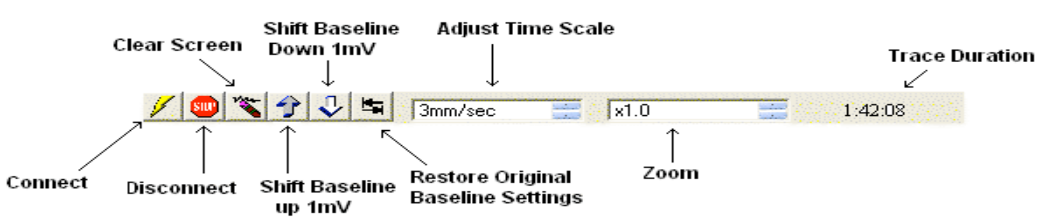


Figure 32: ECG Live! Toolbar Description

Functions	Descriptions
Connect	The connect icon connects the PC to the Host unit via the serial port
Disconnect	Close the connection between the Host Unit and P.C
Clear Screen	Erases all ECG data points plotted on the screen
Shift Baseline Commands	1mV represents a single block on the screen
Adjust Time Scale	Time scale is measured in terms of mm/sec. This was implemented to conform to general ECG standards
Zoom	Magnify Trace by selected amount
Trace Duration	Elapsed time since pressing the connect button

Table 6: Functional Description of ECG Live! Toolbar

14.2.2. Verification of GUI Parameters

Amplitude Settings

Typical ECG display software measures the signal in terms of mV. However the signal being transmitted is in the Volt range (amplified) and has been offset to accommodate the requirements of the DSPic. The signal is hence categorized manually by simultaneously displaying the raw ECG signal on an oscilloscope (output of differential amplifier) and plotting the filtered data on the GUI. The peak to peak voltage of the differential amplifier was measured (As the signal resembled that of figure 16). It is then divided by ten as the gain of the differential amplifier is set to ten. This value represented the peak to peak value of the ECG wave. The peak to peak value on the GUI in terms of millivolts is then set to be equal to the result on the scope. 3 different people were tested to verify and calibrate the result.

Time Scale Settings

A similar method is utilised in categorizing the time scale. The output of the DAC is connected to the oscilloscope while simultaneously viewing the Data on the GUI. A single division on the oscilloscope was measured to be 12.5 mm. The time/division was varied while measuring the time between successive peaks measured and calculating the mm/sec value. The distance between peaks was simultaneously measured on screen and the resultant time scale was calibrated.

Measured ECG using Live Trace

The following trace was obtained using the live trace functionality in the GUI. The time setting was set to 25mm/sec. Currently there exists a problem with the generation of the third lead. Due to the slight delay introduced by the digital filters the results are erroneous.

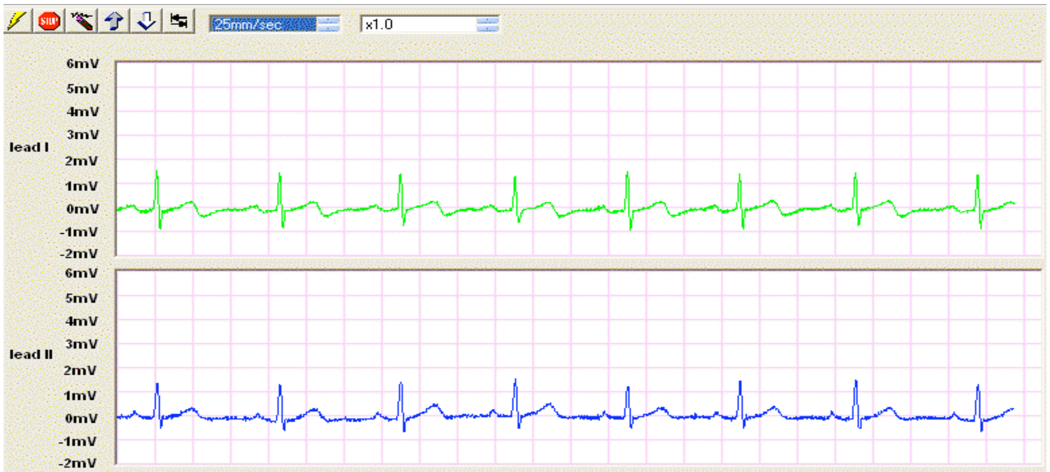


Figure 33: Real Time Data Display using ECG Live! And GUI

New Patient

Part of the specification of the design was to implement a database. Selection of the "New Patient" tab (figure 31) allows the user to add a new patient to the database. Figure 34 below illustrates the patient details form and each field that is stored in the relational database. On pressing the save button the live trace form is loaded and the ECG trace is displayed on pressing the connect button. The ECG data however in this case is stored together with its timestamp in the database and may be viewed at a later stage. Currently the New Patient Episode and Open Patient Episode forms are still under development

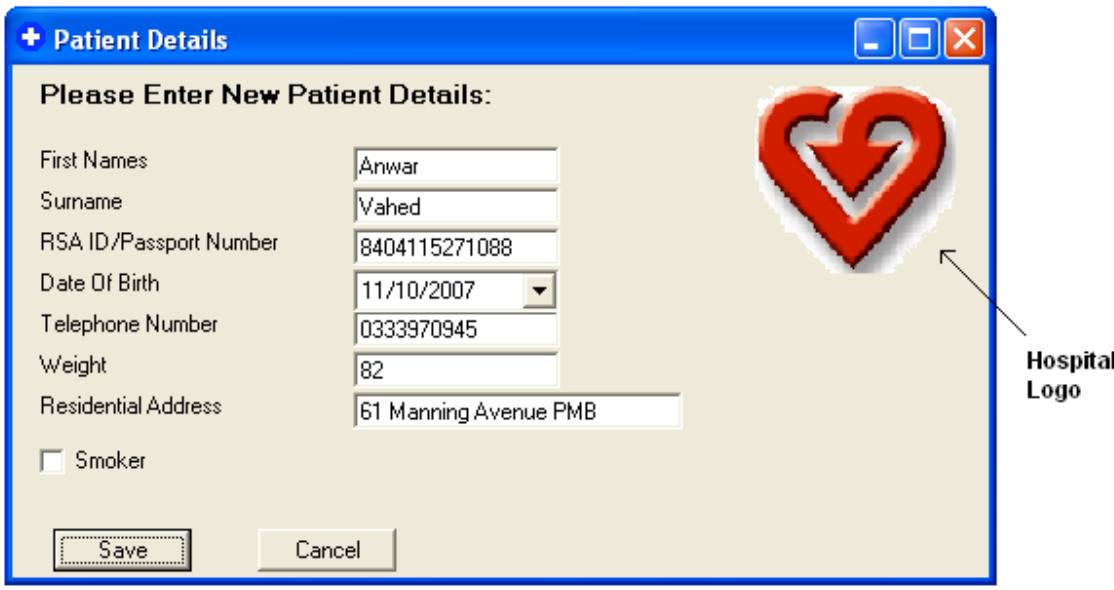


Figure 34: New patient Entry Form

15. ECG Live! Database System

A relational database was designed for the storage of ECG and patient data. The database implementation utilises the Microsoft ActiveX Data object component provided in the visual basic tool suite. The purpose of the relational database is to make available historical data in an attempt to improve the competence of patient record keeping. The database contains personal patient and timestamped ECG data.

The database structure was implemented using MS Access 2000. The database consists of 3 tables named patient, trace and ECGData. The Patient table (figure 35(a)) consists of 9 fields and stores the patient's personal details as illustrated in the figure below. The Patient_ID field is used as the primary key. The field is automatically incremented for each patient added to the database. This approach was selected as the primary key needed to be unique to each patient. The second table named Trace Contains Trace ID field. This field assigns a unique ID to each recorded ECG trace. Note1 and Note2 Fields were added so that the person viewing the trace (Such as a nurse) may add comments to be viewed at a later stage by the cardiologist who will be diagnosing the patient. Finally a third table was implement that stores the actual ECG data. A particular Trace ID is assigned the various data points that are stored. The index field is set as the primary key. Each set of data points (Lead I, II, III) are assigned a particular index. The 3 tables are illustrated in figure 35 below.

Patient : Table

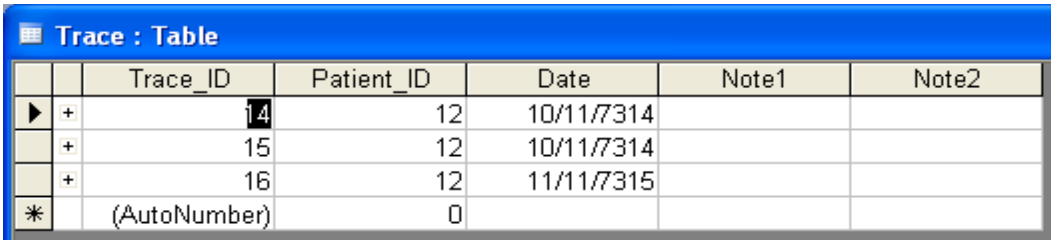
Surname	Name	RSA_ID	Patient_ID	DateOfBirth	TelephoneNumb	ResidentialAddr	Weight	Smoker
Vahed	Anwar	8404115271088	1	11/10/2007	0333970945	61 Manning Ave	82	☑
John	Smith	830321876123	2	3/21/1983	0312012567	90 Manning Roa	110	☐
Sipho	Dlamini	791206052489	3	6/12/1979	0115640921	3 Church Street	63	☑
			(AutoNumber)				0	☐

Figure 35(a): Patient Table: Stores Patients Personal Details

ECGData : Table

Trace_Id	index	Lead1	Lead2	Lead3
14	23029	64	64	0
14	23030	64	63	1
14	23031	63	63	0
14	23032	63	63	0
14	23033	64	63	1

Figure 35(b) Data Table: Stores ECG data



		Trace_ID	Patient_ID	Date	Note1	Note2
▶	+	14	12	10/11/7314		
	+	15	12	10/11/7314		
	+	16	12	11/11/7315		
*		(AutoNumber)	0			

Figure 35 (c): Trace table: Relates a Particular Patient ID to Trace Data

The relationship between the each of tables is illustrated in **Error! Reference source not found.**36. The *1* and ∞ (commonly referred to as one to many) symbols indicate that for each Patient ID in the patient table there exist an infinite number (possibly) of entries for that Patient ID in the data table.

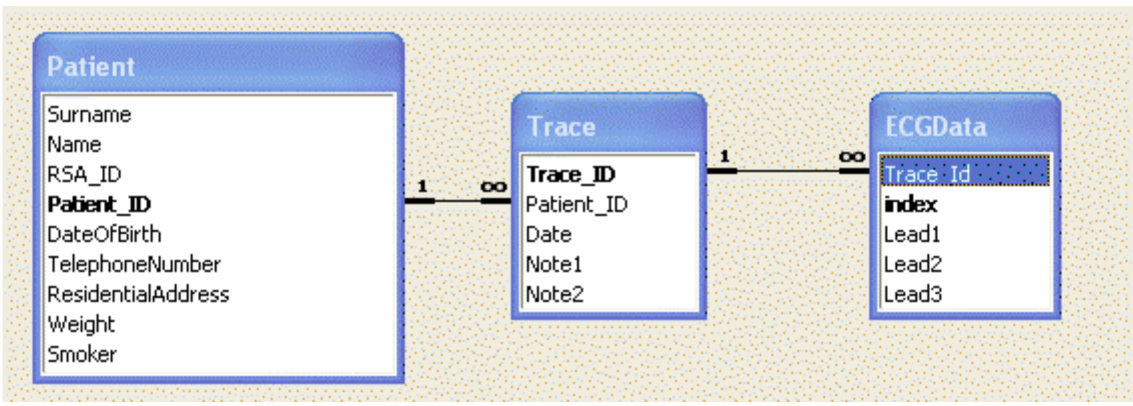


Figure 36: Database Tables and Relationships

The primary benefit of implementing such a database is the simplicity at which it may be adapted to meet the various user needs. For example a Physician/Doctor table can be created and a relation between doctors and patients formed. The database is accessed by the user through the GUI as discussed above.

16. System Enclosure (Mechanical Design)

The housings for both the mobile unit and the host unit are simply constructed metallic boxes. The main purpose of the housings is to protect the circuitry of both units from damage. Metallic boxes are used as this provides shielding to external noise.

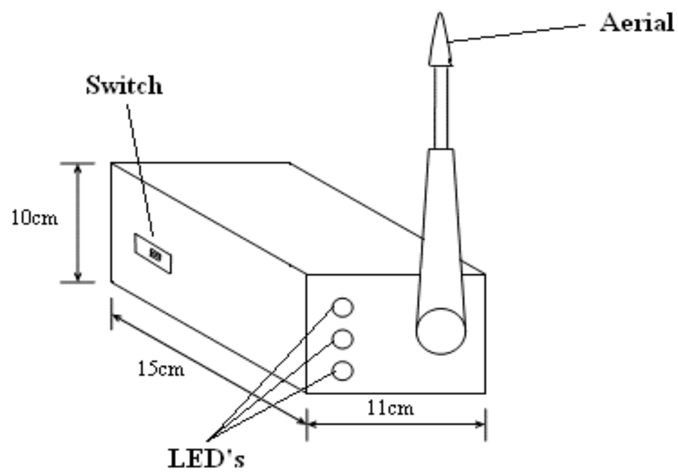


Figure 37(a): The Mobile Unit

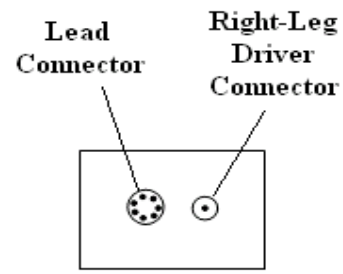


Figure 37(b): The Back View of the Mobile Unit

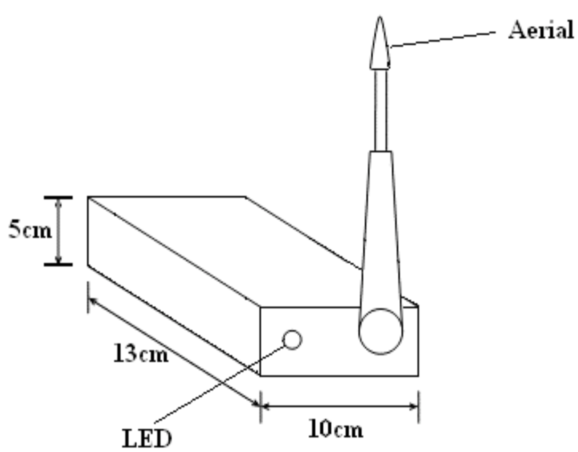


Figure 38(a): The Host Unit

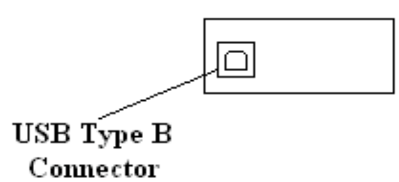


Figure 38(b): The Back View of the Host Unit

17. Conclusion

The design was successfully dissected into various modules. Each module with the exception of the database system has been implemented. The integration of the individual modules was achieved successfully.

All the results were categorically measured. A digital to analogue converter (DAC) was implemented into the design. The DAC was as a necessity for the proper measurement and categorization of measured results. It allowed the filtered ECG data to be viewed on an oscilloscope and necessary measurements to be taken.

The wireless transceiver proved to be an excellent choice. Initial teething problems were experienced during the implementation as the datasheet was not very well documented. Although slightly more challenging to implement than the Nordic options, the RF link is considerably more reliable. The device is also considerably more robust and may be repaired easily (personal experience). Most importantly however the data throughput figure outlined in the data sheet is realistic and achievable unlike many other RF products. A range of 30m was successfully achieved indoors.

All the GUI functionality discussed in the report is operational. The functionality was based on low cost ECG software used in hospitals in South Africa. The ECG trace however is very temperamental with respect to clarity. At times the trace is up to industry standard ECG machines. However, on occasion the signal is distorted slightly.

The storage of patient details and ECG data to the database has been implemented successfully, however loading the stored data proved to be a problem. Further investigation is under way.

18. References

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Appendix A

4th Order Low Pass Filter Design

$f_c = 250Hz$

i	**a$_i$**	**b$_i$**
1	1.8478	1
2	0.7654	1

Filter Section 1

$$C_2 \geq C_1 \frac{4b_1}{a_1^2}$$

Set $C_1 = 100nF$

$$C_2 \geq 100 \times 10^{-9} \frac{4}{(1.8478)^2}$$

$$C_2 \geq 117nF$$

Set $C_1 = 100nF$

$C_2 = 150nF$

$$R_1 = \frac{1.8478 \times 150 \times 10^{-9} - \sqrt{(1.8478)^2 (150 \times 10^{-9})^2 - 4 \times 100 \times 10^{-9} \times 150 \times 10^{-9}}}{4\pi \times 250 \times 100 \times 10^{-9} \times 150 \times 10^{-9}} = 3.129k\Omega \approx 3.3k\Omega$$

$$R_2 = \frac{1.8478 \times 150 \times 10^{-9} + \sqrt{(1.8478)^2 (150 \times 10^{-9})^2 - 4 \times 100 \times 10^{-9} \times 150 \times 10^{-9}}}{4\pi \times 250 \times 100 \times 10^{-9} \times 150 \times 10^{-9}} = 8.619k\Omega \approx 8.66k\Omega$$

Filter Section 2

Set $C_1 = 4.7nF$

$$C_2 \geq 4.7 \times 10^{-9} \frac{4}{(0.7654)^2}$$

$$C_2 \geq 33nF$$

Set $C_1 = 4.7nF$

$C_2 = 33nF$

$$R_1 = \frac{0.7654\times 33\times 10^{-9} - \sqrt{(0.7654)^2\left(33\times 10^{-9}\right)^2 - 4\times 4.7\times 10^{-9}\times 33\times 10^{-9}}}{4\pi\times 250\times 4.7\times 10^{-9}\times 33\times 10^{-9}} = 43.2k\Omega$$

$$R_2 = \frac{0.7654\times 33\times 10^{-9} + \sqrt{(0.7654)^2\left(33\times 10^{-9}\right)^2 - 4\times 4.7\times 10^{-9}\times 33\times 10^{-9}}}{4\pi\times 250\times 4.7\times 10^{-9}\times 33\times 10^{-9}} = 60.4k\Omega$$

Appendix B

A second-order analogue filter has a transfer function given by

$$H_a(s) = \frac{s^2 + \Omega_0^2}{s^2 + Bs + \Omega_0^2}. \qquad (16)^{[12]}$$

Its magnitude response is then

$$|H_a(j\Omega)| = \frac{\left|\Omega_0^2 - \Omega^2\right|}{\sqrt{\left(\Omega_0^2 - \Omega^2\right)^2 + B^2\Omega^2}}, \qquad (17)$$

which approaches unity values, i.e., a gain of 0dB, at $\Omega = 0$ and ∞. The magnitude has a zero value at the notch frequency $\Omega = \Omega_0$. If Ω_1 and Ω_2, $\Omega_2 > \Omega_1$, denote the frequencies at which the gain is down by -3dB, the 3-dB notch bandwidth defined by $(\Omega_2 - \Omega_1)$.

Applying the bilinear transformation to $H_a(s)$ of equation (16), we arrive at

$$\begin{aligned} G(z) &= H_a(s)\big|_{s=\left(1-z^{-1}\right)\left(1+z^{-1}\right)} \\ &= \frac{\left(1+\Omega_0^2\right) - 2\left(1-\Omega_0^2\right)z^{-1} + \left(1+\Omega_0^2\right)z^{-2}}{\left(1+\Omega_0^2+B\right) - 2\left(1-\Omega_0^2\right)z^{-1} + \left(1+\Omega_0^2-B\right)z^{-2}}, \end{aligned} \qquad (18)$$

which can be written as

$$G(z) = \frac{1}{2}\,\frac{(1+\alpha) - 2\beta(1+\alpha)z^{-1} + (1+\alpha)z^{-2}}{1 - \beta(1+\alpha)z^{-1} + \alpha z^{-2}}, \qquad (19)$$

where

$$\alpha = \frac{1+\Omega_0^2 - B}{1+\Omega_0^2 + B}, \qquad (20a)$$

$$\beta = \frac{1-\Omega_0^2}{1+\Omega_0^2}, \qquad (20b)$$

The notch frequency ω_0 and the 3-dB notch bandwidth B_ω of the digital notch filter of equation (19) are related to the constants α and β through

$$\alpha = \frac{1-\tan(B_\omega/2)}{1+\tan(B_\omega/2)}, \qquad (21a)$$

$$\beta = \cos\omega_0 \qquad (21b)$$

Equations (21a) and (21b) are the desired design formulas to determine the constants α and β for a given notch frequency ω_0 and a 3-dB notch bandwidth B_ω.

Appendix C

Aerocomm AC4486 wireless transceiver Configuration registers

Parameter	EEPROM Address	Length (Bytes)	Range	Default	Description
Control 0	45h	1		10010100b (94h)	Settings are: Bit 7 – One Beacon Mode 0 = Beacon every hop 1 = Beacon once per hop cycle Bit 6 – DES Enable 0 = Disable Encryption 1 = Enable Data Encryption Bit 5 – Sync to Channel 0 = Don't Sync to Channel 1 = Sync to Channel **Bit 4 – AeroComm Use Only** **Bit 3 – AeroComm Use Only** Bit 2 – RF Mode 0 = RF Stream Mode 1 = RF Acknowledge Mode Bit 1 – RF Delivery 0 = Addressed 1 = Broadcast **Bit 0 – AeroComm Use Only**
Frequency Offset	46h	1	0 – FFh	01h	Protocol parameter used in conjunction with Channel Number.
Transmit Retries	4Ch	1	1 – FFh	10h	Maximum number of times a packet is sent out in Addressed Acknowledge mode.
Broadcast Attempts	4Dh	1	1 – FFh	04h	Number of times a packet is sent out in Broadcast Acknowledge mode.
API Control	56h	1		01000011b (43h)	Settings are: **Bit 7 – AeroComm Use Only** **Bit 6 – AeroComm Use Only** Bit 5 – Unicast Only 0 = Receive Addressed and Broadcast packets 1 = Only receive Addressed packets Bit 4 – Auto Destination 0 = Use Destination Address 1 = Automatically set Destination to Server **Bit 3 – AeroComm Use Only** Bit 2 – RTS Enable 0 = RTS Ignored 1 = Transceiver obeys RTS Bit 1 – Duplex Mode 0 = Half Duplex 1 = Full Duplex Bit 0 – Auto Config 0 = Use EEPROM values 1 = Auto Configure Values
Interface Timeout	58h	1	2 – FFh	04h	Specifies a byte gap timeout, used in conjunction with RF Packet Size, to determine when a packet is complete (0.5ms per increment).
Sync Channel	5Ah	1	0 – 3Fh	01h	Used to synchronize the hopping of collocated

Appendix D

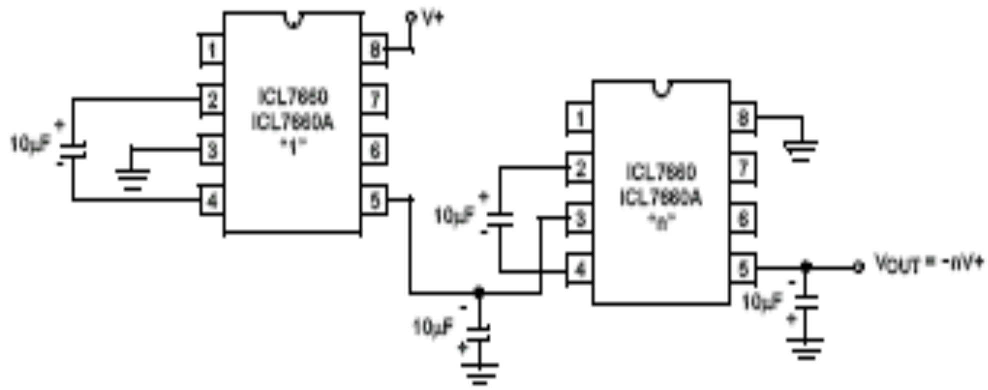

Figure D-1: ICL7660 Schematic [19]

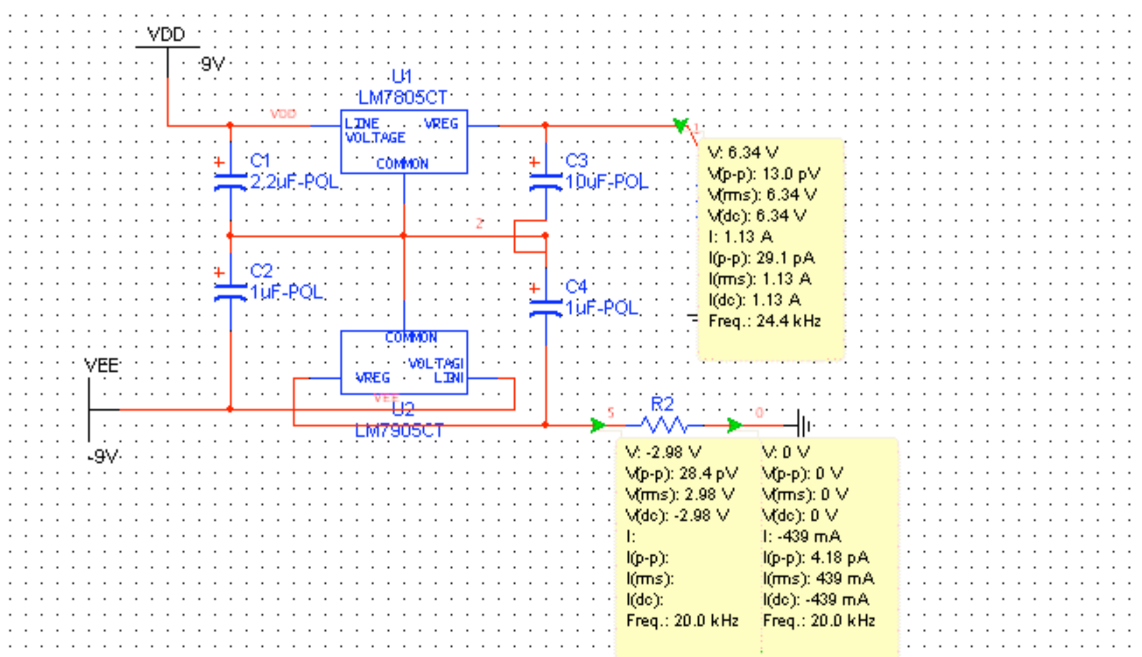

Figure D-2: Simulated Power Supply