Cardless Security System

88-400-01: CAPSTONE DESIGN PROJECT

PROGRESS REPORT

JANUARY TO APRIL 2018

Department of Computer and Electrical Engineering

Attention to
Dr. Arezoo EMADI and Dr. Mitra MIRHASSANI

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CONTENTS

Cardless Security System

Robert Goleberski, *Student Member, IEEE,* Zuwei Li, *Student Member, IEEE,*
and Matthew Santos, *Student Member, IEEE*

I. Progress Summary

At this time the project has reached the halfway mark and although significant progress has been made, presently development is approximately two weeks behind schedule. The need to perform several design iterations has pushed part selection back. In order to reconcile lost time and prevent further delay an increased effort from the group members is required. A new schedule has been drafted with a tighter timeline which still reserves the month of July for testing. Presently the design of nearly all electric circuit sub-components is complete however part selection of in some areas is still underway and will need to be completed as soon as possible. Design of the biometric algorithm is also complete and has been shown to produce 94% accuracy. Implementation of this algorithm into microprocessor code is still ongoing and will likely be conducted alongside breadboard testing to aid in debugging.

II. Introduction

The purpose of this report is to outline the current state of progression on the cardless security system capstone project, describe the work remaining and present an updated schedule. This report covers the period of time between initial selection of the project in January up until May 5th 2018 which represents roughly half of the allocated project timeframe. During this time design on various aspects have been completed and the transition towards selecting parts for a physical implementation is underway. Prior to the discussion on development situation, the following brief synopsis of the project and its associated design objectives is provided in order to provide context and reiterate expectations.

A. Project Description

The project entails the development of a cardless security system focused on electrocardiogram (ECG) biometrics which is capable of uniquely identifying an individual in order to discern their level of access. Regulation of this access is to be conducted using a secure mechanical locking system operated by a direct current motor. Additional features are to be included in order to further increase security and prevent unauthorized entry. The device is expected to be an embedded solution powered by batteries with audio and visual indicators used to denote various system states.

B. Project Design Objectives

1) Differentiate between individuals based on electrocardiogram signals
2) Develop a secure mechanical locking system driven by an electric motor

III. Work Completed

Development has been separated into three main sub-projects. These sub-projects include the analog front end, the microprocessor, and the power system. In order to facilitate perception of progress a block diagram illustrating these sub-projects and their composition is presented in Figure 1. The subsequent sections are used to summarize the current status of these three areas.

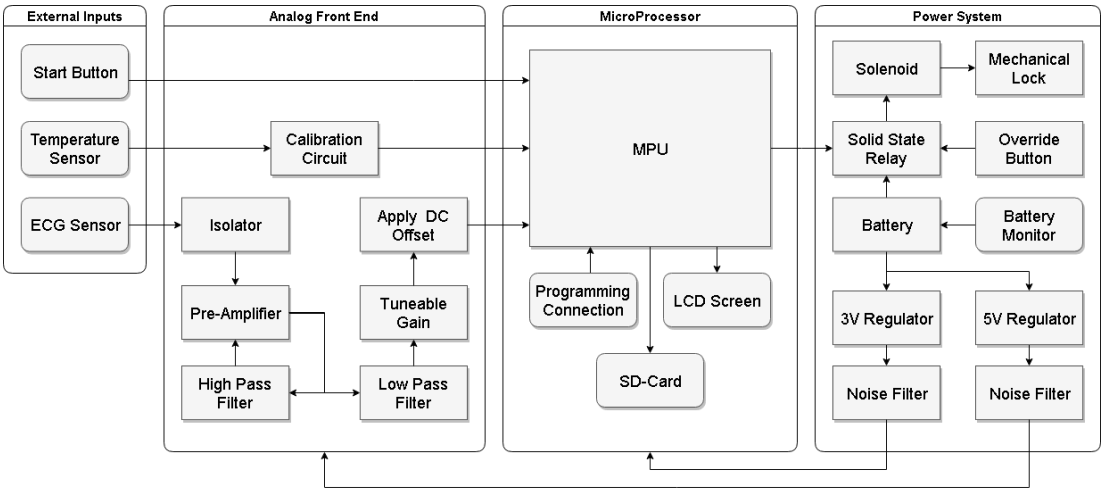


Fig. 1. Overall Design Block Diagram

A. Analog Front End

This sub-project is responsible for providing the interface to and refinement of the real world signals before directing them to the microcontroller for acquisition and processing. At present the design and simulation of the ECG line to the microprocessor has been completed although part selection is still being conducted. The necessary theory required for the temperature sensor calibration circuit has been completed but its final design values are subject to sensor selection which is also ongoing.

As the measurement of real signals is always accompanied by noise preliminary analog filters were strategically implemented in order extract clear ECG signals. At present the analog ECG processing consists of an instrumentation amplifier which is used for its low noise gain and isolation. A first order high-pass filter configured to provide reference feedback to the instrumental amplifier for low frequency noise removal and lastly a pair of 2nd order low-pass filters which have been preset to a cutoff frequency of 100Hz. Simulation of this configuration has demonstrated excellent results as seen in Figure 2 which illustrates the frequency response of the ECG front end. From the figure it is clearly seen that the region of interest from 500mHz to 100Hz experiences an undistorted gain of approximately 20dB with first order falloff to the left and second order to the right.

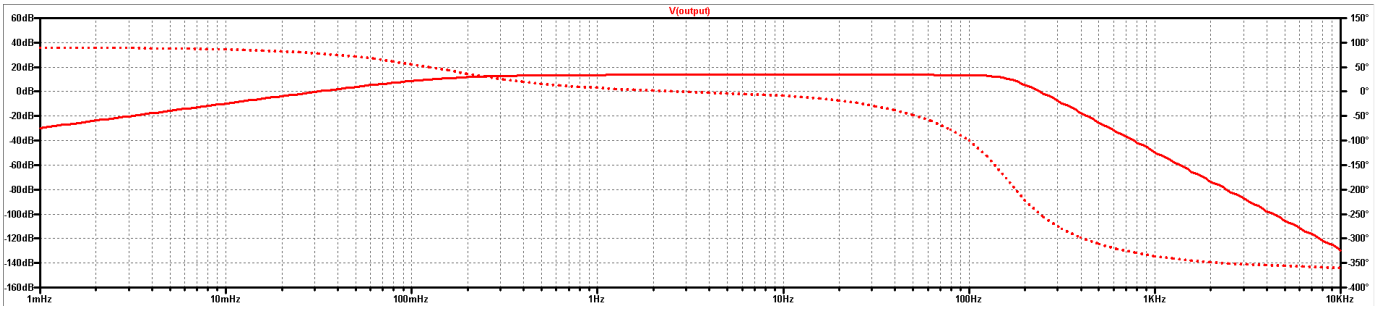
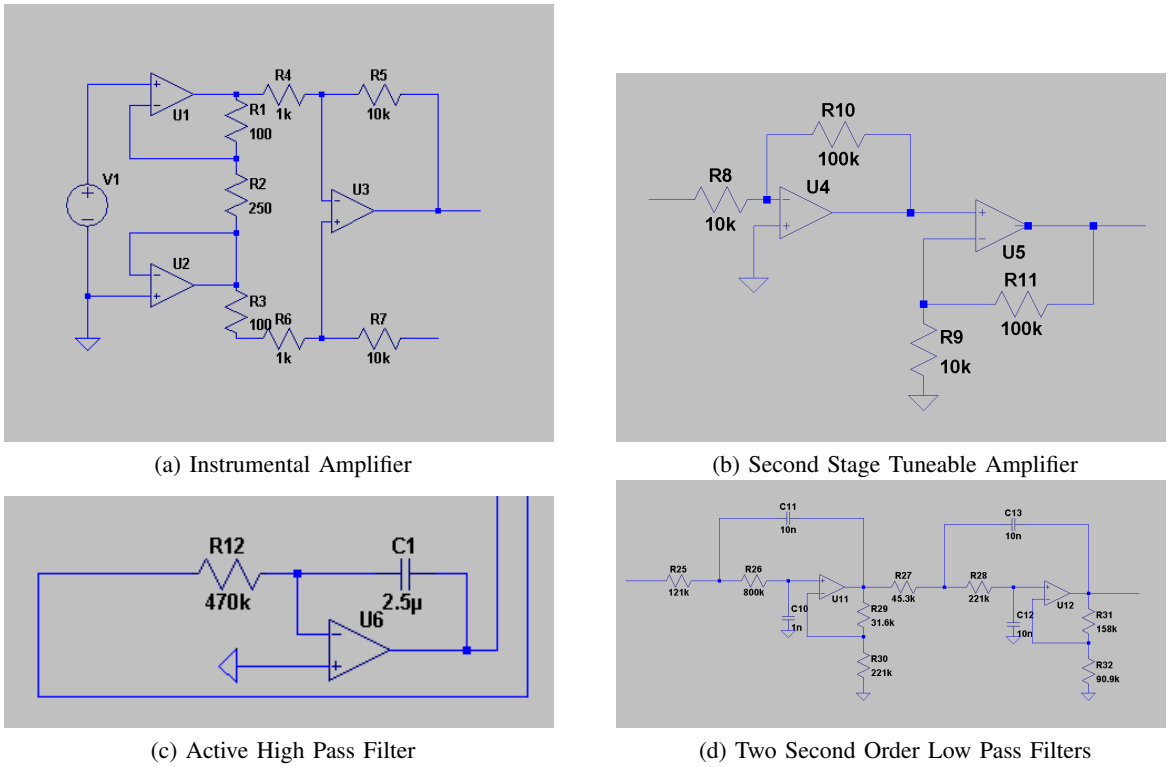


Fig. 2. Analog ECG Frequency Response

Additional consideration was placed into correctly positioning the ECG output signal in the 0V to 3.3V region required by the microcontroller's analog to digital converter. This was done by utilizing a potentiometer tuneable secondary gain stage which also serves to apply the required DC offset. These front end components are individually presented in Figure 3 with the complete design illustrated in Appendix B.



(a) Instrumental Amplifier

(b) Second Stage Tuneable Amplifier

(c) Active High Pass Filter

(d) Two Second Order Low Pass Filters

Fig. 3. Analog Front End Components

B. Microprocessor

A large majority of the assessment period was dedicated to the design and refinement of the biometric algorithm responsible for distinguishing an individual heart signal. A complete overview of the algorithm at present is illustrated in Figure 4. The computation consists of filtering the ECG signal using a series of digital filters followed by a custom feature extraction procedure which generates the primary test vector.

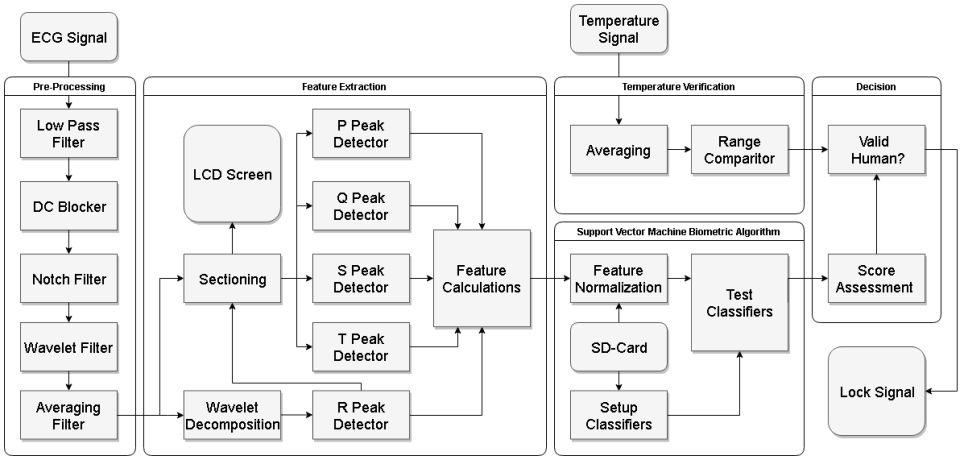


Fig. 4. Microprocessor Biometric Check Procedure

A support vector machine based classifier was employed as it offered more flexibility and was also more intuitive. As predicted while the application of support vectors was straight forward the amount of processing required to form said vectors exceeded the capabilities of most conventional microprocessors. Thus offloading of this task was required and the procedure for doing so takes advantage of the micro-SD card for the transfer medium as illustrated in Figure 5.

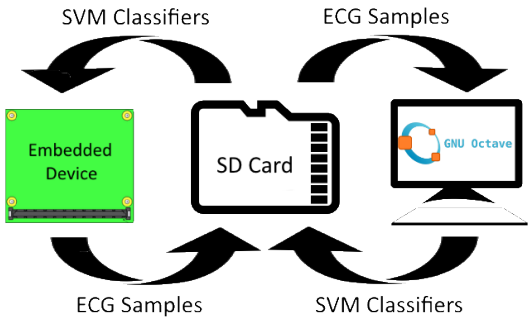


Fig. 5. Data Transfer Concept

At this time design of the algorithm itself is considered to be complete. It utilizes a total of 27 features to employ a one versus rest assessment on each individual included in the database taking advantage of the radial basis function kernel for separation. Utilizing a public collection of prerecorded ECGs the algorithm was extensively tested in computer simulations and successfully distinguished 47 out of the 50 individuals included in the database while also refusing an additional 10 who were not. Thus at present the success rate is estimated to be 94% with no false positives. In order to provide additional insight into the level of accuracy two additional figures are included in Appendix C which illustrate feature distinguishability levels and the capability of the radial basis function to isolate particular individuals across two features.

Following algorithm design the dsPIC33FJ128GP802 by Microchip was selected to be the central processor for this project for its low cost and built in digital signal processing enhancements which allow for bulk multiplication and addition operations. The completed microprocessor and peripheral schematic is illustrated in Appendix D along with several notes on layout considerations. Based of rough calculations it is estimated that utilizing this microcontroller with a sampling time of 20 seconds and a database consisting of 50 people the assessment can be completed in five minutes. While reduction of this duration is possible it would require either a reduction in database capacity or identification accuracy.

C. Power Distribution and Lock System

The first issue confronted in this part of the project was powering the microprocessor. The supply line to power the selected microprocessor required a stable voltage of 3.3V with a peak current of 200mA. This was easily obtained with a simple buck-converter and power generated through D type batteries which were selected for their high ampere hour rating. A battery monitoring circuit was designed utilizing different colour light emitting diodes (LEDs) to indicate the energy level remaining. The monitor itself is to be push button activated in order to further conserve power.

The next task was designing the control for the lock. Initial design plans utilized a solenoid that would lock a strike keeping the door closed. The idea being once the signal from the microcontroller was applied a relay would activate the solenoid and the door could be opened. This was deemed too simple and so instead a deadbolt mechanism was proposed. In order to control the deadbolt a motor is to be utilized. It will be controlled using pulse width modulation coming from the microprocessor. The motor will either be a servo motor which can be controlled simply by PWM or a DC motor that would require a motor driver component. In addition there will also be a magnetic reed switch installed on the door and connected to the microprocessor to aid with positioning control of the deadbolt. In order to open the lock from inside

a push-button connected to the microprocessor will be used to inform the processor to move the open the door. At this time the circuit design has been completed and roughly half of the required parts have been selected. A complete overview of the power system is presented in Appendix E. Physical testing of the battery monitor circuit was performed using remnants of an older project and was shown to behave as expected.

IV. Work Scheduled

Progress has been made on the bulk of the design task but several sections still require additional work before implementation can begin. For the analog front end the sensors need to be selected along with the remainder of components and the calibration circuit for the temperature sensor suitably updated. Similarly the remainder of the components required for the power system must be chosen and additional consideration must be placed into the design of the mechanical locking mechanism and power line to the analog front end. At this time while the biometric algorithm has been designed it still needs to be integrated into microprocessor code and progress on this front is still ongoing.

Following the completion of the aforementioned tasks the procurement of the required parts can begin and breadboard testing of the various sub-sections started. Following successful verification a complete printed circuit board layout is to be generated and the final product constructed.

V. Outstanding Issues

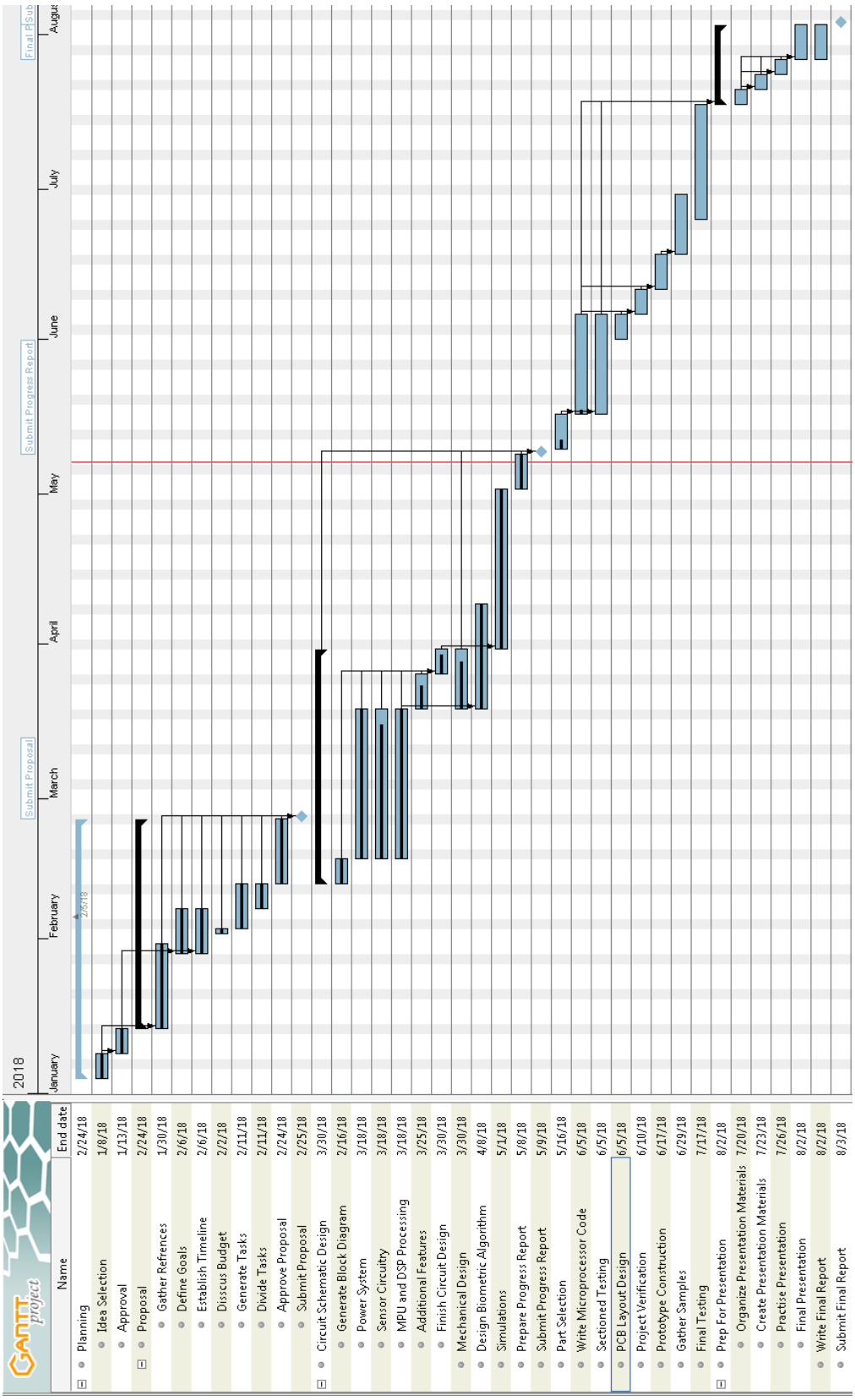
Although algorithm tests thus far have made use of public ECG signals said data was gathered using a different apparatus and thus will likely exhibit discrepancies from the utilized setup. This would lead to increased error in support vector classifications and could produce erroneous results. The creation of a database obtained utilizing the device itself would serve to eliminate this problem however this is not a trivial affair. As the sampling of student information that could be considered personally identifying raises ethical concerns the Research and Ethics Board (REB) on campus was contacted and consulted about how to handle the situation. An insight into the acceptable methods for gathering research data was achieved and steps are being taken to obtain REB approval. The process is lengthy and will require some level of assistance from the project supervisor. In addition permission will need to be sought out for the sending of a departmental email requesting willing participants in an independent manner. The goal is to have collected all the information needed to submit a proposal to the REB by the middle of May after which it is expected to have sanctioned sampling begin in mid June.

VI. Schedule Changes

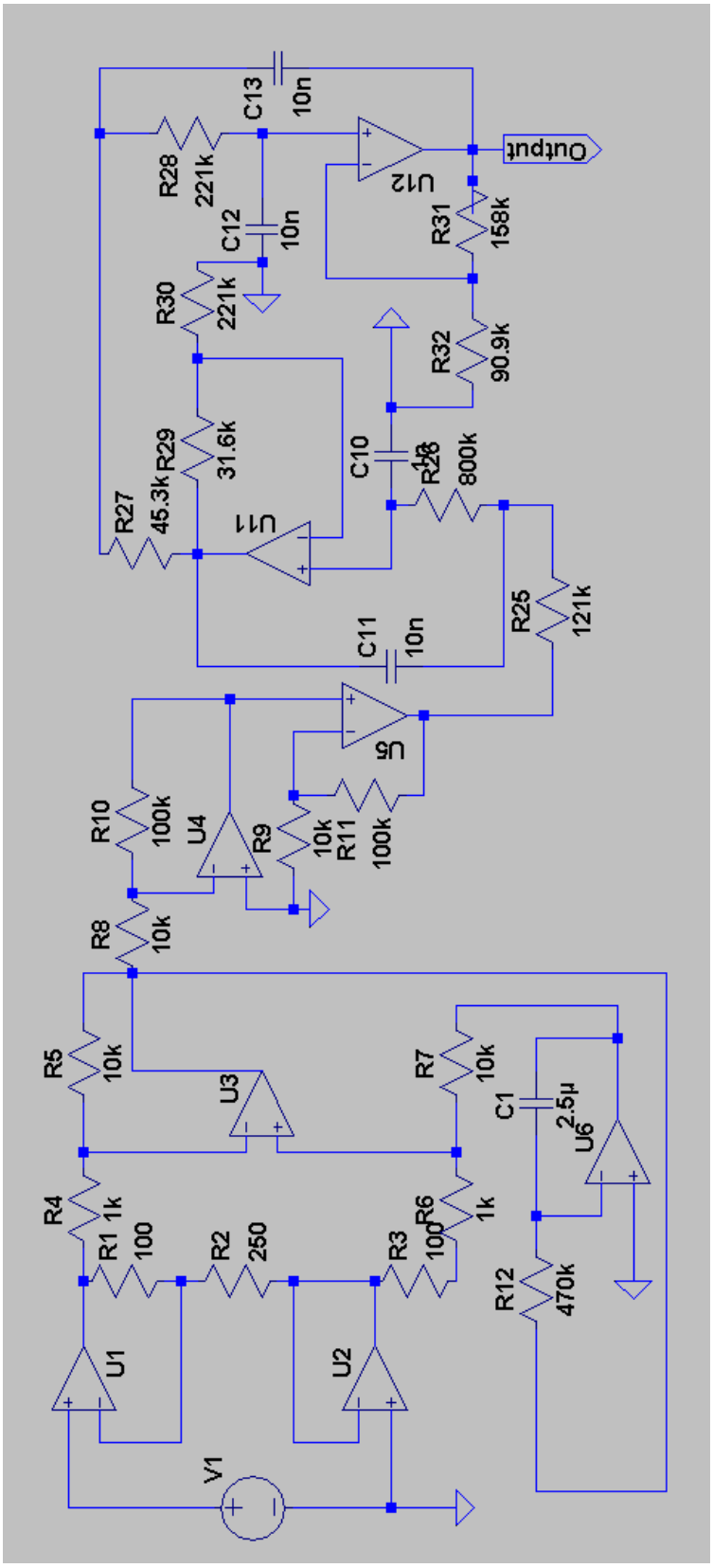
Modifications to the proposed schedule were required in order to allocate additional time for revising the initial designs and performing part selection. A revised schedule is proposed and is presented in Appendix A illustrating the current level of progress and restructuring past tasks to more closely resemble work done. In addition a new section dedicated to the breadboard testing of individual sub-projects prior to prototype assembly was added. Through the addition of this section it is hoped that any design issues can be eliminated prior to pcb manufacturing.

The primary goal of completing the overall prototype before the start of July remains unaltered, thus continuing to reserve a whole month of time for troubleshooting and testing.

APPENDIX A
REVISED PROJECT SCHEDULE



APPENDIX B
ECG ANALOG FRONT END SCHEMATIC



APPENDIX C
BIOMETRIC ALGORITHM TEST

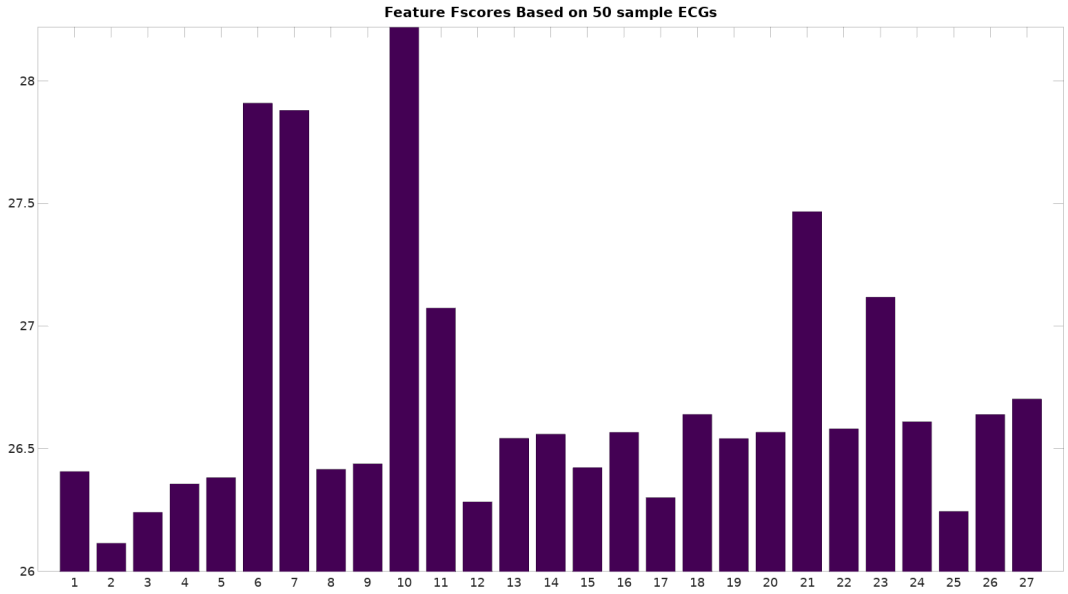


Fig. 6. Relative Feature Distinguishability through Fscore

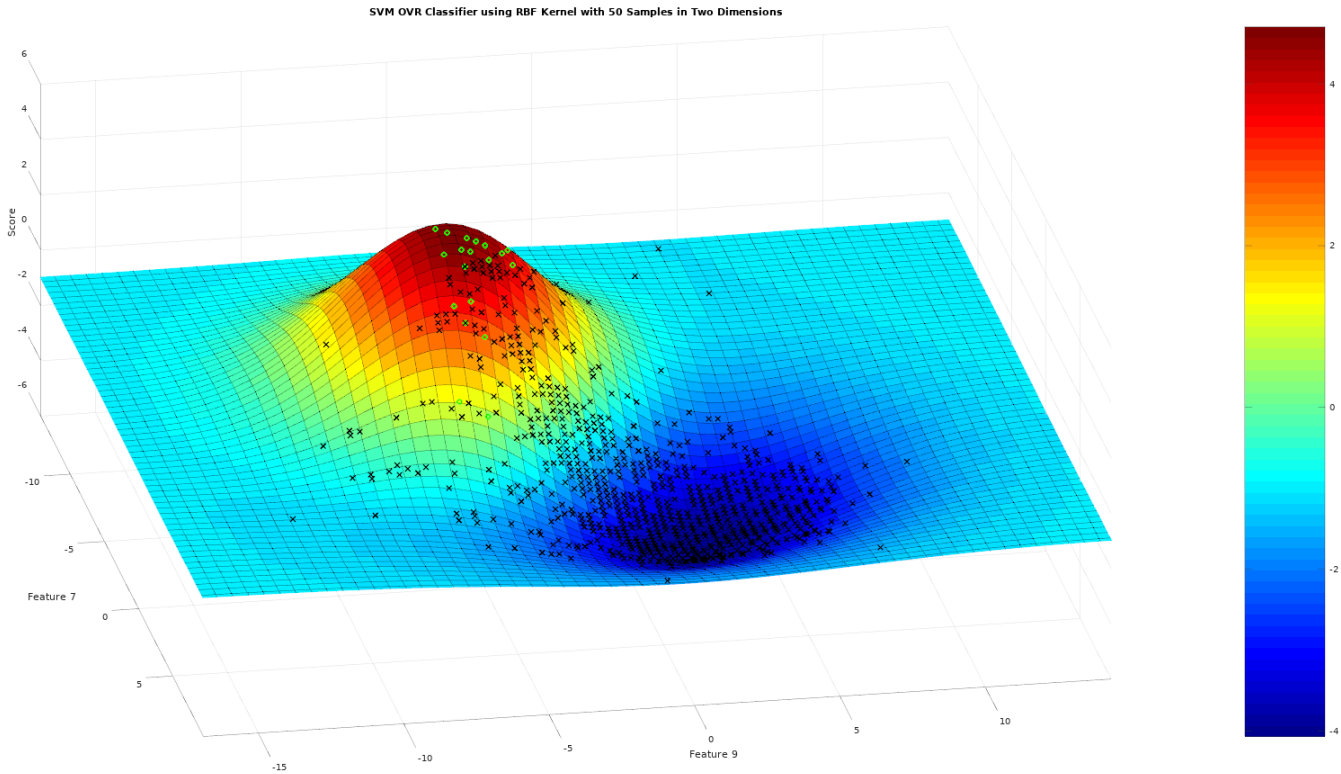
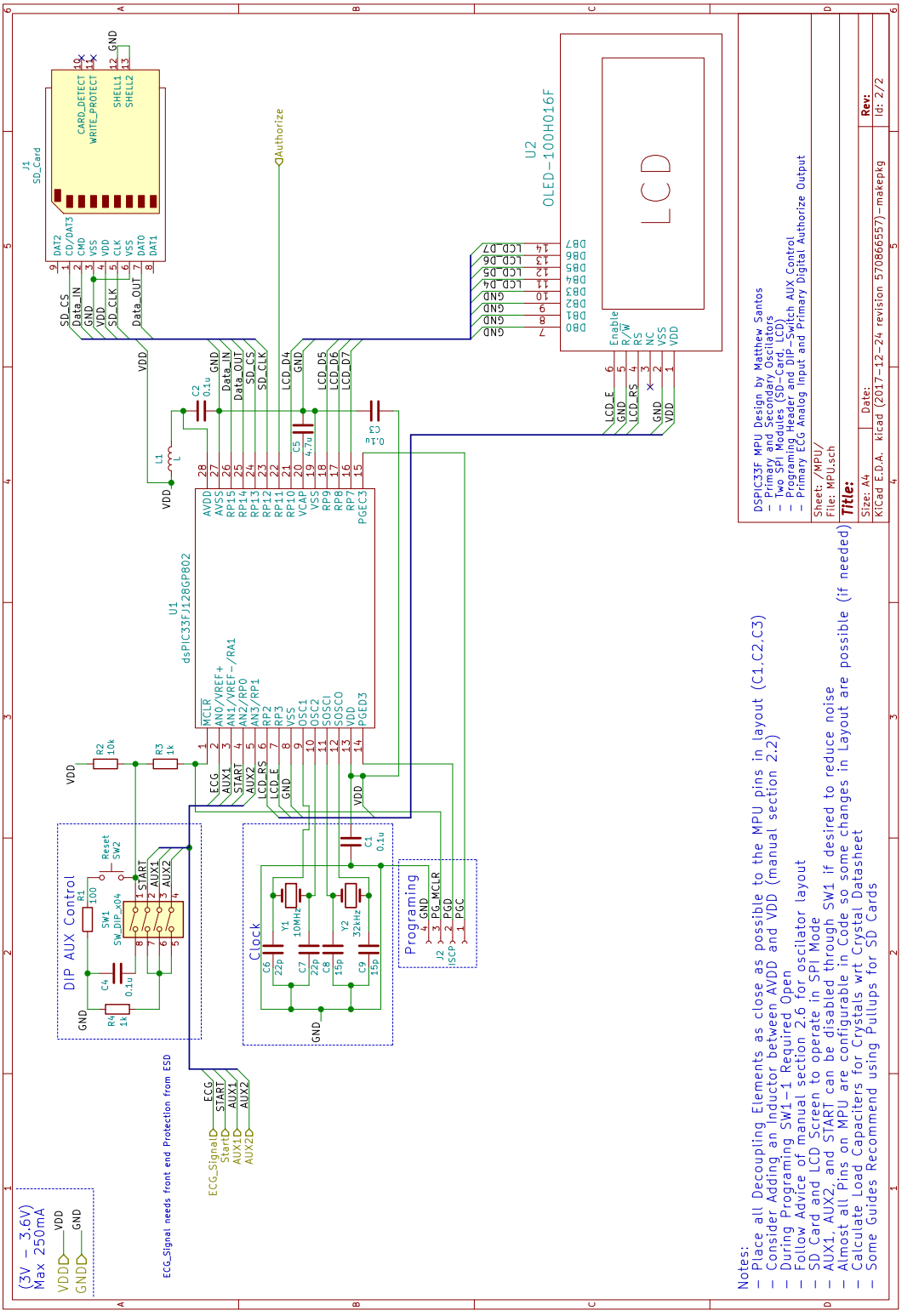


Fig. 7. Two Dimensional Feature Classification Example

APPENDIX D
MICROPROCESSOR SCHEMATIC



APPENDIX E
POWER SYSTEM SCHEMATIC