A Configurable Sawtooth Based PWM Generator with 2 ns On-Time for >50 MHz DCDC Converters

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***Abstract*—Size and cost of a switched mode power supply can be reduced by increasing the switching frequency. The maximum switching frequency and the maximum conversion ratio are limited by the duty cycle of a PWM signal. In DCDC converters, a sawtooth generator is the fundamental circuit block to generate the PWM signal. The presented PWM generator is based on two parallel, fully interleaved PWM generator stages, each containing an integrator based sawtooth generator and two 3-stage high-speed comparators. A digital multiplexing of the PWM signals of each stage eliminates the dependency of the minimum on-time on the large reset times of the sawtooth ramps. A separation of the references of the PWM comparators in both stage allows to configure the PWM generator for a DCDC converter operating in fixed frequency or in constant on-time mode, which requires an operation in a wide frequency range. The PWM generator was fabricated in an 180 nm HV BiCMOS technology, as part of a DCDC converter. Measurements confirm minimum possible on-time pulses as short as 2 ns and thus allows switching frequencies of DCDC converters of >50 MHz at small duty cycle of <10%. At moderate duty cycles switching frequencies up to 100 MHz are possible.**

I. Introduction

The increasing complexity of electrical systems requires a continuous reduction of system size and cost. For power management, switched mode power supplies are utilized to achieve high power density with a high conversion efficiency. They require filter components like inductors and capacitors, which mainly dominate the cost and converter size. Applications like IT servers, battery driven applications in e-mobility vehicles or power tools have a DC supply in the range of 12 V up to 70 V and higher. To supply micro-controllers or low voltage control circuits, the supply voltage has to be converted into a low DC voltage in the range of 0.5 V to 5 V. Consequently, the converter has to support a large conversion ratio.

A. Fast Switching DCDC Converters

A typical implementation of a DCDC converter as synchronous buck converter is shown in Fig. 1a [1]. A low-side power FET and an inversely controlled high-side FET (MNHS and MNLS) are generating a pulsed input voltage at the switching node VSW, which is filtered by L_0 and C_0 to obtain a lower DC output voltage. While the low-side FET MNLS is directly controlled by the signal $CTRL_{LS}$ on the low-side domain, the control signal for the high-side FET $CTRL_{HS}$ is shifted to a high-voltage domain by a level shifter, since the gate driver is referenced to the switching node VSW.

Fig. 1b shows the simplified schematic of the control part of the converter, known as voltage mode control (VMC). An error amplifier generates the resulting error signal $VERR$ of

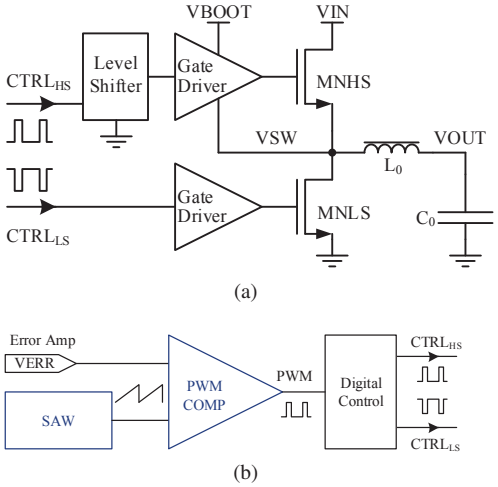

Fig. 1. a) Synchronous buck converter architecture; b) PWM generation and regulation concept of the converter.

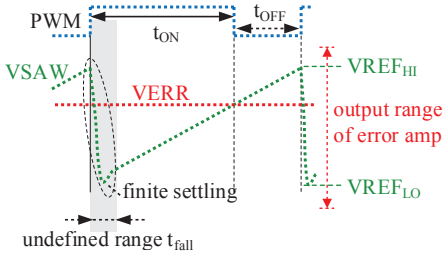

Fig. 2. PWM generation based on a conventional sawtooth signal.

$VOUT$ with respect to a reference voltage. $VERR$ is compared to a sawtooth signal by a comparator (PWM COMP). Its output is a pulse width modulated (PWM) signal, which controls the on- and off-times of the power FETs and thus the transferred energy towards $VOUT$. Converters are often locally implemented at the point of load and require a high level of integration. This can be achieved by increasing the switching frequency [2], [3] as it scales down the passive components, but the switching frequency is limited by the decreasing efficiency, especially at high input voltages. Besides the level shifter [4] the sawtooth generator limits the maximum operating frequency and the conversion ratio, respectively. Hence, it belongs to the fundamental building blocks in DCDC converters [5] and is the focus of this paper. One way to circumvent the efficiency drawback of hard-switching topologies at large switching frequencies is to apply soft-switching techniques, which are often PWM controlled and thus also require a precise on-time control.

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B. Requirements for Sawtooth and PWM Generator

The output $VOUT$ of a conventional buck converter, as shown in Fig. 1, is adjusted by the duty cycle D of the PWM signal of the converter. It is calculated as $D = VOUT/VIN = t_{ON}/(t_{ON} + t_{OFF})$, with the input voltage VIN and the on- and off- time of the PWM signal (t_{ON} and t_{OFF}), Fig. 2. The switching frequency is determined by $f_{SW} = 1/(t_{ON} + t_{OFF})$. A conversion from $VIN = 12$ V to $VOUT = 1.2$ V, which is typical e.g. in IT server or automotive applications, require a minimum duty cycle of $D \leq 0.1$. This corresponds to a minimum pulse width of $t_{ON} < 10$ ns at a switching frequency of 10 MHz and $t_{ON} < 2$ ns at 50 MHz. The sawtooth ramps are started at a voltage $VREF_{LO}$ which is above the minimum output voltage of the error amplifier, while the maximum ramp voltage $VREF_{HI}$ is below the maximum output voltage of the amplifier (Fig. 2). Thus, the error signal $VERR$ can fall below and rise above the signal range of the sawtooth ramps, which allows a duty cycle range from 0 % to 100 %. The minimum on-time limits either the maximum conversion ratio or the switching frequency.

The minimum duty cycle is further limited by the falling slope of the sawtooth signal. As shown in Fig. 2, the ramp of the sawtooth signal is typically reset at the rising edge of the PWM. This requires a finite settling time t_{fall} of the rising slope. Thus, the minimum pulse width of the PWM signal has to be limited to $t_{ON} > t_{fall}$ as the input signal of the PWM comparator is not valid during t_{fall} and the PWM signal cannot be set low correctly.

As the timing requirements are difficult to fulfill by the control circuits, the converter can be switched to constant on-time mode [6]. The on-time is kept constant at a feasible value, e.g. 5 ns, while the off-time is adjusted, to regulate the output voltage. The drawback is a widely varying switching frequency from the operating frequency down to a few MHz.

Converters suitable for input voltages as large as 50 V and above require a high-voltage technology for the power stage. These technologies are typically not optimized for speed and high bandwidth. Even low-voltage transistors have moderate bandwidths in the range of 1 GHz and limit the speed of analog circuits to the nano-second range.

While level shifters and gate drivers can propagate on-time pulses of less than 3 ns [4], a sawtooth generator is required which is suitable for PWM signals with on-time pulses in the same range. Therefore, the focus of this paper is on sawtooth generatation for PWM signals with on-time pulses of < 2 ns, suitable for both constant frequency or constant on-time operation.

II. Limitations of Conventional Sawtooth Generators

Conventional concepts to generate sawtooth signals are shown in Fig. 3 [1], [7], [8]. Figure 3a shows a concept in which a linear regulator generates the lower sawtooth level $VREF_{LO}$. A switch connects a capacitor to $VREF_{LO}$. A constant reference current $ISAW$ is charging up the capacitance and thus generates the sawtooth ramp. A comparator detects, when the ramp reaches the upper level $VREF_{HI}$ and the ramp is reset again to $VREF_{LO}$ by turning on the switch

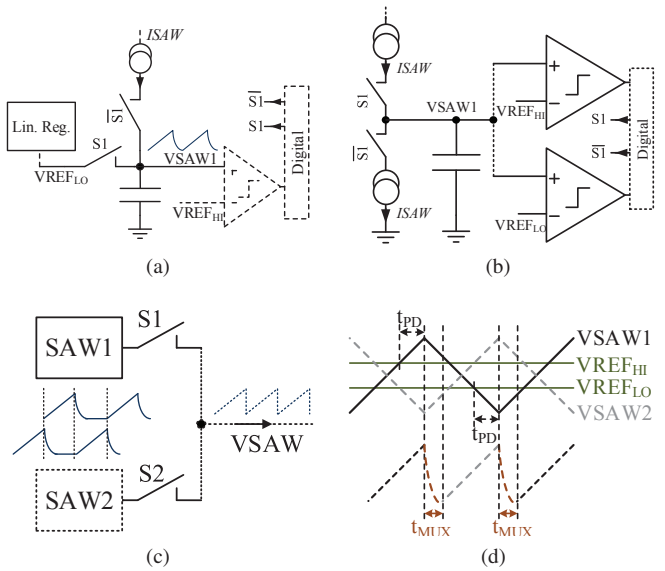


Fig. 3. Conventional sawtooth generator concepts a) using a linear regulator as lower reference, b) based on a triangular signal generator, c) multiplexing two interleaved sawtooth signals, d) the resulting multiplexed sawtooth signal of two triangular signal generators.

for a short time. The falling slope, shown in Fig. 2, is limited by the on-resistance of the switch. A larger switch would introduce parasitic coupling and add a non-linear parasitic capacitance to the main capacitor. During the falling slope either the maximum on- or the maximum off time of the PWM is limited, depending on the time when PWM signal is reset. A large discharge current to the output of the linear regulator would cause a significant voltage step at $VREF_{LO}$. A large buffer capacitance is not suitable as it makes the linear regulator too slow, and it would require a large die size.

The coupling to the reference can be avoided with the concept shown in Fig. 3b. A capacitor is charged and discharged with an identical reference current $ISAW$, which results in a triangular signal. The upper as well as the lower level $VREF_{HI}$ and $VREF_{LO}$ of the sawtooth signal are detected by a comparator. For both Figures 3a and 3b a faster falling slope is achieved by multiplexing two phase shifted sawtooth signals, as shown in Fig. 3c. Only the parasitic capacitances of the switches in the multiplexer and the output node have to be discharged. Two identical triangular generators are required to be multiplexed. The resulting signals of the multiplexed triangular signals and the resulting sawtooth signal are shown in Fig. 3d. At high frequencies, the ramp up time and thus the period of the multiplexed sawtooth signal is mainly determined by the propagation delay t_{PD} of the comparator, which varies over process variations and temperature by more than 30 % [9]. This drawback also applies to the single stage generator of Fig. 3b.

Another disadvantage of the multiplexed sawtooth concept is, that during the fast falling slope at the output of the multiplexer (see Fig. 3c) the input capacitances of the following PWM comparator and the capacitances of the multiplexer have to be discharged. As shown in Fig. 3d, the falling slope during t_{MUX} limits the minimum on-time of the PWM signal [2].

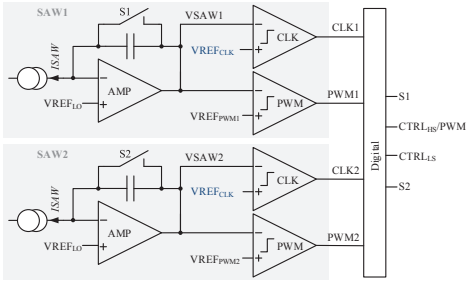


Fig. 4. Proposed sawtooth generator, based on two interleaved integrator stages.

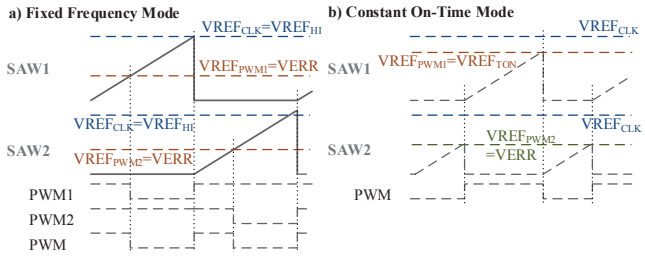


Fig. 5. Signals of the sawtooth generator a) in oscillator mode and b) constant on-time mode.

III. Proposed Sawtooth Based PWM Generator

The proposed configurable sawtooth based PWM generator, shown in Fig. 4, is able to generate PWM pulses as small as 2 ns. The reference current $ISAW$ and the upper ramp reference $VREF_{HI}$ is adjustable and thus allows to control the slope and amplitude of the ramps. This enables a wide frequency range from < 2 MHz up to > 50 MHz.

Two parallel integrator stages are used as sawtooth generators to obtain interleaved ramp signals $VSAW1$ and $VSAW2$ [10]. Each stage uses two comparators (PWM and CLK) directly at the integrator output. An independent digital control of each stage allows to configure the sawtooth generator to operate in fixed frequency mode (normal converter operation) or constant on-time mode (VIN step). The signals of the proposed sawtooth generator are shown in Fig. 5. In fixed frequency mode, both CLK comparators detect when the ramp reaches the upper sawtooth level $VREF_{CLK}$. This determines the switching frequency of the converter (Fig. 5a). When a CLK comparator detects a ramp crossing $VREF_{CLK}$, the ramp is reset and the ramp of the complementary stage is started. Each of the PWM comparators at the integrator outputs generate the signals $PWM1$ and $PWM2$ during the ramp phase of its stage by comparing the ramp to the voltage $VERR$ of the error amplifier. The final PWM signal is generated by a digital circuit. The PWM signal is set high when a ramp crosses $VREF_{CLK}$ and is set low on each of the falling edges of $PWM1$ and $PWM2$. In constant on-time mode, the ramps are reset already after crossing $VREF_{PWM1}$ or $VREF_{PWM2}$, respectively. The on-time of the PWM signal can be adjusted by multiplexing a constant reference $VREF_{TON}$ to the PWM comparator reference $VREF_{PWM1}$. The output voltage of the converter is regulated by applying the error voltage $VERR$ to the reference $VREF_{PWM2}$ of the second PWM comparator. The result is a variable frequency.

The ramps of the sawtooth signals are generated by an integrator. The output of an amplifier is regulated to the lower reference $VREF_{LO}$ while the switches S1, S2 short the feedback capacitor. When the switch is turned off, the current $ISAW$, drawn out of the negative input of the amplifier, is integrated, and a linear ramp is obtained. The reset of the one ramp can occur slowly during the ramp time of the other integrator stage.

A standard symmetrical amplifier is used for the integrator, which is suitable to achieve the required bandwidth, fast enough to settle during the ramp time of the complementary integrator stage. The amplifier in the integrator can be designed faster than a linear regulator used for the concept of Fig. 3a. As the integrator's feedback capacitor provides a miller-compensation at the same time, no additional capacitance has to be added to limit the bandwidth. The switch across the feedback capacitor is implemented as a transmission gate. Both parallel PMOS and NMOS switches have identical parasitic capacitances to compensate the coupled charge during their complementary switching. While conventional concepts have closed switches in the charging path, the switches in the proposed concept are open during the ramp up. Thus, the resistance and the size of the switches can be kept small and the influence on the ramp is negligible. The switches only have to assure to discharge the sawtooth signal during the charging time of the complementary ramp.

All four comparators are 3-stage high-speed comparators, because a fast detection of a very small voltage difference at the comparator input is required . The first and second stage are implemented fully differentially with a sufficient gain to increase the voltage swing. In the third stage, which provides a single ended output with full voltage swing for the digital circuit, the charging and discharging of parasitic capacitances are dominant. Thus, instead of maximizing the gain, the sizes of all transistors in the signal path are kept at a minimum. A further buffer stage is used to drive the digital load.

Compared to the conventional concepts in Fig. 3, the PWM comparator has to be used two times, but no multiplexing of the sawtooth ramps is required. Multiplexing is done in the digital domain. As the CLK and PWM comparators are independent of each other, the minimum on-time of the PWM signal only depends on the propagation delay of the PWM comparator and the digital circuit, and is not limited to the time t_{MUX} of the multiplexed falling edge of the sawtooth signal, as shown in Fig. 3d. Thus, the remaining minimum pulse width is limited by the bandwidth of the technology. Another advantage of this concept is that the charging current of the capacitor is not drawn from the reference $VREF_{LO}$, as it is the case in the concept shown in Fig. 3a. A common reference can be used for all integrator stages without any interference.

IV. Experimental Results

The proposed PWM generator was implemented in a buck converter fabricated in a 180 nm HV BiCMOS Technology. A microphotograph of the sawtooth generator is shown in Fig. 6. Measurement results of the sawtooth generator at a frequency of 10 MHz in Fig. 7a. The interleaved ramps are started at $VREF_{LO} = 1.5$ V. The ramp is charged with a $ISAW = 26$ µA up to the upper reference $VREF_{HI} =$

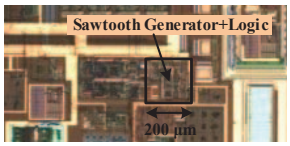
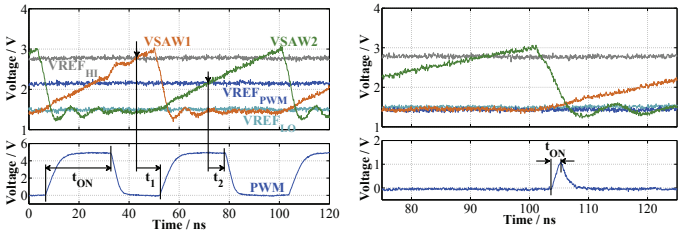


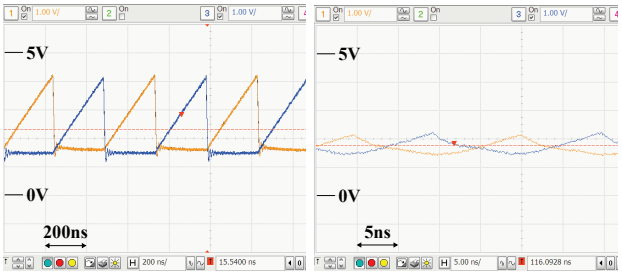
Fig. 6. Microphotograph of the sawtooth generator, implemented in a 180 nm HV BiCMOS technology.



(a) (b)

Fig. 7. Measured sawtooth generator signals at 10 MHz and the PWM signal at a) 50 % duty cycle and b) minimum on-time of 2 ns.

2.8 V. The reference for both PWM comparators is set in the center between $VREF_{LO}$ and $VREF_{HI}$ to $VREF_{PWM1} = VREF_{PWM2} = 2.15$ V. When the ramp reaches $VREF_{HI}$, the second ramp $VSAW2$ is started and the PWM signal is set to high after t_1. When $VSAW2$ reaches $VREF_{PWM}$, the PWM comparator turns low and sets the falling edge of the PWM signal with a delay of the comparator and the digital circuit t_2. The minimum possible on-time of PWM would be limited to t_2, when $VREF_{PWM}$ is very close to $VREF_{LO}$ and the PWM comparator switches immediately after the ramp has started. To reduce the minimum possible on-time to a minimum, an additional digital delay of approximately 3 ns is added to t_1 to delay the rising edge of the on-time pulse, and thus compensate for the comparator delay. Thus, the resulting duty cycle of $D = 50.5\,\%$ matches the expected value. A minimum on-time of the PWM signal of $t_{ON} = 2$ ns is achieved in a measurement shown in Fig. 7b. Due to the interleaved stages, the resulting PWM runs at 20 MHz, which is twice the frequency of the sawtooth generators. The slopes of the digital nodes, i.e. the comparator outputs and the PWM signal at the digital output, are significantly reduced in the on-chip measurement, as the probes added a considerable capacitance. Even with Picoprobes, the probe capacitance is at least 5 times larger than the node capacitances. Thus the PWM signal at minimum on-time a rail-to-rail switching cannot be measured, but the turn high and turn low events are indicated.



(a) (b)

Fig. 8. Complementary sawtooth signals measured at a) 2 MHz b) 50 MHz.

The frequency of the sawtooth stages can be adjusted over a wide range by either adjusting the upper reference $VREF_{CLK}$ or by a variation of the externally adjustable reference current $ISAW1 = ISAW2$. Figure 8 shows measurements at a sawtooth frequency of 2 MHz and of 50 MHz, which results in a PWM frequency of 4 MHz and 100 MHz, respectively. Thus, a converter with a switching frequency of 100 MHz could still work with a duty cycle down to 20 % using the proposed sawtooth based PWM generator.

V. Conclusion

A sawtooth based PWM generator suitable for DCDC converters with switching frequencies > 50 MHz and very low duty cycles at high conversion ratios is presented. Two digitally multiplexed, fully interleaved integrator stages, each including a ramp and the PWM comparator, allow minimal pulses of the PWM signal. The on-time is not limited by the finite reset time of the sawtooth signals. A separation of the PWM comparator references of each interleaved stage allows to digitally configure DCDC converters for fixed frequency or constant on-time mode during operation. A digital delay compensation of the PWM comparator allows on-time pulses of the PWM signal of < 2 ns, confirmed by measurements from a test chip in 180nm high-voltage BiCMOS technology. An adjustable reference current controlling the slope of the sawtooth ramps offers an adjustable gain of the converter output voltage regulation. Together with a variable reference for the sawtooth amplitude, the PWM signal can be adjusted over a wide frequency range. Measurements confirms a frequency of the interleaved sawtooth signals of 2 MHz and 50 MHz, which results in a PWM frequency range of 4 MHz and 100 MHz.

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