COMS12200 problem set #5

Within this problem slot, the idea is that you attempt to solve the set of pencil-and-paper, exam-style questions presented below; in doing so, you can (optionally) use an interactive system to anonymously register your solutions. More concretely, optionally start by installing the Socrative client, e.g.,

- for Chrome

  http://chrome.google.com/webstore/detail/socrative-student/nblhpecglllndfihipmpdoikimcmgkha

- for Android

  http://play.google.com/store/apps/details?id=com.socrative.student

- for iOS

  http://itunes.apple.com/gb/app/socrative-student/id477618130

or using the web-based application at

http://www.socrative.com,

then entering the 9-character "room name" which should be displayed top-center on the projector screen. Then, we will alternate as follows:

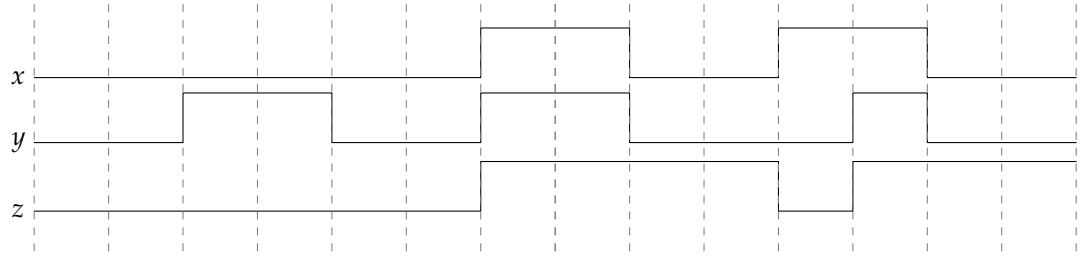
1. solve the current question, and optionally register your solution using Socrative,
2. wait until everyone is finished (or say ∼ 5 minutes elapse), at which point we will discuss the questions and solutions using any collated Socrative results as a starting point.

Q1. From the following list

`A:` the design of a DRAM cell includes more transistors than an SRAM cell
`B:` an SRAM cell can store more information than a DRAM cell
`C:` SRAM cells can be accessed more quickly than DRAM cells
`D:` DRAM cells require a mechanism to refresh their content

identify **each** statement that correctly describes SRAM and DRAM cells.

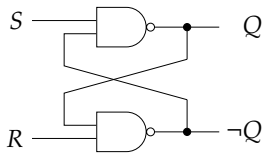
Q2. Consider the following waveform



which details the behaviour of three signals labelled x, y and z. Which of the following components *could* the behaviour illustrated relate to?

`A:` an SR-type flip-flop
`B:` an SR-type latch
`C:` a D-type flip-flop
`D:` a D-type latch
`E:` a T-type flip-flop

Q3. The following diagram



illustrates a preliminary NAND-based SR-latch design, in the sense it currently lacks an enable signal. If Q and Q' denote the current and next state respectively, which of the following excitation tables

			Current		*Next*	
	S	R	Q	$\neg Q$	Q'	$\neg Q'$
A:	0	0	0	1	0	1
	0	0	1	0	1	0
	0	1	?	?	0	1
	1	0	?	?	1	0
	1	1	?	?	0	0
B:	0	0	?	?	1	1
	0	1	?	?	1	0
	1	0	?	?	0	1
	1	1	0	1	0	1
	1	1	1	0	1	0
C:	0	0	?	?	0	1
	1	1	?	?	1	0
D:	0	?	?	?	0	1
	1	?	?	?	1	0
E:	?	0	?	?	0	1
	?	1	?	?	1	0

correctly captures the behaviour of this circuit?

Q4. Consider a DRAM memory device with a capacity of 65536 addressable bytes. Of the following options

A: 8 address pins, 65536 cells
B: 16 address pins, 65536 cells
C: 8 address pins, 524288 cells
D: 16 address pins, 524288 cells

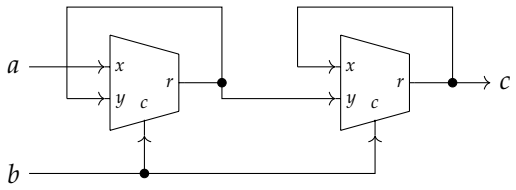
which offers the most likely description of said device?

Q5. Figure 1 illustrates the design of a DRAM memory. The labels on four components in the block diagram have been blanked-out, then replaced with the symbols α, β, γ and δ: which of the following mappings

A:	α	$\mapsto$	row address buffer
	β	$\mapsto$	row address decoder
	γ	$\mapsto$	column address buffer
	δ	$\mapsto$	column address decoder
B:	α	$\mapsto$	row address buffer
	β	$\mapsto$	column address buffer
	γ	$\mapsto$	row address decoder
	δ	$\mapsto$	column address decoder
C:	α	$\mapsto$	column address buffer
	β	$\mapsto$	row address buffer
	γ	$\mapsto$	column address decoder
	δ	$\mapsto$	row address decoder
D:	α	$\mapsto$	row address decoder
	β	$\mapsto$	column address decoder
	γ	$\mapsto$	row address buffer
	δ	$\mapsto$	column address buffer
E:	α	$\mapsto$	column address decoder
	β	$\mapsto$	row address decoder
	γ	$\mapsto$	column address buffer
	δ	$\mapsto$	row address buffer

do you think is correct?

Q6. Although perhaps unusual, the following diagram



illustrates a circuit with well defined behaviour. Based on analysis of this behaviour, which of the following components

`A:` a flip-flop
`B:` a latch
`C:` a RAM cell
`D:` a ROM cell
`E:` a clock multiplier

does the circuit implement?

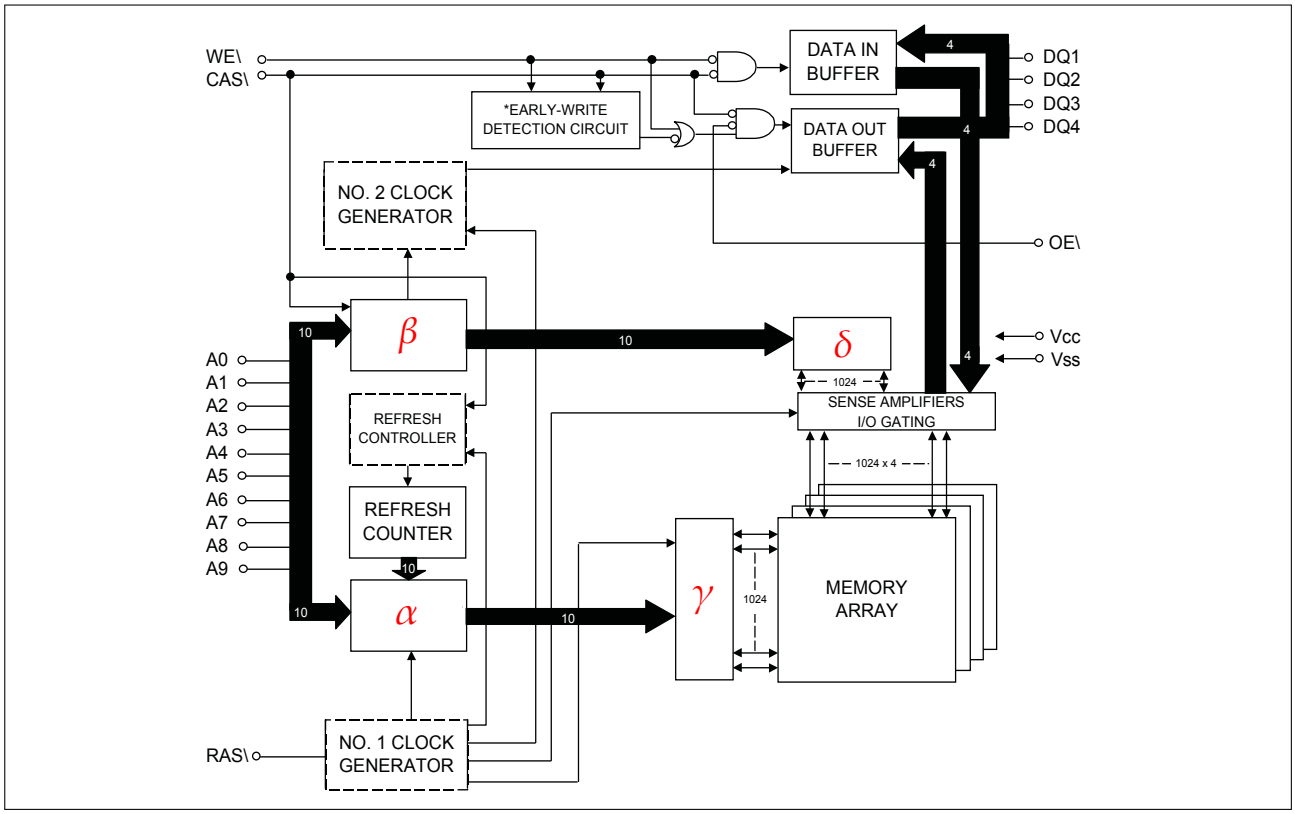


Figure 1: *A* 4Mbit *DRAM block diagram (source:* `http://www.micross.com/pdf/MT4C4001J.pdf`*).*