COMS12200 problem set #6

Within this problem slot, the idea is that you attempt to solve the set of pencil-and-paper, exam-style questions presented below; in doing so, you can (optionally) use an interactive system to anonymously register your solutions. More concretely, optionally start by installing the Socrative client, e.g.,

- for Chrome

  http://chrome.google.com/webstore/detail/socrative-student/nblhpecglllndfihipmpdoikimcmgkha

- for Android

  http://play.google.com/store/apps/details?id=com.socrative.student

- for iOS

  http://itunes.apple.com/gb/app/socrative-student/id477618130

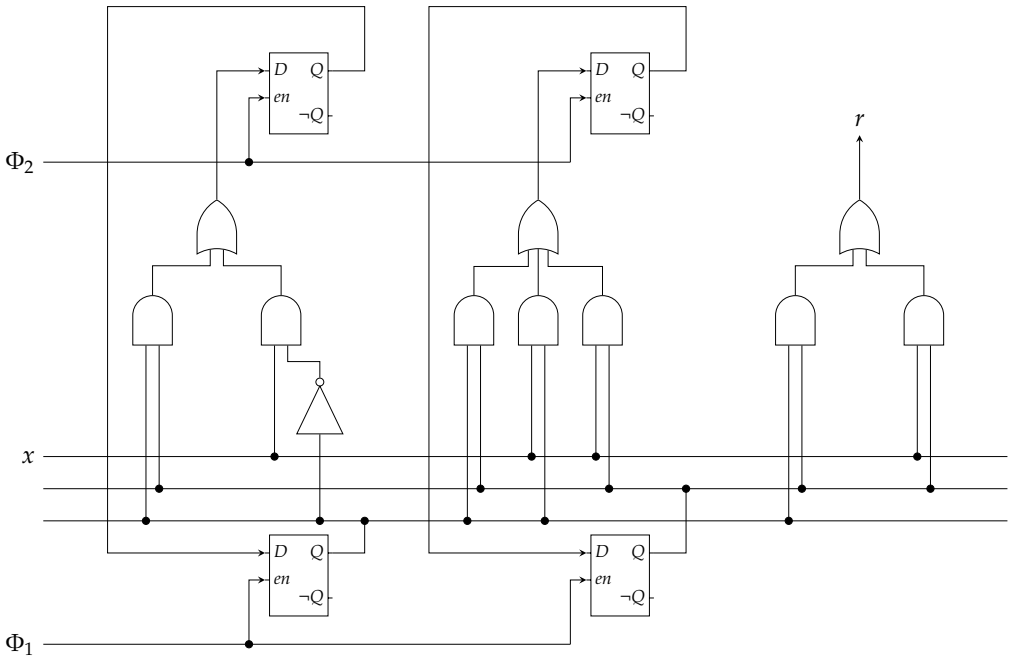
or using the web-based application at

http://www.socrative.com,

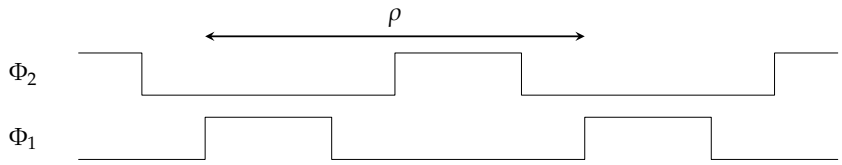
then entering the 9-character "room name" which should be displayed top-center on the projector screen. Then, we will alternate as follows:

1. solve the current question, and optionally register your solution using Socrative,
2. wait until everyone is finished (or say ∼ 5 minutes elapse), at which point we will discuss the questions and solutions using any collated Socrative results as a starting point.

All questions in this Section relate to a Finite State Machine (FSM) whose concrete implementation is as follows:



Notice that the implementation is based on use of four D-type latches, and a 2-phase clock supplied via Φ_1 and Φ_2; one additional input x plus one output r are also evident. To function correctly, a clock generator ensures Φ_1 and Φ_2 are driven as follows:



Q1. From the following list

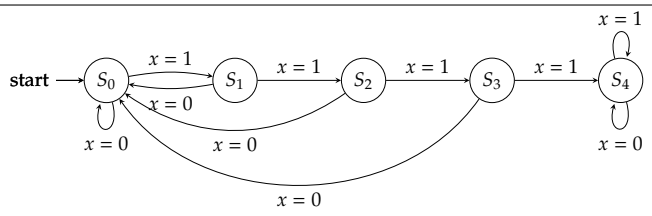
A: Φ_1 and Φ_2 are digital signals
B: Φ_1 and Φ_2 are non-overlapping
C: Φ_1 and Φ_2 are gated
D: Φ_1 and Φ_2 are unskewed
E: Φ_1 and Φ_2 each have a duty cycle of 33%

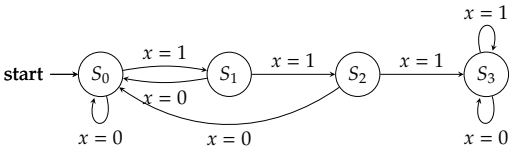
identify **each** property the clock generator *must* guarantee is true for the implementation to function correctly.

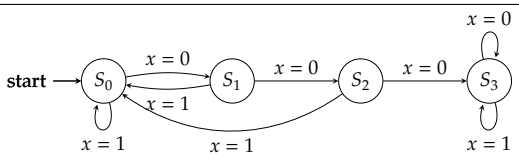
Q2. Consider the two D-type latches at the bottom of the diagram, which form a 2-bit register. Imagine the value stored in this register is expressed as a 2-bit integer: when the implementation is initially powered-on, is this value equal to

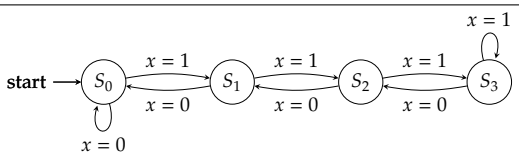
A: $00_{(2)}$
B: $01_{(2)}$
C: $10_{(2)}$
D: $11_{(2)}$
E: any of the above

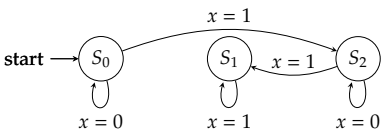
Q3. Any FSM specification will include a transition function, often denoted δ, which can be described in either tabular or diagrammatic form. Of the following options

A :


B :


C :


D :


E :


which captures the transition function of this FSM?

Q4. Which of the following FSM types, namely

A: Mealy
B: Moore

does this implementation represent?

Q5. In the 2-phase clock waveform above, ρ illustrates the clock period: recall this is inversely proportional to the clock frequency. Imagine the gate delay for NOT, AND, and 2- and 3-input OR gates are 10ns 20ns 20ns, 30ns respectively, and the critical path associated for a D-type latch is 60ns. Which of the following best matches the maximum possible clock frequency of this implementation?

A: 1.0kHz
B: 5.9MHz
C: 9.0MHz
D: 9.5MHz
E: 1.0GHz

Q6. Which of the following best describes the purpose of this FSM?

A: set $r = 1$ iff. the current value of x is different from the previous value of x,
B: act as a modulo 4 counter that is incremented by the value of x, and set $r = 1$ the current counter value is zero,
C: compute the Hamming weight of a sequence fed as input bit-by-bit via x, and set $r = 1$ once this is equal to 3
D: count the number of consecutive times $x = 1$, and set $r = 1$ once this is equal to 3
E: inspect the sequence fed as input bit-by-bit via x, and set $r = 1$ iff. this sequence, when interpreted as an unsigned integer, is odd