The BasIC PDK Circuit Theory

April 11th 2025

1 Circuit Theory

1.1 RC

The RC circuit used to validate both the resistor and capacitor Verilog-A models contains a charge equation 1 and a discharge equation 6 for the voltage across the load capacitor V_C.

$$V_C = V_{in}(1 - e^{-t/\tau}),\ \tau = RC = t_r/5 \tag{1}$$

$$V_C = V_{in}e^{-t/\tau},\ \tau = RC = t_f/5 \tag{2}$$

$$t_{pd} = 10RC \tag{3}$$

1.2 RL

The RL circuit is used to validate both the resistor and inductor Verilog-A models. The equations below include a charge equation 4 and a discharge equation 5. The output voltage V_L is taken across the inductor of the RL circuit.

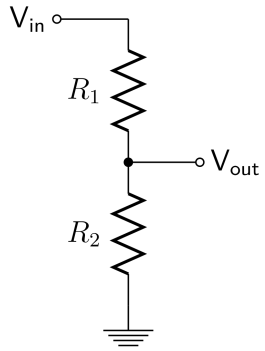
$$V_L = V_{in}(1 - e^{-t/\tau}),\ \tau = \frac{L}{R} = t_r/5 \tag{4}$$

$$V_L = V_{in}e^{-t/\tau},\ \tau = \frac{L}{R} = t_f/5 \tag{5}$$

$$t_{pd} = 10\frac{L}{R} \tag{6}$$

1.3 R-R Divider

The resistor-based voltage divider used to validate the Verilog-A resistor model uses equation 7 to characterize its output voltage.



$$V_{out} = \frac{R_2}{R_1 + R_2} V_{in} \tag{7}$$

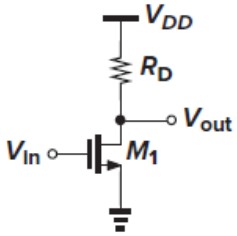
1.4 C-C Divider

The capacitor-based voltage divider used to validate the Verilog-A capacitor model uses equation 8 to characterize its output voltage.

$$V_{out} = \frac{C_1}{C_1 + C_2} V_{in} \tag{8}$$

1.5 Common Source Amplifier

The common-source amplifier used to validate the Verilog-A NMOS model uses equation 9 or 11 to characterize its output gain.



$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{R_S R_D \xi s^2 + (R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB}))s + 1} \tag{9}$$

$$\xi = C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB} \tag{10}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{-g_m R_D}{(1 + \frac{s}{\omega_{in}})(1 + \frac{s}{\omega_{out}})} \tag{11}$$

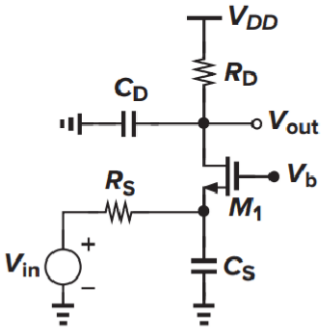
$$\omega_{in} = \frac{1}{R_S(C_{GS} + (1 + g_m R_D)C_{GD}} \tag{12}$$

$$\omega_{out} = \frac{1}{(R_D||(\frac{C_{GD}+C_{GS}}{C_{GD}} * \frac{1}{g_{m1}}))(C_{eq} + C_{DB})} \tag{13}$$

$$C_{eq} = C_{GD}C_{GS}/(C_{GD} + C_{GS}) \tag{14}$$

1.6 Common Gate Amplifier

The common gate amplifier will be used to validate the NMOS, Capacitor, and Resistor Verilog A models. The frequency response 15, and 22 will be used to validate results from simulation.

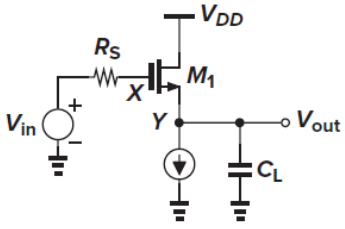


$$\frac{V_{out}}{V_{in}}(s) = \frac{(g_m + g_{mb})R_D}{(1 + (g_m + g_{mb}))R_s(1 + \frac{C_S}{g_m + g_{mb}R_S^{-}1}s)(1 + R_D C_D s)} \tag{15}$$

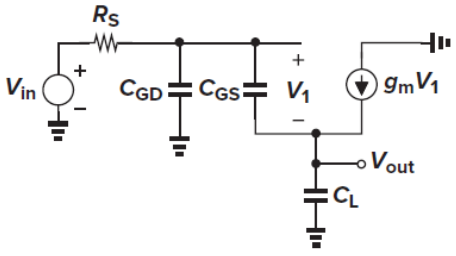
$$\omega_{p1} = \frac{1}{R_D C_S},\ \omega_{p2} = \frac{g_m + g_{mb} + R_S^{-1}}{C_s} \tag{16}$$

1.7 Source Follower Buffer

The source follower buffer used to validate the Verilog-A NMOS model uses equation 17 to characterize its output gain.



(a)



(b)

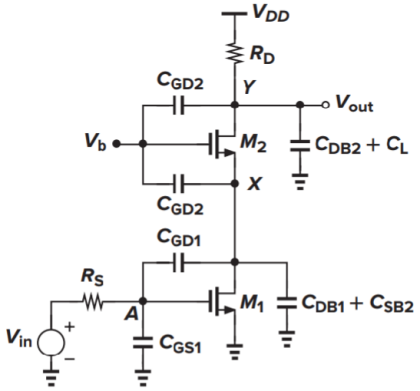
$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m + C_{GS}s}{R_S(C_{GS}C_L + C_{GS}C_{GD} + C_{GD}C_L)s^2 + (g_m R_S C_{GD} + C_L + C_{GS})s + g_m} \tag{17}$$

$$Z_{in} = \frac{1}{C_{GS}s} + \frac{1}{C_L s} + \frac{g_m}{C_{GS}C_L s^2} \tag{18}$$

$$Z_{out} = \frac{R_S C_{GS}s + 1}{g_m + C_{GS}s} \tag{19}$$

1.8 Common Source Cascode Amplifier

Verilog-A NMOS models will be used to implement the CS Cascode amplifier circuit topology. Equations 21, 20, and 22 will be used to validate the simulation results.



$$\omega_{py} = \frac{1}{R_D(C_{DB2} + C_L + C_{GS2}} \tag{20}$$

$$\omega_{px} = \frac{g_{m2} + g_{m1}}{2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2}} \tag{21}$$

$$\omega_{p1} = \frac{1}{R_D C_S},\ \omega_{p2} = \frac{g_m + g_{mb} + R_S^{-1}}{C_s} \tag{22}$$

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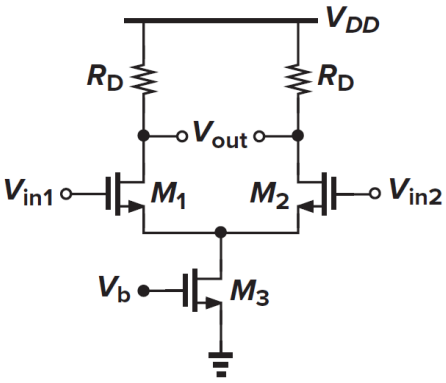
1.9 Differential Pair with Passive Load

The differential pair amplifier with a passive load used to validate the Verilog-A NMOS and resistor models uses equation 23 to characterize its output gain. It has input and output holes, calculated in equations 24 and 25.



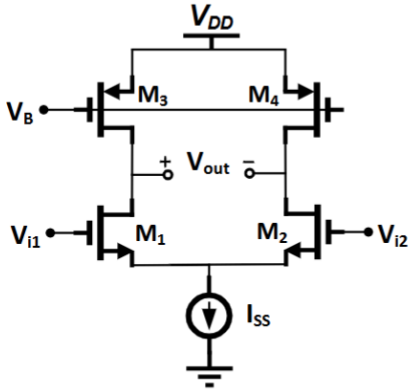
$$\frac{V_{od}}{V_{id}} = -g_m R_D \tag{23}$$

$$\omega_{in} = \frac{1}{R_S(C_{GS} + (1 + g_m R_D)C_{GD})} \tag{24}$$

$$\omega_{out} = \frac{1}{R_D || (\frac{C_{GD}+C_{GS}}{C_{GD}} * \frac{1}{g_{m1}})(C_{eq} + C_{DB})} \tag{25}$$

1.10 Differential Pair with Active Load

Verilog-A NMOS and PMOS models will be used to implement a differential pair with active load circuit topology. Equations 27, 28, and 26 will be used to validate the simulation results.



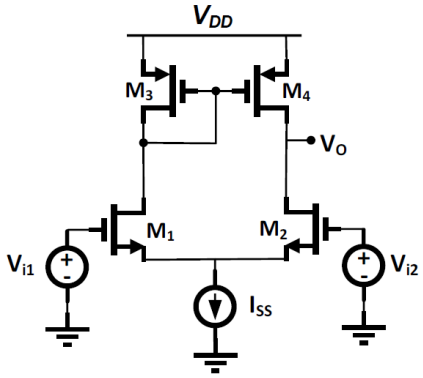
$$\frac{V_{od}}{V_{id}} = g_{m1} \times r_{on} || r_{op} \tag{26}$$

$$\omega_{in} = \frac{1}{R_S(C_{GS} + (1 + g_m R_D)C_{GD})} \tag{27}$$

$$\omega_{out} = \frac{1}{R_D||(\frac{C_{GD}+C_{GS}}{C_{GD}} * \frac{1}{g_{m1}})(C_{eq} + C_{DB})} \tag{28}$$

1.11 Differential Pair with Current Mirror

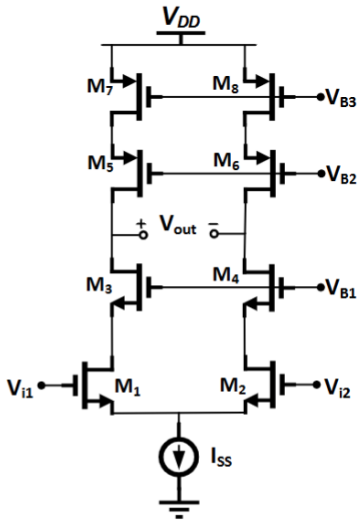
The differential pair amplifier with a current mirror used to validate the Verilog-A NMOS and PMOS models uses equation 29 to characterize its output gain.



$$\frac{V_{out}}{V_{in}} = \frac{g_{mN} r_{oN} (2g_{mP} + C_E s) r_{oP}}{2r_{oP} r_{oN} C_E C_L s^2 + ((2r_{oN} + r_{oP})C_E + r_{oP}(1 + 2g_{mP} r_{oN})C_L)s + 2g_{mP}(r_{oN} + r_{oP})} \tag{29}$$

1.12 Differential Pair with Cascode Driver and Load

The differential pair amplifier with a cascode driver and load will be used to validate the Verilog-A NMOS and PMOS models using equation 30 to characterize its output gain.



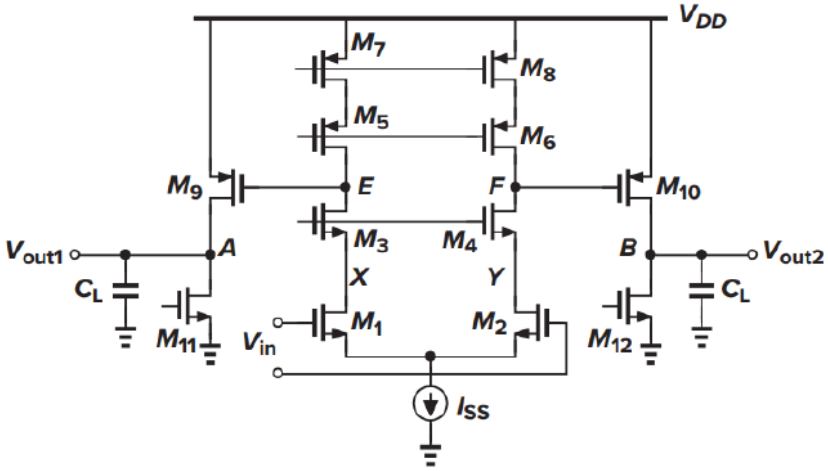
$$\frac{V_{od}}{V_{id}} \approx g_{m1}[(g_{m3}r_{o3}r_{o1})||(g_{m5}r_{o5}r_{o7})] \tag{30}$$

1.13 OpAmp with Two Poles

The single stage OpAmp, differential pair with passive load, amplifier will be used to validate the Verilog-A model OpAmp with Two Poles.

1.14 Two-Stage OpAmp with Three Poles

The two-stage opamp used to validate the Verilog-A OpAmp models has three poles. The following is a detailed transistor model; however, the validation model uses two OpAmps (1-pole and 2-pole versions).



1.15 1.25V Reference with MOSFET and BJT

The 1.25V reference voltage source, shown below, will be implemented using NMOS, PMOS, and PNP Verilog A models.