The BasIC PDK User Guide and Circuit Theory

April 11th 2025

1 Overview

The BasIC PDK User Guide includes the respective Verilog-A module parameters, constants, and associated circuit theory.

2 Physical Constants

Constant	Value	Units
ϵ_o	$8.854e-12$	F/m
ϵ_{si}	$1.036e-11$	F/m
k	$1.38e-23$	J/K
q	$1.60e{-}19$	C
n_i	10^{10}	cm^{-3}

2.1 NMOS/PMOS Physical Parameters

NMOS	Value	PMOS	Value	Units
V_{THN}	1.0	V_{THP}	-1.05	V
N_{nsub}	$9e+14$	N_{psub}	$5e+14$	cm^{-3}
t_{nox}	$9e-3$	t_{pox}	$9e-3$	um
C_{jswn}	$0.35e^{-11}$	C_{jswp}	$0.32e^{-11}$	F/m
C_{jn}	$0.56e^{-3}$	C_{jp}	$0.94e^{-3}$	F/m^2
Φ_{msn}	0.31	Φ_{msp}	-1.36	V
μ_n	350×10^{-4}	μ_p	100×10^{-4}	$m^2/V/s$
C_{ovn}	0.4×10^{-9}	C_{ovp}	0.3×10^{-9}	F/m
E_n	10^{-6}	E_p	10^{-6}	m
I_{s0n}	10^{-9}	I_{s0p}	10^{-9}	A
λ_n	0.1	λ_p	0.2	V^{-1}

N_{sub}: substrate doping.
t_{ox}: Gate-oxide thickness.
C_j: Junction capacitance.
C_{jsw}: Junction sidewall capacitance.
Φ_{ms}: Gate work function.

μ: Carrier mobility.
Cov: Gate-drain, Gate-source overlap capacitance.
E: Drain and source length.
I_{s0}: Subthreshold leakage current.
λ: Channel length modulation coefficient.

3 Models

3.1 NMOS

3.1.1 External Parameters

Parameter	Type	Supported Values	Description
body_effect	Integer	[0, 1]	Enables body effect.
cl_modulation	Integer	[0, 1]	Enables Channel Length Modulation.
parasitics	Integer	[0, 1]	Enables Parasitic Capacitors.
width	Real	(0, 100μ]	Channel width in m.
length	Real	(0, 100μ]	Channel length in m.
mismatch	Integer	[0,1]	Enables component mismatch.
procVar	Integer	[0,1]	Enables process variation.
procVal	Real	[0,0.1)	Process variation factor.

Table 1: NMOS Verilog-A Model Parameters

3.1.2 Equations and Internal Parameters

$$L = length(1 + procVar * procVal * 0.2) + mmatch * mmVal * rand(seed) \quad (1)$$

$$W = width(1 + procVar * procVal * 0.2) + mmatch * mmVal * rand(seed) \quad (2)$$

$$t'_{ox} = t_{ox}(1 + procVar * procVal * 0.2) + mmatch * mmVal * rand(seed) \quad (3)$$

$$C_{ox} = \frac{\epsilon_{ox}}{t'_{ox}} \quad (4)$$

$$I_D = \left\{ \begin{array}{l} I_0 \frac{W}{L} e^{\frac{V_{GS}}{\xi V_T}},\ V_{GS} < V_{THN} \\ 0.5\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{THN})^2(1 + \lambda V_{DS}), V_{THN} < V_{GS} \leq V_{DS} + V_{THN} \\ \frac{WLC_{ox}}{2} + WC_{ov},\ V_{GS} \geq V_{DS} + V_{THN} \end{array} \right\} \quad (5)$$

$$\Gamma = I_{sub}(V_{GS})\delta_{cl}(V_{GS}) \tag{6}$$

$$\delta_{cl}(V_{GS}) = \left\{ \begin{array}{l} clme(1+\lambda V_{DS}),\ (V_{THN} \le V_{GS} \le V_{DS}+V_{THN}) \\ 1,\ V_{GS} < V_{THN}\ or\ V_{GS} > V_{DS}+V_{THN} \end{array} \right\} \tag{7}$$

$$I_{sub}(V_{GS}) = \left\{ \begin{array}{l} 1,\ V_{GS} > V_{THN} \\ (isth)\exp(\frac{V_{GS}}{\xi V_T}),\ V_{GS} \le V_{THN} \end{array} \right\} \tag{8}$$

$$V_{THN} = V_{THN0} + (be \times \gamma)(\sqrt{2\Phi_F + |V_{SB}|} - \sqrt{|2\Phi_F|}) \tag{9}$$

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_{sub}}}{C_{ox}} \tag{10}$$

$$V_{THN0} = \Phi_{MS} + 2\Phi_F + \frac{\sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}}{C_{ox}} \tag{11}$$

$$\Phi_F = \frac{kT}{q}\ln(\frac{N_{sub}}{n_i}) \tag{12}$$

3.1.3 Internal Parasitic Capacitance

The BasICPDK NMOS model captures parasitic gate-source, gate-drain, drain-body, source-body, and gate-body parasitic capacitance through a set of piece-wise and linear equations.

$$C_{SB} = C_{DB} = WEC_{J0}(1+\frac{V_R}{\Phi_B})^{-m} + 2(W+E)C_{J0}(1+\frac{V_R}{\Phi_B})^{-m} \tag{13}$$

$$C_{GB} = \left\{ \begin{array}{l} \frac{WLC_{ox}C_d}{WLC_{ox}+C_d},\ V_{GS} < V_{THN} \\ 0,\ V_{GS} \ge V_{THN} \end{array} \right\} \tag{14}$$

$$C_{GD} = \left\{ \begin{array}{l} WC_{ov},\ V_{GS} < V_{DS}+V_{THN} \\ \frac{WLC_{ox}}{2} + WC_{ov},\ V_{GS} \ge V_{DS}+V_{THN} \end{array} \right\} \tag{15}$$

$$C_{GS} = \left\{ \begin{array}{l} WC_{ov},\ V_{GS} < V_{THN} \\ \frac{2}{3}WLC_{ox} + WC_{ov}, V_{THP} < V_{GS} \le V_{DS}+V_{THN} \\ \frac{WLC_{ox}}{2} + WC_{ov},\ V_{GS} \ge V_{DS}+V_{THN} \end{array} \right\} \tag{16}$$

3.2 PMOS

3.2.1 External Parameters

Parameter	Type	Supported Values	Description
be	Integer	[0, 1]	Enables body effect.
clme	Integer	[0, 1]	Enables Channel Length Modulation.
width	Real	(0, 100]	Channel width in m.
length	Real	(0, 100]	Channel length in m.
mmatch	Integer	[0,1]	Enables component mismatch.
procVar	Integer	[0,1]	Enables process variation.
procVal	Real	[0,1]	Process variation factor.

Table 2: PMOS Verilog-A Model Parameters

3.2.2 Equations and Internal Parameters

$$L = length(1 + procVar * *procVal0.2) + mmatch * mmVal * rand(seed) \quad (17)$$

$$W = width(1 + procVar * procVal * 0.2) + mmatch * mmVal * rand(seed) \quad (18)$$

$$t'_{ox} = t_{ox}(1 + procVar * procVal * 0.2) + mmatch * mmVal * rand(seed) \quad (19)$$

$$C_{ox} = \frac{\epsilon_{ox}}{t'_{ox}} \quad (20)$$

$$I_{off} = I_{s0p} e^{\frac{V_{GS}}{V_t}} \quad (21)$$

$$I_{tri} = -\mu_p C_{ox} \frac{W}{L}[(V_{GS} - |V_{THP}|)V_{DS} - \frac{1}{2}V_{DS}^2] \quad (22)$$

$$I_{sat} = -\mu_p C_{ox} \frac{W}{L}[(V_{GS} - |V_{THP}|)^2(1 + clme\lambda V_{DS}) \quad (23)$$

$$I_{ds} = \left\{ \begin{array}{l} I_{off}, |V_{GS}| < |V_{THP}| \\ I_{tri}, |V_{DS}| \leq |V_{GS}| - |V_{THP}| \\ I_{sat}, |V_{DS}| > |V_{GS}| - |V_{THP}| \end{array} \right\} \quad (24)$$

$$V_{THP} = V_{THP0} + (be \times \gamma)(\sqrt{2\Phi_F + |V_{SB}|} - \sqrt{2\Phi_F}) \tag{25}$$

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_{sub}}}{C_{ox}} \tag{26}$$

$$V_{THP0} = \Phi_{msp} + 2\Phi_F + \frac{\sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}}{C_{ox}} \tag{27}$$

$$\Phi_F = \frac{kT}{q}\ln(\frac{N_{sub}}{n_i}) \tag{28}$$

3.2.3 Internal Parasitic Capacitance

The BasICPDK PMOS model captures parasitic gate-source, gate-drain, drain-body, source-body, and gate-body parasitic capacitance through a set of piecewise and linear equations.

$$C_{SB} = C_{DB} = WEC_{jp} + 2(W+E)C_{jswp} \tag{29}$$

$$C_{GB} = \left\{ \begin{array}{l} \frac{WLC_{ox}C_d}{WLC_{ox}+C_d},\ V_{GS} < V_{THP} \\ 0,\ V_{GS} \geq V_{THP} \end{array} \right\} \tag{30}$$

$$C_{GD} = \left\{ \begin{array}{l} WC_{ov},\ V_{GS} < V_{DS} + V_{THP} \\ \frac{WLC_{ox}}{2} + WC_{ov},\ V_{GS} \geq V_{DS} + V_{THP} \end{array} \right\} \tag{31}$$

$$C_{GS} = \left\{ \begin{array}{l} WC_{ov},\ V_{GS} < V_{THP0} \\ \frac{2}{3}WLC_{ox} + WC_{ov}, V_{THP} < V_{GS} \leq V_{DS} + V_{THP} \\ \frac{WLC_{ox}}{2} + WC_{ov},\ V_{GS} \geq V_{DS} + V_{THP} \end{array} \right\} \tag{32}$$

3.3 Resistor

3.3.1 External Parameters

Parameter	Type	Supported Values	Description
α	Real	[0, 1)	First order temperature coefficient.
β	Real	[0, 1)	Second order temperature coefficient.
κ	Real	[0, 1)	Third order temperature coefficient.
ρ_o	Real	$(0, \infty)$	Material resistivity, $\frac{\Omega m}{K}$ at T_o.
T_o	Real	$(0, \infty)$	Measurement Temperature (K) of ρ_o
width	Real	$(0, 10^{-4}]$	Width in m.
length	Real	$(0, 10^{-4}]$	Length in m.
thick	Real	$(0, 10^{-4}]$	Thickness of material in m.
mmatch	Integer	[0,1]	Enables component mismatch.
procVar	Integer	[0,1]	Enables process variation.
procVal	Real	[0,1)	Process variation factor.

Table 3: Resistor Verilog-A Model Parameters

3.3.2 Equation and Internal Parameters

$$R = \frac{\rho_o}{t}(1 + \alpha(T - T_o) + \beta(T - T_o)^2 + \kappa(T - T_o)^3)\frac{L}{W} \tag{33}$$

$$L = length(1 + procVar * procVal) + mmatch * rand(seed) \tag{34}$$

$$W = width(1 + procVar * proVal) + mmatch * rand(seed) \tag{35}$$

$$t = thick(1 + procVar * procVal) + mmatch * rand(seed) \tag{36}$$

3.4 Capacitor

3.4.1 External Parameters

Parameter	Type	Supported Values	Description
α	Real	[0, 1)	First order temperature coefficient.
β	Real	[0, 1)	Second order temperature coefficient.
κ	Real	[0, 1)	Third order temperature coefficient.
ϵ_r	Real	(0, ∞)	Material permittivity at T_0.
T_o	Real	(0, ∞)	Measurement Temperature (K) of ϵ_r
width	Real	(0, 100]	Width in m.
length	Real	(0, 100]	Length in m.
distance	Real	(0, 100]	Distance between planes in m
mismatch	Integer	[0,1]	Enables component mismatch.
procVar	Integer	[0,1]	Enables process variation.
procVal	Real	[0,1)	Process variation factor.

Table 4: Capacitor Verilog-A Model Parameters

3.4.2 Equation and Internal Parameters

$$C = \frac{\epsilon WL}{d}(1 + \alpha(T - T_o) + \beta(T - T_o)^2 + \kappa(T - T_o)^3) \tag{37}$$

$$L = length(1 + procVar * procVal) + mmatch * rand(seed) \tag{38}$$

$$W = width(1 + procVar * proVal) + mmatch * rand(seed) \tag{39}$$

$$t = thick(1 + procVar * procVal) + mmatch * rand(seed) \tag{40}$$

$$d = distance(1 + procVar * procVal) + mmatch * rand(seed) \tag{41}$$

3.5 Inductor

3.5.1 External Parameters

Parameter	Type	Supported Values	Description
α	Real	[0, 1)	First order temperature coefficient.
β	Real	[0, 1)	Second order temperature coefficient.
κ	Real	[0, 1)	Third order temperature coefficient.
μ_r	Real	(0, ∞)	Relative permeability of material at T_0.
T_o	Real	(0, ∞)	Temperature (K) at which μ_r was measured.
length	Real	(0, 100]	Length of the material wire in m.
radius	Real	(0, 100]	radius of the material wire core m.
mmatch	Integer	[0,1]	Enables component mismatch.
procVar	Integer	[0,1]	Enables process variation.
procVal	Real	[0,1)	Process variation factor.

Table 5: Inductor Verilog-A Model Parameters

3.5.2 Equation and Internal Parameters

$$L = L_0(1 + \alpha(T - T_o) + \beta(T - T_o)^2 + \kappa(T - T_o)^3) \tag{42}$$

$$L_o = \frac{\mu_o \mu_r}{len} \pi r^2 \tag{43}$$

$$len = length(1 + procVar * procVal + mmatch * rand(seed)) \tag{44}$$

$$r = radius(1 + procVar * procVal + mmatch * rand(seed)) \tag{45}$$

3.6 NPN Transistor

3.6.1 External Parameters

Parameter	Type	Supported Values	Description
η	Real	(1,2)	Fitting factor.
I_{se}	Real	$(10^{-15},\ 10^{-12})$	Saturation current in Amperes.
β	Real	$(0,\ 1000)$	Beta in active mode.
V_{BE}	Real	$(0,\ 1000)$	Base Emitter Voltage.
β_{sat}	Real	$(0,\ 1000)$	Beta in saturation mode.
β_{rev}	Real	$(0,\ 1000)$	Beta in reverse mode.
mismatch	Integer	[0,1]	Enables component mismatch.
n	Integer	$[0,\ 10^{20}]$	Scaling factor
procVar	Integer	[0,1]	Enables process variation factor.
procVal	Real	[0,1)	Process variation factor.

Table 6: NPN Verilog-A Model Parameters

3.6.2 Equation and Internal Parameters

$$I_E = I_S(e^{\frac{V_{be}q}{\eta kT}} - 1) \tag{46}$$

$$V_{be} = V_t ln(n) + V_{BE} \tag{47}$$

$$I_E = I_C + I_B \tag{48}$$

$$I_{B-active} = \beta I_C \tag{49}$$

$$I_{B-saturation} = \beta_{sat} I_C \tag{50}$$

$$I_{B-reverse} = \beta_{rev} I_C \tag{51}$$

$$I_{SE} = (10^{-15})(1 + procVar * procVal) + mmatch * rand(seed) \tag{52}$$

3.7 PNP Transistor

3.7.1 External Parameters

Parameter	Type	Supported Values	Description
η	Real	(1,2)	Fitting factor.
I_{se}	Real	$(10^{-15},\ 10^{-12})$	Saturation current in Amperes.
β	Real	$(0,\ 1000)$	Beta in active mode.
V_{BE}	Real	$(0,\ 1000)$	Base Emitter Voltage.
β_{sat}	Real	$(0,\ 1000)$	Beta in saturation mode.
β_{rev}	Real	$(0,\ 1000)$	Beta in reverse mode.
mismatch	Integer	[0,1]	Enables component mismatch.
n	Integer	$[0,\ 10^{20}]$	Scaling factor
procVar	Integer	[0,1]	Enables process variation factor.
procVal	Real	[0,1)	Process variation factor.

Table 7: PNP Verilog-A Model Parameters

3.7.2 Equation and Internal Parameters

$$I_E = I_S(e^{\frac{V_{be}q}{\eta kT}} - 1) \tag{53}$$

$$V_{be} = V_t ln(n) + V_{BE} \tag{54}$$

$$I_E = I_C + I_B \tag{55}$$

$$I_{B-active} = \beta I_C \tag{56}$$

$$I_{B-saturation} = \beta_{sat} I_C \tag{57}$$

$$I_{B-reverse} = \beta_{rev} I_C \tag{58}$$

$$I_{SE} = (10^{-15})(1 + procVar * procVal) + mismatch * rand(seed) \tag{59}$$

3.8 Single Pole Amplifier

3.8.1 External Parameters

Parameter	Type	Supported Values	Description
f	Real	$(0, \infty)$	Pole frequency in Hertz.
A	Real	$(1, \infty)$	DC gain.
mismatch	Integer	[0,1]	Enables component mismatch.
procVar	Integer	[0,1]	Enables process variation factor.
procVal	Real	[0,1)	Process variation factor.

Table 8: Single Pole Amplifier Verilog-A Model Parameters

3.8.2 Equation and Internal Parameters

$$V_{out} = \frac{A}{1 + \omega j} V_{in},\ \omega = 2\pi f \tag{60}$$

3.9 Two-Pole Amplifier

3.9.1 External Parameters

Parameter	Type	Supported Values	Description
f_1	Real	$(0, \infty)$	First pole frequency in Hertz.
f_2	Real	$(0, \infty)$	Second pole frequency in Hertz.
A	Real	$(1, \infty)$	DC gain.
mismatch	Integer	[0,1]	Enables component mismatch.
procVar	Integer	[0,1]	Enables process variation factor.
procVal	Real	[0,1)	Process variation factor.

Table 9: Two-Pole Amplifier Verilog-A Model Parameters

3.9.2 Equation and Internal Parameters

$$V_{out} = \frac{A}{(1 + \omega_{p1} j)(1 + \omega_{p2} j)} V_{in},\ \omega_{p1,p2} = 2\pi f_{1,2} \tag{61}$$

3.10 Three-Pole Amplifier

3.10.1 External Parameters

Parameter	Type	Supported Values	Description
$f1$	Real	$(0, \infty)$	First pole frequency in Hertz.
$f2$	Real	$(0, \infty)$	Second pole frequency in Hertz.
$f3$	Real	$(0, \infty)$	Third pole frequency in Hertz.
A	Real	$(1, \infty)$	DC gain.
mismatch	Integer	[0,1]	Enables component mismatch.
procVar	Integer	[0,1]	Enables process variation factor.
procVal	Real	[0,1)	Process variation factor.

Table 10: Three-Pole Amplifier Verilog-A Model Parameters

3.10.2 Equation and Internal Parameters

$$V_{out} = \frac{A}{(1+\omega_{p1}j)(1+\omega_{p2}j)(1+\omega_{p3}j)} V_{in},\ \omega_{p1,p2,p3} = 2\pi f_{1,2,3} \tag{62}$$

4 Circuit Theory

4.1 RC

The RC circuit used to validate both the resistor and capacitor Verilog-A models contains a charge equation 63 and a discharge equation 68 for the voltage across the load capacitor V_C.

$$V_C = V_{in}(1 - e^{-t/\tau}),\ \tau = RC = t_r/5 \tag{63}$$

$$V_C = V_{in}e^{-t/\tau},\ \tau = RC = t_f/5 \tag{64}$$

$$t_{pd} = 10RC \tag{65}$$

4.2 RL

The RL circuit is used to validate both the resistor and inductor Verilog-A models. The equations below include a charge equation 66 and a discharge equation 67. The output voltage V_L is taken across the inductor of the RL circuit.

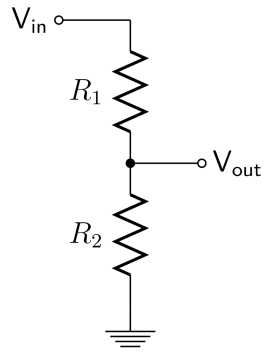
$$V_L = V_{in}(1 - e^{-t/\tau}),\ \tau = \frac{L}{R} = t_r/5 \tag{66}$$

$$V_L = V_{in}e^{-t/\tau},\ \tau = \frac{L}{R} = t_f/5 \tag{67}$$

$$t_{pd} = 10\frac{L}{R} \tag{68}$$

4.3 R-R Divider

The resistor-based voltage divider used to validate the Verilog-A resistor model uses equation 69 to characterize its output voltage.



$$V_{out} = \frac{R_2}{R_1 + R_2}V_{in} \tag{69}$$

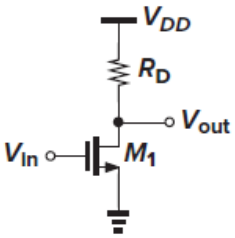
4.4 C-C Divider

The capacitor-based voltage divider used to validate the Verilog-A capacitor model uses equation 70 to characterize its output voltage.

$$V_{out} = \frac{C_1}{C_1 + C_2}V_{in} \tag{70}$$

4.5 Common Source Amplifier

The common-source amplifier used to validate the Verilog-A NMOS model uses equation 71 or 73 to characterize its output gain.



$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{R_S R_D \xi s^2 + (R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB}))s + 1} \tag{71}$$

$$\xi = C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB} \tag{72}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{-g_m R_D}{(1 + \frac{s}{\omega_{in}})(1 + \frac{s}{\omega_{out}})} \tag{73}$$

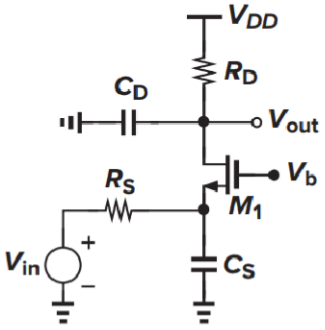
$$\omega_{in} = \frac{1}{R_S(C_{GS} + (1 + g_m R_D)C_{GD}} \tag{74}$$

$$\omega_{out} = \frac{1}{(R_D || (\frac{C_{GD}+C_{GS}}{C_{GD}} * \frac{1}{g_{m1}}))(C_{eq} + C_{DB})} \tag{75}$$

$$C_{eq} = C_{GD}C_{GS}/(C_{GD} + C_{GS}) \tag{76}$$

4.6 Common Gate Amplifier

The common gate amplifier will be used to validate the NMOS, Capacitor, and Resistor Verilog A models. The frequency response 77, and 84 will be used to validate results from simulation.

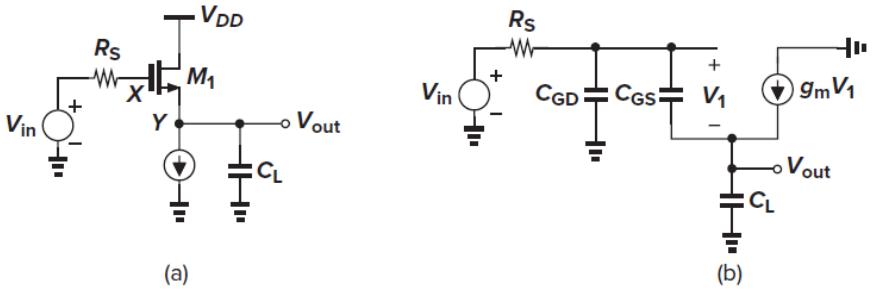


$$\frac{V_{out}}{V_{in}}(s) = \frac{(g_m + g_{mb})R_D}{(1 + (g_m + g_{mb}))R_s(1 + \frac{C_S}{g_m + g_{mb}R_S^{-}1}s)(1 + R_D C_D s)} \tag{77}$$

$$\omega_{p1} = \frac{1}{R_D C_S},\ \omega_{p2} = \frac{g_m + g_{mb} + R_S^{-1}}{C_s} \tag{78}$$

4.7 Source Follower Buffer

The source follower buffer used to validate the Verilog-A NMOS model uses equation 79 to characterize its output gain.



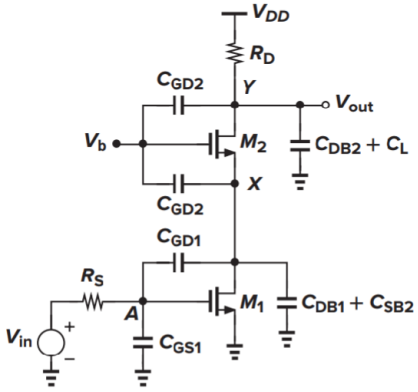
$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m + C_{GS}s}{R_S(C_{GS}C_L + C_{GS}C_{GD} + C_{GD}C_L)s^2 + (g_m R_S C_{GD} + C_L + C_{GS})s + g_m} \tag{79}$$

$$Z_{in} = \frac{1}{C_{GS}s} + \frac{1}{C_L s} + \frac{g_m}{C_{GS}C_L s^2} \tag{80}$$

$$Z_{out} = \frac{R_S C_{GS}s + 1}{g_m + C_{GS}s} \tag{81}$$

4.8 Common Source Cascode Amplifier

Verilog-A NMOS models will be used to implement the CS Cascode amplifier circuit topology. Equations 83, 82, and 84 will be used to validate the simulation results.



$$\omega_{py} = \frac{1}{R_D(C_{DB2} + C_L + C_{GS2}} \tag{82}$$

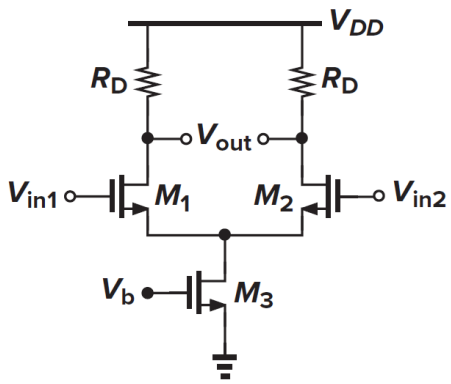
$$\omega_{px} = \frac{g_{m2} + g_{m1}}{2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2}} \tag{83}$$

$$\omega_{p1} = \frac{1}{R_D C_S},\ \omega_{p2} = \frac{g_m + g_{mb} + R_S^{-1}}{C_s} \tag{84}$$

w

4.9 Differential Pair with Passive Load

The differential pair amplifier with a passive load used to validate the Verilog-A NMOS and resistor models uses equation 85 to characterize its output gain. It has input and output holes, calculated in equations 86 and 87.



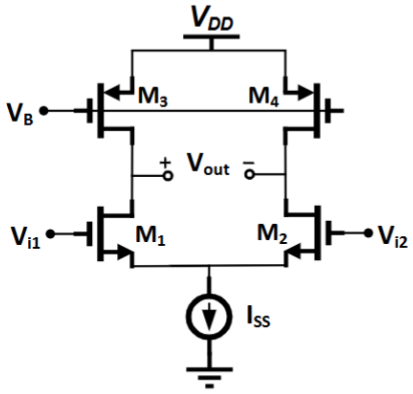
$$\frac{V_{od}}{V_{id}} = -g_m R_D \tag{85}$$

$$\omega_{in} = \frac{1}{R_S(C_{GS} + (1 + g_m R_D)C_{GD})} \tag{86}$$

$$\omega_{out} = \frac{1}{R_D || (\frac{C_{GD}+C_{GS}}{C_{GD}} * \frac{1}{g_{m1}})(C_{eq} + C_{DB})} \tag{87}$$

4.10 Differential Pair with Active Load

Verilog-A NMOS and PMOS models will be used to implement a differential pair with active load circuit topology. Equations 89, 90, and 88 will be used to validate the simulation results.



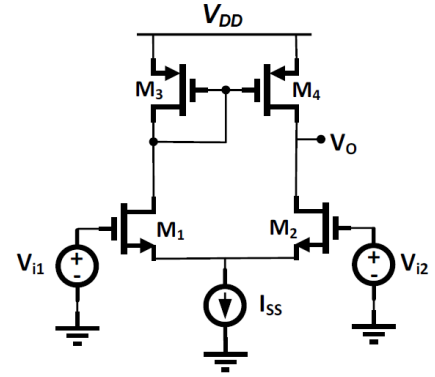
$$\frac{V_{od}}{V_{id}} = g_{m1} \times r_{on}||r_{op} \tag{88}$$

$$\omega_{in} = \frac{1}{R_S(C_{GS} + (1 + g_m R_D)C_{GD})} \tag{89}$$

$$\omega_{out} = \frac{1}{R_D||(\frac{C_{GD}+C_{GS}}{C_{GD}} * \frac{1}{g_{m1}})(C_{eq} + C_{DB})} \tag{90}$$

4.11 Differential Pair with Current Mirror

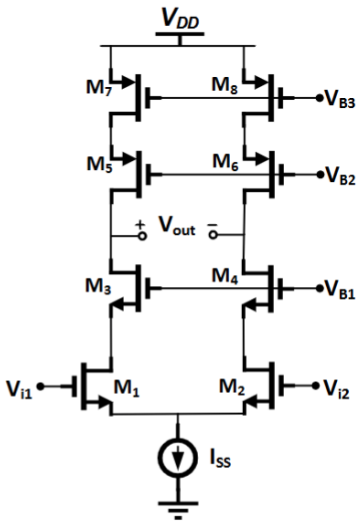
The differential pair amplifier with a current mirror used to validate the Verilog-A NMOS and PMOS models uses equation 91 to characterize its output gain.



$$\frac{V_{out}}{V_{in}} = \frac{g_{mN} r_{oN}(2g_{mP} + C_E s)r_{oP}}{2r_{oP}r_{oN}C_E C_L s^2 + ((2r_{oN} + r_{oP})C_E + r_{oP}(1 + 2g_{mP}r_{oN})C_L)s + 2g_{mP}(r_{oN} + r_{oP})} \tag{91}$$

4.12 Differential Pair with Cascode Driver and Load

The differential pair amplifier with a cascode driver and load will be used to validate the Verilog-A NMOS and PMOS models using equation 92 to characterize its output gain.



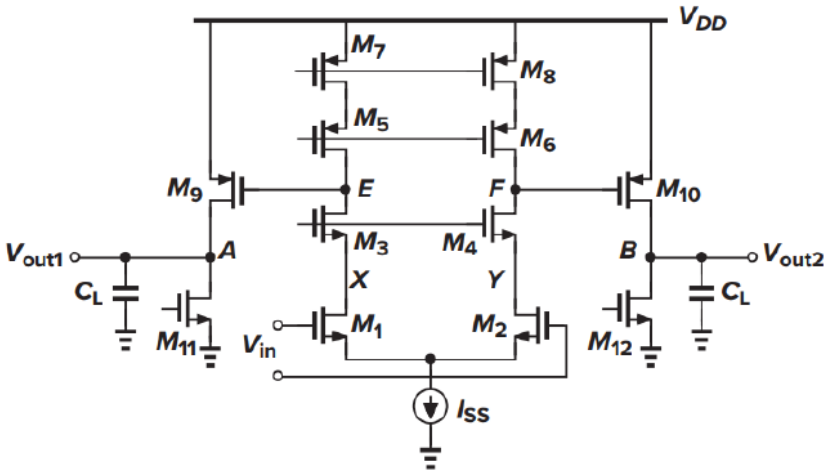
$$\frac{V_{od}}{V_{id}} \approx g_{m1}[(g_{m3}r_{o3}r_{o1})||(g_{m5}r_{o5}r_{o7})] \tag{92}$$

4.13 OpAmp with Two Poles

The single stage OpAmp, differential pair with passive load, amplifier will be used to validate the Verilog-A model OpAmp with Two Poles.

4.14 Two-Stage OpAmp with Three Poles

The two-stage opamp used to validate the Verilog-A OpAmp models has three poles. The following is a detailed transistor model; however, the validation model uses two OpAmps (1-pole and 2-pole versions).



4.15 1.25V Reference with MOSFET and BJT

The 1.25V reference voltage source, shown below, will be implemented using NMOS, PMOS, and PNP Verilog A models.