SCOMP External Memory Peripheral API

Peripheral Description

The SCOMP External Memory Peripheral provides up to 2^{16} or 65,536 16-bit words of dynamically configurable external memory for SCOMP. Four memory operation modes are available including normal, stack, queue, and circular buffer. The effective memory size of the peripheral can be changed at runtime. Read and write permissions as well as permission override passwords can be applied to any word in memory.

The functionality of each of the peripheral's five registers is described in detail below.

Chip Select (0x70)

On read operations, MEM_DATA[15:0] drives IO_DATA, providing SCOMP with the data at the current location of the read pointer in accordance with read access control restrictions at the target address.

> In stack mode, both the read and write pointer will be auto-decremented if the stack is not empty.

> In queue mode, only the read pointer will be auto-incremented or wrapped around if the queue is not empty.

> In circular buffer mode, the read pointer will be auto-incremented or wrapped around if the circular buffer is not empty.

On write operations, MEM_DATA[15:0] accepts any 16-bit word of data and its contents are written to memory in accordance with write access control restrictions at the target address.

> In stack mode, both the read and write pointer will be auto-incremented if the stack is not full.

> In queue mode, only the write pointer will be auto-incremented or wrapped around if the queue is not full.

> In circular buffer mode, the write pointer will be auto-incremented or wrapped around. If the circular buffer is full, the read pointer will also be auto-incremented or wrapped around.

Memory Mode (0x71)

The values corresponding to each memory operation mode are as follows: 0b00=Normal, 0b01=Stack, 0b10=Queue, 0b11=Circular buffer.

On read operations, MODE[1:0] drives IO_DATA, providing SCOMP with the numerical identifier of the current memory operation mode.

On write operations, MODE[1:0] accepts the bottom 2 bits of the IO_DATA bus, updates the peripheral's memory operation mode, and resets both the read and write pointers to address 0.

The peripheral defaults to normal mode.

Memory contents are not cleared on mode change.

Memory Address (0x72)

On read operations, MEM_ADDR[15:0] drives IO_DATA, providing SCOMP with the current write address of the external memory peripheral.

On write operations, MEM_ADDR[15:0] accepts any 16-bit address and sets the memory pointer when the peripheral is operating in normal mode. Manual memory pointer manipulation is restricted when the peripheral is operating in stack, queue, and circular buffer modes.

Metadata (0x73)

On read operations, the cached metadata including memory availability (AVAIL), read permissions (RP), and write permissions (WP) but excluding the permission override password (PERMISSION_OVERRIDE_PWD[15..3]) will drive IO_DATA, providing SCOMP with the metadata currently being used for write operations.

On write operations, any data sent to the metadata register is cached* and used as metadata for data written into memory afterward. The metadata register is formatted with the permission override password (PERMISSION_OVERRIDE_PWD[15:3]) in the first 13 bits, followed by the availability of the memory address (AVAIL) where 0=Available and 1=Unavailable, followed by the read permissions of the word in memory (RP) where 0=Restricted and 1=Unrestricted, and finally the write permissions of the word in memory (WP) where 0=Restricted and 1=Unrestricted.

The peripheral defaults to the following metadata settings: 0b111 denoting unavailable, unrestricted read, unrestricted write.

When the peripheral is operating in stack, queue, or circular buffer mode, write permissions are ignored to guarantee no unintended loss of input data.

> * All components of metadata will be cached at least until the next read or write operation. For security purposes, the permission override password is wiped after every read or write operation. Availability, read permissions, and write permissions are cached indefinitely or until new values are provided.

Memory Size (0x74)

EFF_MEM_SIZE[15:0] accepts any 16-bit value and sets the peripheral's effective memory size (maximum of 65,536 words). Attempted access beyond the effective memory size is restricted.

The peripheral defaults to its maximum memory size of 2^{16} or 65,536 words.

Peripheral Register Map

Address	Register Name	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0x70	Chip Select	MEM_DATA[15:0]															
0x71	Memory Mode	-	-	-	-	-	-	-	-	-	-	-	-	-	-	MODE[1:0]	
0x72	Memory Address	MEM_ADDR[15:0]															
0x73	Metadata	PERMISSION_OVERRIDE_PWD[15:3]													AVAIL	RP	WP
0x74	Memory Size	EFF_MEM_SIZE[15:0]															