Write the pipeline timeline for a 2-wide out-of-order superscalar processor with one ALU/Branch EX unit and one Load/Store EX unit.
Assume split instruction and data memory, full data forwarding, and perfect branch prediction (with both BHT and BTB).
Assume all instructions are already dispatched to the instruction queue (instructions will start from the EX stage).
Assume initially s0 is renamed to p10 and s1 is renamed to p11 and that both operands are ready. Other operands are not ready.

This is the code:

```
lw t0, 0(s0)
add t1, t0, t1
addi t0, s0, 1
sw t0, 0(s0)
beq t1, t0, loop
lw t0, 0(s0)
```

Start by renaming registers to physical registers and then draw the timeline. Physical registers are allocated in the order of: p0, p1, p2, p3, p4, …

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
lw p0, 0(p10)	EX	MEM	WB																						
add p1, p0, p11			EX	MEM	WB																				
addi p2, p10, 1	EX	MEM	WB																						
sw p2, 0(p10)		EX	MEM	WB																					
beq p1, p2, loop				EX	MEM	WB																			
lw p3, 0(p10)			EX	MEM	WB																				

* All instructions have already been dispatched so there will only be EX, MEM, WB stages (no IF or ID).
* When there is a choice, the scheduler always prioritizes older instructions.