Write the pipeline timeline for a 1-wide processor with an optimized 5-stage pipeline.
Assume split instruction and data memory, full data forwarding, and perfect branch prediction (with both BHT and BTB)

| Cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **lw t0, 0(s0)** | | | | | | | | | | | | | | | | | | | | | | | | | |
| **add t1, t0, t1** | | | | | | | | | | | | | | | | | | | | | | | | | |
| **addi t0, s0, 1** | | | | | | | | | | | | | | | | | | | | | | | | | |
| **sw t0, 0(s0)** | | | | | | | | | | | | | | | | | | | | | | | | | |
| **beq t1, t0, loop** | | | | | | | | | | | | | | | | | | | | | | | | | |
| **lw t0, 0(s0)** | | | | | | | | | | | | | | | | | | | | | | | | | |

* Can be simulated using 1-wide-opt.conf and midterm_1_review.tr trace.