Write the pipeline timeline for a 2-wide VLIW processor with one ALU/Branch operation slot and one Load/Store operation slot.
Assume split instruction and data memory, full data forwarding, and perfect branch prediction (with both BHT and BTB).

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
lw t0, 0(s1)	IF	ID	EX	MEM	WB																				
addi t0, t0, 4			IF	ID	EX	MEM	WB																		
addi t1, t1, 4				IF	ID	EX	MEM	WB																	
addi t2, t1, 4					IF	ID	EX	MEM	WB																

* Can be simulated using the 2-wide-opt.conf and midterm_1_review.tr trace. The result is going be for an in-order superscalar but the only difference for a VLIW is that instead of the hazard detection unit inserting bubbles, the compiler schedules instructions so that there are no hazards.

Write the list of VLIW instructions based on the above schedule (note: you may have less than 10 instructions).

Insts	ALU/Branch	Load/Store
1	nop	lw t0, 0(s1)
2	nop	nop
3	addi t0, t0, 4	nop
4	addi t1, t1, 4	nop
5	addi t2, t1, 4	nop
6		
7		
8		
9		
10		