Write the pipeline timeline for a 2-wide VLIW processor with one ALU/Branch operation slot and one Load/Store operation slot.

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
lw t0, 8(s0)																									
addi t0, t0, 20																									
sw t0, 8(s0)																									
lw t0, 12(s0)																									
sw t0, 16(s0)																									
beq t0, s0, loop																									
lw t0, 8(s0)																									

Write the list of VLIW instructions based on the above schedule (note: you may have less than 10 instructions).

Insts	ALU/Branch	Load/Store
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		