Given the following instructions and timeline, list all the hazards and their types.
Assume unified memory, no data forwarding, and no branch prediction.

| Cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **lw t0, 0(s0)** | IF | ID | EX | MEM | WB | | | | | | | | | | | | | | | | | | | | |
| **add t1, t0, t1** | | IF | ID | EX | MEM | WB | | | | | | | | | | | | | | | | | | | |
| **addi t0, s0, 1** | | | IF | ID | EX | MEM | WB | | | | | | | | | | | | | | | | | | |
| **sw t0, 0(s0)** | | | | IF | ID | EX | MEM | WB | | | | | | | | | | | | | | | | | |
| **beq t1, t0, loop** | | | | | IF | ID | EX | MEM | WB | | | | | | | | | | | | | | | | |
| **lw t0, 0(s0)** | | | | | | IF | ID | EX | MEM | WB | | | | | | | | | | | | | | | |

* Structural hazard between lw and sw due to conflict in memory read port
* Data hazard between lw and add
* Data hazard between addi and sw
* Data hazard between add and beq
* Data hazard between addi and beq
* Control hazard between beq and lw