Assume all instructions are already dispatched to the instruction queue (instructions will start from the EX stage).
Assume initially s0 is renamed to p10 and that p10 is ready. Other operands are not ready.

This is the code:

lw t0, 8(s0)
addi t0, t0, 20
sw t0, 8(s0)
lw t0, 12(s0)
sw t0, 16(s0)
beq t0, s0, loop
lw t0, 8(s0)

Start by renaming registers to physical registers and then draw the timeline. Physical registers are allocated in the order of: p0, p1, p2, p3, p4, …

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

* All instructions have already been dispatched so there will only be EX, MEM, WB stages (no IF or ID).
* When there is a choice, the scheduler always prioritizes older instructions.