Write the pipeline timeline for a 1-wide processor with a classic 5-stage pipeline: IF, ID, EX, MEM, WB.
Assume unified memory, no data forwarding, and no branch prediction.

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
lw t0, 0(s0)	IF	ID	EX	MEM	WB																				
add t1, t0, t1		IF	-	-	-	ID	EX	MEM	WB																
addi t0, s0, 1						IF	ID	EX	MEM	WB															
sw t0, 0(s0)							IF	-	-	-	ID	EX	MEM	WB											
beq t1, t0, loop											IF	ID	EX	MEM	WB										
lw t0, 0(s0)												-	-	IF	ID	EX	MEM	WB							

* Can be simulated using 1-wide.conf and midterm_1_review.tr trace.