

ASM1182e Data Sheet

PCI Express Packet Switch

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Environmentally hazardous materials are not used in this product.



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Revision History

Rev.	Date	Description		
0.1	Dec. 14, 2012	Initial Release		
0.2	May. 8, 2013	Modify core power range		
1.0	Oct. 9, 2013	Change version to 1.0		
1.1	Dec. 4, 2013	Add Power on/off sequence		
1.2	Sep 18, 2014	Add Chip temperature calculation, remove power off sequence		
1.3	May 14, 2015	Add Top marking		
1.4	Nov 6, 2015	Add PCIe differential clock range		
1.5	Dec. 18, 2019	 Add SMbus slave address information Add Strapping pin timing requirement 		



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1. General Description

ASM1182e, PCI express packet switch, 1 PCIe x1 Gen2 upstream port to 2 PCIe x 1 Gen2 downstream ports, enable users to extend PCIe ports on mother board or embedded system. PCIe interface of ASM1182e is PCIe Base SPEC 2.0 compliance.

2. Features

General Features

- Standard Compliant
 - > PCI express base SPEC 2.0 and backward compatible with SEPC 1.1 & 1.0a
 - > PCI Power management SPEC 1.2
- Port configuration
 - > 1 PCle x1 lane Gen2 upstream port to 2 PCle x1 lane Gen2 downstream ports
- PCIe power management
 - > Link state L0, L0s, L1, L2/L3 Ready and L3
 - > device state D0, D3 hot
- Short latency delay
- Integrate 100MHz PCIe differential clock buffer,no extra clock buffer needed.
- Support I2C interface for debug usage
- 7 x 7 QFN48 RoHS package

3. Package Type

♦ 7x7 QFN48



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4. Functional Diagram

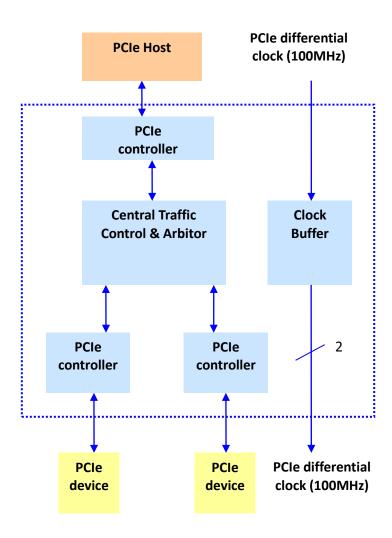


Figure 1: Functional Diagram



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5. Pinout Diagrams

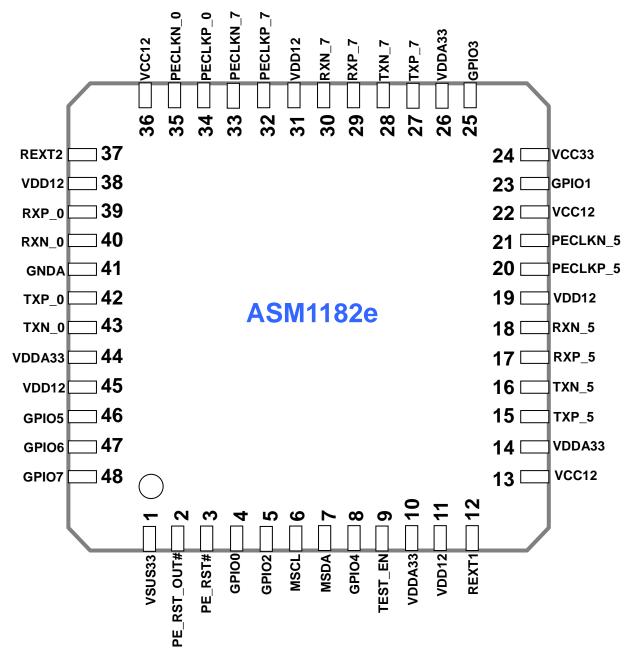


Figure 2: ASM1182e Pinout



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6. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
0	Output pin
I/O	Bi-directional pin
Р	Power pin
G	Ground pin
OD	Open Drain

N Pin I/O Descriptions					
N	Number	1/0	Descriptions		
Upstream Signals					
REXT1	12	I	External Resistor for PCIE PHY. External resistor should be		
KEXII		1	connected this pin to ground.		
TXP_0	42	0	CIE Upstream TX+ signal		
TXN_0	43	0	PCIE Upstream TX- signal		
RXP_0	39	I	PCIE Upstream RX+ signal		
RXN_0	40	I	PCIE Upstream RX- signal		
PECLKP_0	34	I	PCIE 100MHz Clock input+		
PECLKN_0	35	I	PCIE 100MHz Clock input-		
			Downstream Signals		
REXT2	37	0	External Resistor for PCIE PHY. External resistor should be		
			connected this pin to ground.		
TXP_5	15	0	PCIE downstream lane5 TX+ signal (logic device 7)		
TXN_5	16	0	PCIE downstream lane5 TX- signal (logic device 7)		
RXP_5	17	I	PCIE downstream lane5 RX+ signal (logic device 7)		
RXN_5	18	I	PCIE downstream lane5 RX- signal (logic device 7)		
TXP_7	27	0	PCIE downstream lane7 TX+ signal (logic device 3)		
TXN_7	28	0	CIE downstream lane7 TX- signal (logic device 3)		
RXP_7	29	I	PCIE downstream lane7 RX+ signal (logic device 3)		
RXN_7	30	I	PCIE downstream lane7 RX- signal (logic device 3)		
PECLKP_5	20	0	PCIE 100MHz Clock output+		
PECLKN_5	21	0	PCIE 100MHz Clock output-		
PECLKP_7	32	0	PCIE 100MHz Clock output+		
PECLKN_7 33 O PCIE 100MHz Clock output-					
			MISC Signals		
PE_RST#	3	I	Chip global reset		
PE_RST_OUT#	2	0	PCIE Reset for downstream port		
MSCL	6	I/O	SMBus/I2C clock signal		
MSDA	7	I/O	SMBus/I2C data signal		
TEST_EN	9	I	Test mode enable, connect to GND		
GPIO0	4	I/O	General purpose input/output 0		
GPIO1	23	I/O	General purpose input/output 1		
GPIO2	5	I/O	General purpose input/output 2		
GPIO3	25	I/O	General purpose input/output 3		
GPIO4	8	I/O	General purpose input/output 4		
GPIO5	46	I/O	General purpose input/output 5		





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N	Pin Number	I/O	Descriptions	
GPIO6	47	I/O	General purpose input/output 6	
GPIO7	48	I/O	General purpose input/output 7	
			Power	
VSUS33	1	P	3.3V suspend power	
VDDA33	10,14,26,44	P	3.3V Power Input, for PCIE PHY	
VDD12	11,19,31,38 ,45	P	1.2V Power Input, for PCIE PHY	
VCC33	24	P	3.3V Power Input, for PAD	
VCC12	13,22,36	P	1.2V Power Input for Core	
GNDA	41	G	Ground	



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7. Function Description

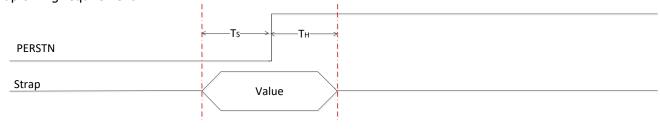
7.1. Strapping Table

Pins	Function	Default (internal pull)
GPIO0	Clock buffer mode setting. 0: PLL mode; 1: bypass mode	Pull up
GPIO1	Clock buffer termination enable. 0: disable; 1: enable	Pull up
GPIO2	Reserved for test mode.	Pull up
GPIO3	Reserved for ASM1187e	Pull up
GPIO4	SMBus enable. Please refer to below SMBus/I2C table	Pull up
GPIO5	SMBus address[0].	Pull up
GPIO6	SMBus address[1].	Pull up
GPIO7	SMBus address[2].	Pull up
MSCL	I2C enable. Please refer to below SMBus/I2C table.	Pull up

SMBus/I2C table

GPIO4 (SMBus enable)	MSCL (I2C enable)	Function
0	0	(MSCL, MSDA) is no function
0	1	(MSCL, MSDA) is I2C, connected to a EEPROM, chip is master
1	0	(MSCL, MSDA) is SMBus, chip is salve
1	1	(MSCL, MSDA) is SMBus, chip is salve

Strap timing requirement



	Parameter	Min	Max	Unit
Ts	Setup time for capture	1		ms
Тн	Hold time for capture	1		ms

7.2 SMBus Address

GPIO7, GPIO6, GPIO5 (SM bus address select)	SM bus address
3'b000	0x6C
3'b001	0x6A
3'b010	0x7C
3'b011	0x7A
3′b100	0x8C
3'b101	0x8A
3'b110	0x9C
3'b111	0x90



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8 Electrical Characteristics

8.1 Absolute Maximum Ratings

O12 Absolute Maximum Ratings				
Parameter	Range	Units		
Power Supply for 1.2V	-0.5~+1.6	V		
Power Supply for 3.3V	-0.5~+4.5	V		
DC Input Voltage	-0.5~+4.5	V		
Output Voltage	-0.5~+4.5	V		
Storage Temperature	-65~150	₀ C		
HBM ESD	+/-2	KV		
MM ESD	+/-200	V		

8.2 Recommand Operation Condition

Symbols	Parameter	Min.	Тур.	Max.	Units
V CC33	3.3V IO Power Supply	3.0	3.3	3.6	V
V DDA33	PCIE 3.3V Analog Power Supply	3.0	3.3	3.6	V
V CC12	1.2V Core Power Supply	1.0	1.15	1.3	V
V _{DD12}	PCIE 1.2V Power Supply	1.0	1.15	1.3	V
V sus33	3.3V Suspend IO Power Supply	3.0	3.3	3.7	V
Tc	Operating Case Temperature		25	95	0C
T ɔ	Operating Junction Temperature	0	25	120	0C

8.3 DC Electrical Characteristics for GPIO/RST Pins (Temperature = 45°C)

Symbols	Parameter	Min.	Тур.	Max.	Units
V IH	Input High Level				V
V IL	Input Low Level			0.8	V
V HYS	Input Hysteresis	0.57	0.6	0.65	V
V TH-L2H	VTH of Schmitt Trigger low to high	1.38		1.8	V
V TH-H2L	VTH of Schmitt Trigger high to low	0.82		1.15	V
R up	Internal Pull-up resistance while Vin=0V	67	98.3	140	ΚΩ
	Internal Pull-up resistance while Vin=VCCH/2 V	37.85	55	77	ΚΩ
In	Input pull-up leakage current while Vin=0V	21.4	33.6	53.7	uA
	Input pull-up leakage current while Vin=VCCH/2 V	19.5	30	47.6	uA
V он	Output High Voltage	2.64			V
V oL	Output Low Voltage			0.66	V
Іон	Driving Current of Output High		8		mA
IoL	Driving Current of Output Low		8		mA

8.4 Reference Resistor Requirement

Parameter Parameter	Value	Units
REXT* External Reference Resistor	12.1K+/-1%	Ohm





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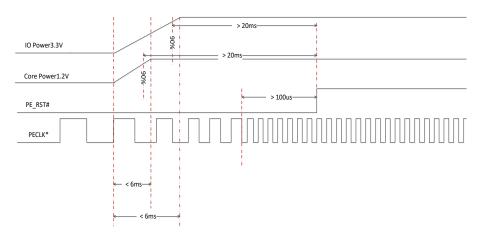
8.5 PCI Express Differential Reference Clock Input Ranges

6.5 PCI Express Differential Reference Clock input Ranges						
Symbols	Parameter	Min	Тур	Max	Unit	Remark
FIN-DIFF	The input frequency is 100 MHz + 300 ppm and max. – 5000 including SSC-dictated variations Differential input frequency		100		MHz	
	Rising Edge Rate	0.6		4.0	V/ns	
	Falling Edge Rate	0.6		4.0	V/ns	
V IH	Differential Input High Voltage	150			mV	
VIL	Differential Input Low Voltage			-150	mV	
Vcross	Absolute crossing point voltage	250		550	mV	
VCROSS-DELTA	Variation of VCROSS over all rising			140	mV	
V _{RB}	Ring-back Voltage Margin	-100		100	mV	
TSTABLE	Time before VRB is allowed	500			ps	
TPERIOD-AVG	Average Clock Period Accuracy	-300		2800	ppm	
TPERIOD-ABS	Absolute Period (including litter and			10.203	ns	
Tcc-jitter	Cycle to Cycle Jitter			150	ps	
VMAX	Absolute Max input voltage			1.15	V	
VMIN	Absolute Min input voltage			-0.3	V	
	Duty Cycle	4 0		60	%	
R/F Matching	Rising edge rate (REFCLK+) to Falling edge rate (REFCLK-) matching			20	%	
Zc-dc	Clock source DC impedance	40		60	Ω	



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8.6 Power On/Off Sequence



Symbols	Parameter		Max	Unit	Remark
t ₁	Power ramp up to 100%		6	ms	
t ₂	Power on 90% ready to PE_RST# deassertion			ms	
t ₃	PCI Express Reference stable Clock before PE_RST# deassertion	100		us	

8.7 Chip Temperature(Tj, Tc) Calculation

Symbol	Parameter	How to get?
Ta	Ambient temperature	Measure temperature around chip
Tj	Operating junction temperature	Tj = ⊖ja * power + Ta
Tc	Operating case temperature	Tc = Tj - Ψjt * power
⊖ja	Junction to Ambient thermal resistance	Provided by package vendor, for QFN48, it's 30.6
Ψjt	Junction to top thermal characterization	Provided by package vendor, for QFN48, it's 0.1
Power	Chip power consumption	Measure chip power consumption

- > Thermal test board condition, please refer to JEDEC JESD51-5
- > Thermal Test Method Environmental Conditions refer JESD51-2
- Example: If chip power consumption is 0.8W; Ta=40^oC

Tj = 30.6 * 0.8 + 40 = 64.48°C

Tc = 64.48 - 0.1 * 0.8 = 64.4°C



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9 Power Consumption

	Test Item	Test State	Min.	Тур.	Max.	
I 33	Total Consumption Current for 3.3V Power	L0		92	94	mA
		Idle		92	94	mA
		Suspend		0.05	0.05	mA
I 12	Total Consumption Current for 1.05V Power	L0		470	480	mA
		Idle		450	460	mA
		Suspend		0	0	mA
	Tabal Danier	L0		800	808	mW
	Total Power Consumption	Idle		775	786	mW
		Suspend		0.16	0.16	mW



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10 Package Information

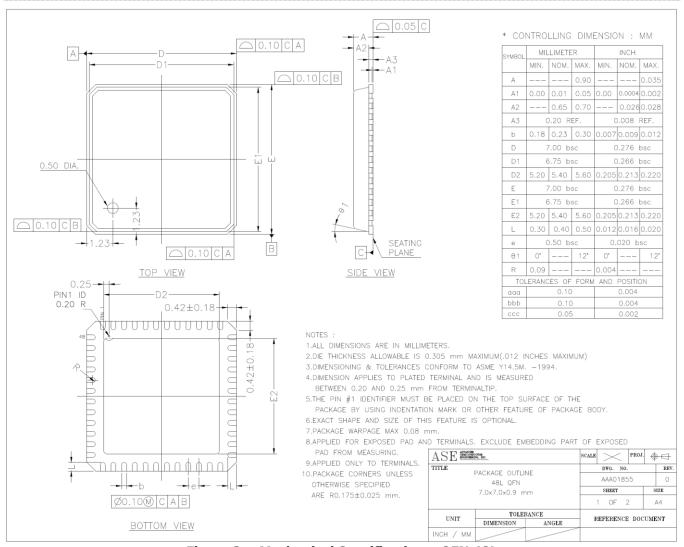


Figure 3: Mechanical Specification – QFN 48L



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11 Top marking Information

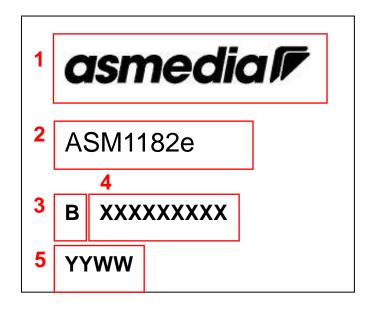


Figure 4: Top marking of ASM1182e

1. asmedia: ASMedia Logo

2. ASM1182e: Product Name

3. B: Version of ASMedia Logo

4. XXXXXXXXX: Serial No. Reserved for Vendor

5. YYWW: Date Code