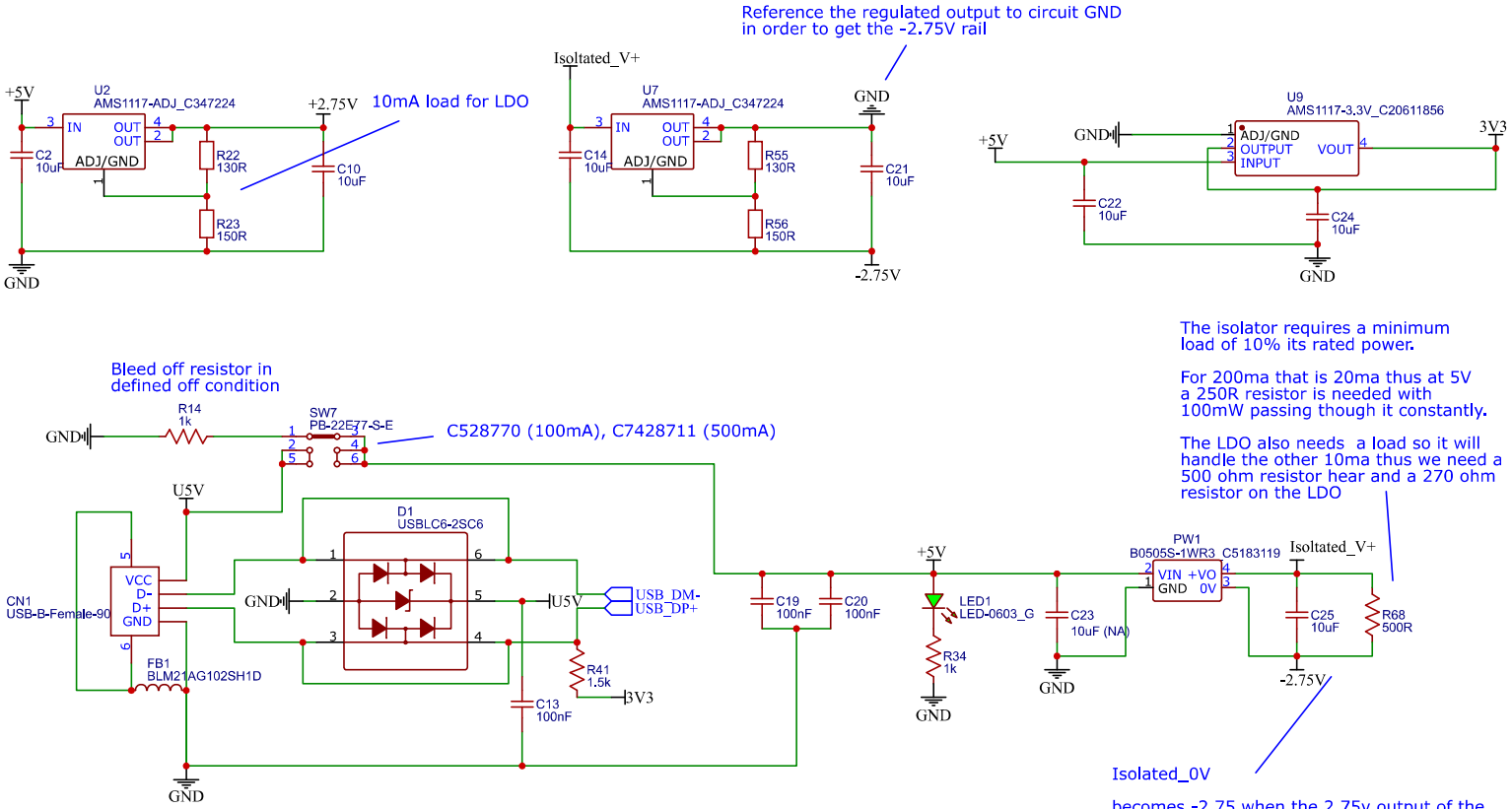

TITLE: Sheet_1		REV: 1.0
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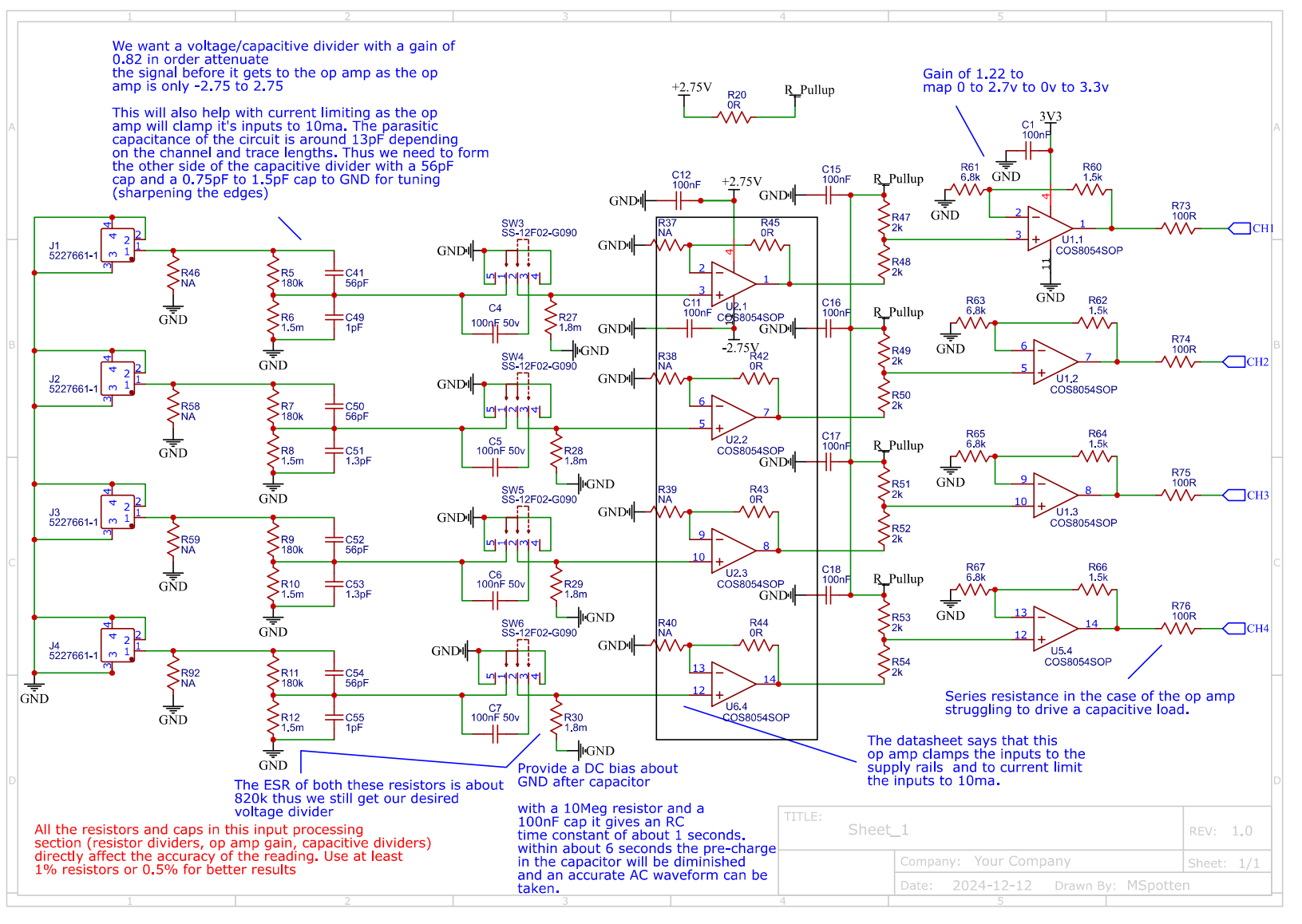
We want a voltage/capacitive divider with a gain of 0.82 in order attenuate the signal before it gets to the op amp as the op amp is only -2.75 to 2.75
This will also help with current limiting as the op amp will clamp it's inputs to 10ma. The parasitic capacitance of the circuit is around 13pF depending on the channel and trace lengths. Thus we need to form the other side of the capacitive divider with a 56pF cap and a 0.75pF to 1.5pF cap to GND for tuning (sharpening the edges)
Gain of 1.22 to map 0 to 2.7v to 0v to 3.3v
+2.75V
R20 0R
R_Pullup
3V3
C1 100nF
J1 5227661-1
J2 5227661-1
J3 5227661-1
J4 5227661-1
R46 NA
R58 NA
R59 NA
R92 NA
R5 180k
R6 1.5m
R7 180k
R8 1.5m
R9 180k
R10 1.5m
R11 180k
R12 1.5m
C41 56pF
C49 1pF
C50 56pF
C51 1.3pF
C52 56pF
C53 1.3pF
C54 56pF
C55 1pF
GND
SW3 SS-12F02-G090
SW4 SS-12F02-G090
SW5 SS-12F02-G090
SW6 SS-12F02-G090
C4 100nF 50v
C5 100nF 50v
C6 100nF 50v
C7 100nF 50v
R27 1.8m
R28 1.8m
R29 1.8m
R30 1.8m
C12 100nF
C11 100nF
-2.75V
R37 NA
R38 NA
R39 NA
R40 NA
R45 0R
R42 0R
R43 0R
R44 0R
U2.1 COS8054SOP
U2.2 COS8054SOP
U2.3 COS8054SOP
U6.4 COS8054SOP
C15 100nF
C16 100nF
C17 100nF
C18 100nF
R47 2k
R48 2k
R49 2k
R50 2k
R51 2k
R52 2k
R53 2k
R54 2k
R61 6.8k
R60 1.5k
R63 6.8k
R62 1.5k
R65 6.8k
R64 1.5k
R67 6.8k
R66 1.5k
U1.1 COS8054SOP
U1.2 COS8054SOP
U1.3 COS8054SOP
U5.4 COS8054SOP
R73 100R
R74 100R
R75 100R
R76 100R
CH1
CH2
CH3
CH4
Series resistance in the case of the op amp struggling to drive a capacitive load.
The datasheet says that this op amp clamps the inputs to the supply rails and to current limit the inputs to 10ma.
The ESR of both these resistors is about 820k thus we still get our desired voltage divider
Provide a DC bias about GND after capacitor
with a 10Meg resistor and a 100nF cap it gives an RC time constant of about 1 seconds. within about 6 seconds the pre-charge in the capacitor will be diminished and an accurate AC waveform can be taken.
All the resistors and caps in this input processing section (resistor dividers, op amp gain, capacitive dividers) directly affect the accuracy of the reading. Use at least 1% resistors or 0.5% for better results
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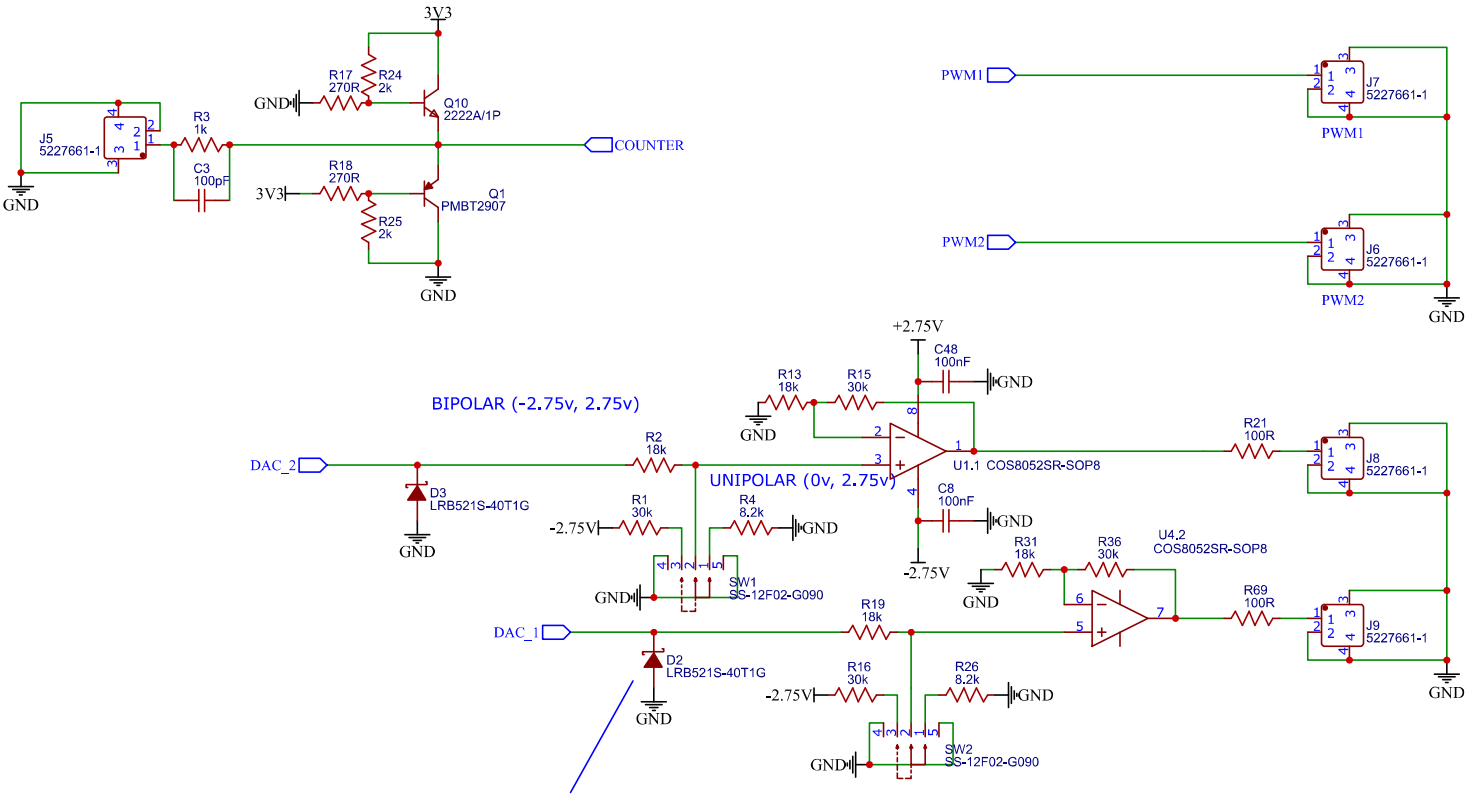

Schottky Diodes for protecting
The STM32 in the condition that
the switch is in Bipolar Mode and
the stm32 ADC is in an off (high
impedance) state. In this state
the negative voltage on the bottom side
of the resistor divider in bipolar mode
could cause a negative voltage at the
stm32 input

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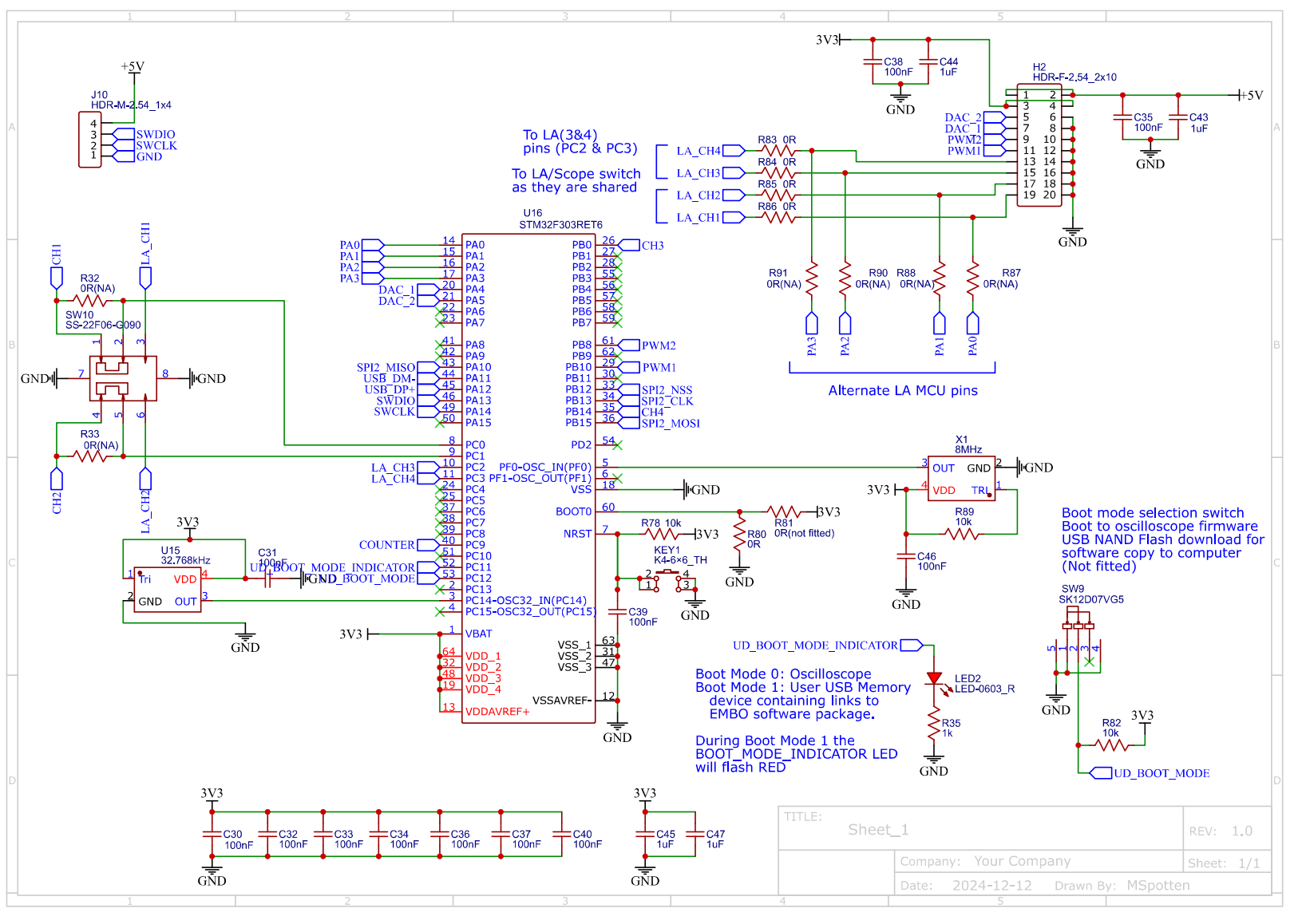
+5V
J10
HDR-M-2.54_1x4
SWDIO
SWCLK
GND
3V3
C38
100nF
C44
1uF
H2
HDR-F-2.54_2x10
C35
100nF
C43
1uF
DAC_2
DAC_1
PWM2
PWM1
To LA(3&4)
pins (PC2 & PC3)
To LA/Scope switch
as they are shared
LA_CH4
LA_CH3
LA_CH2
LA_CH1
R83 0R
R84 0R
R85 0R
R86 0R
R91
0R(NA)
R90
0R(NA)
R88
0R(NA)
R87
0R(NA)
PA3
PA2
PA1
PA0
Alternate LA MCU pins
U16
STM32F303RET6
CH1
LA_CH1
R32
0R(NA)
SW10
SS-22F06-G090
R33
0R(NA)
CH2
LA_CH2
PA0
PA1
PA2
PA3
DAC_1
DAC_2
SPI2_MISO
USB_DM-
USB_DP+
SWDIO
SWCLK
COUNTER
LA_CH3
LA_CH4
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PB8
PB9
PB10
PB11
PB12
PB13
PB14
PB15
PD2
CH3
PWM2
PWM1
SPI2_NSS
SPI2_CLK
CH4
SPI2_MOSI
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
PC12
PC13
PC14-OSC32_IN(PC14)
PC15-OSC32_OUT(PC15)
PF0-OSC_IN(PF0)
PF1-OSC_OUT(PF1)
VSS
BOOT0
NRST
VBAT
VDD_1
VDD_2
VDD_3
VDD_4
VSS_1
VSS_2
VSS_3
VSSAVREF-
VDDAVREF+
X1
8MHz
R89
10k
C46
100nF
R78 10k
R80
0R
R81
0R(not fitted)
KEY1
K4-6×6_TH
C39
100nF
U15
32.768kHz
C31
100nF
UD_BOOT_MODE_INDICATOR
GND_BOOT_MODE
Boot mode selection switch
Boot to oscilloscope firmware
USB NAND Flash download for
software copy to computer
(Not fitted)
SW9
SK12D07VG5
UD_BOOT_MODE
R82
10k
Boot Mode 0: Oscilloscope
Boot Mode 1: User USB Memory
device containing links to
EMBO software package.
During Boot Mode 1 the
BOOT_MODE_INDICATOR LED
will flash RED
LED2
LED-0603_R
R35
1k
C30
100nF
C32
100nF
C33
100nF
C34
100nF
C36
100nF
C37
100nF
C40
100nF
C45
1uF
C47
1uF
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