Solid State Digitally Resettable and Programmable Circuit Breaker

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MAD VLSI Final project, Fall 2014

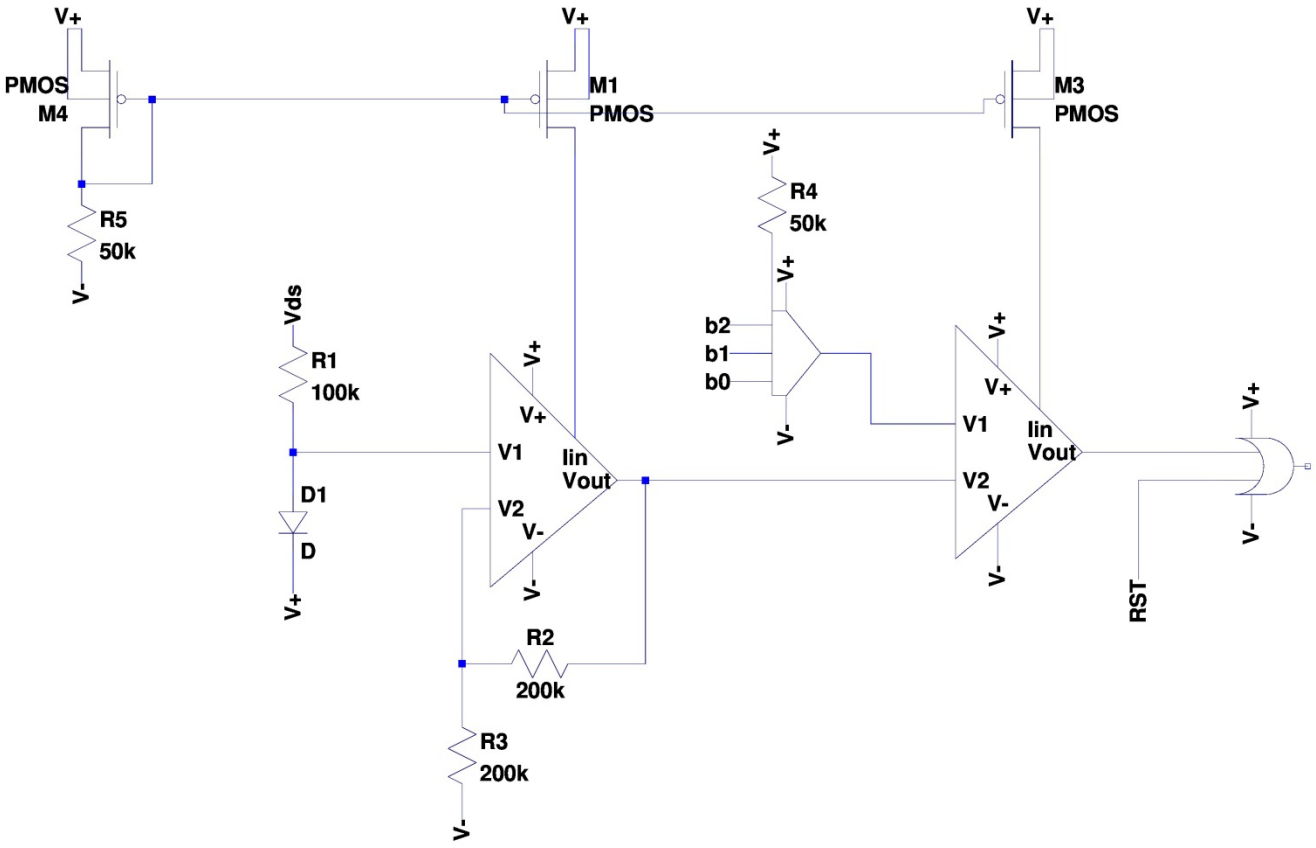
Our intention:

We want to create a chip that preforms the logic necessary to shut off a MOSFET in an over current condition, acting like a digitally resettable circuit breaker. It utilizes the fact that a low side NMOS power FET operating in the ohmic region has a fairly linear relationship between drain voltage and drain-source current. Our chip compares this voltage to a digitally programmable set point, and provides the logic signal to drive the gate of the FET. It also has a digital reset pin that allows the FET to be turned back on after tripping.

Circuit Design:

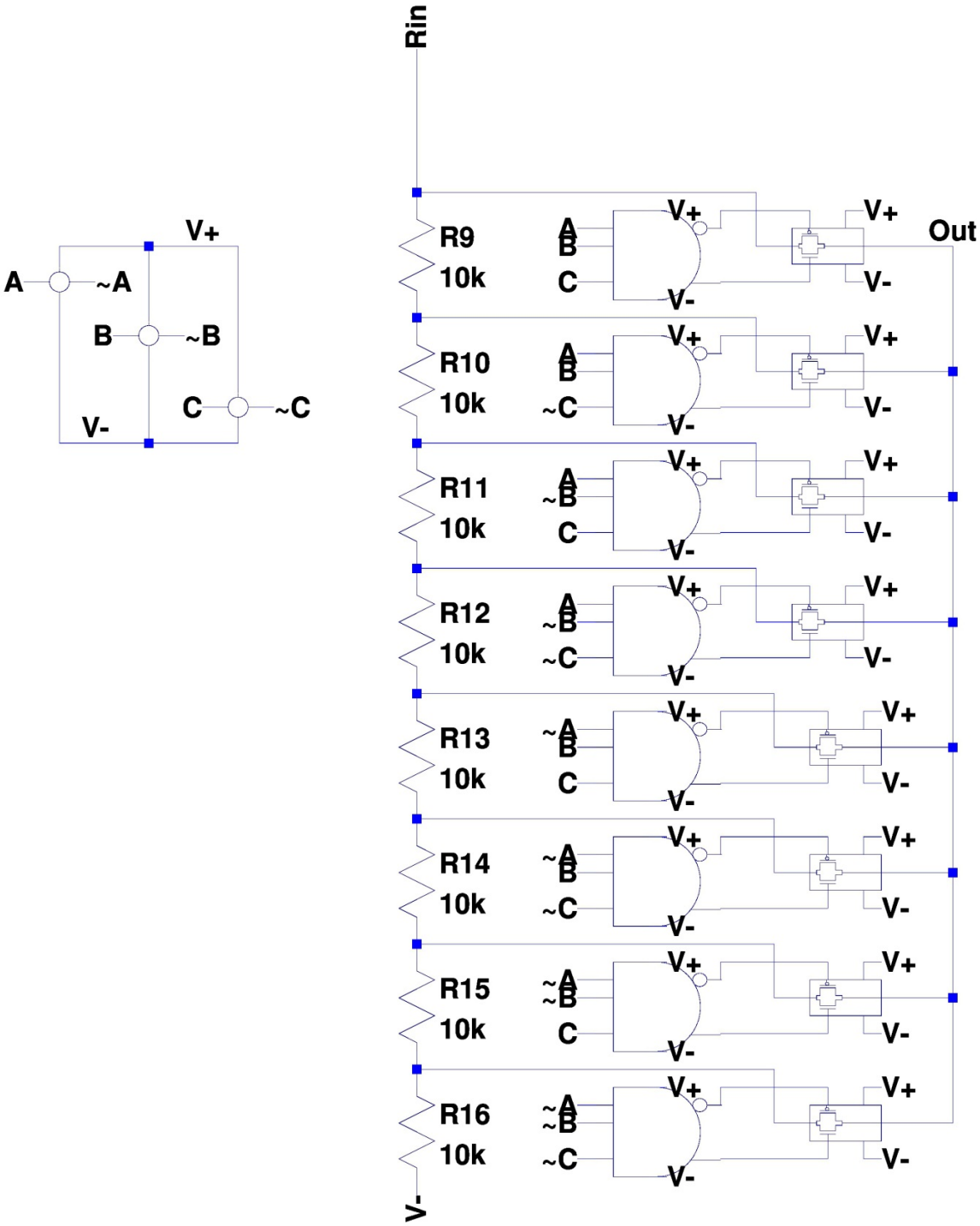
See https://github.com/MattWis/MADVLSI-Final for fully detailed schematics

Top Level Schematic:

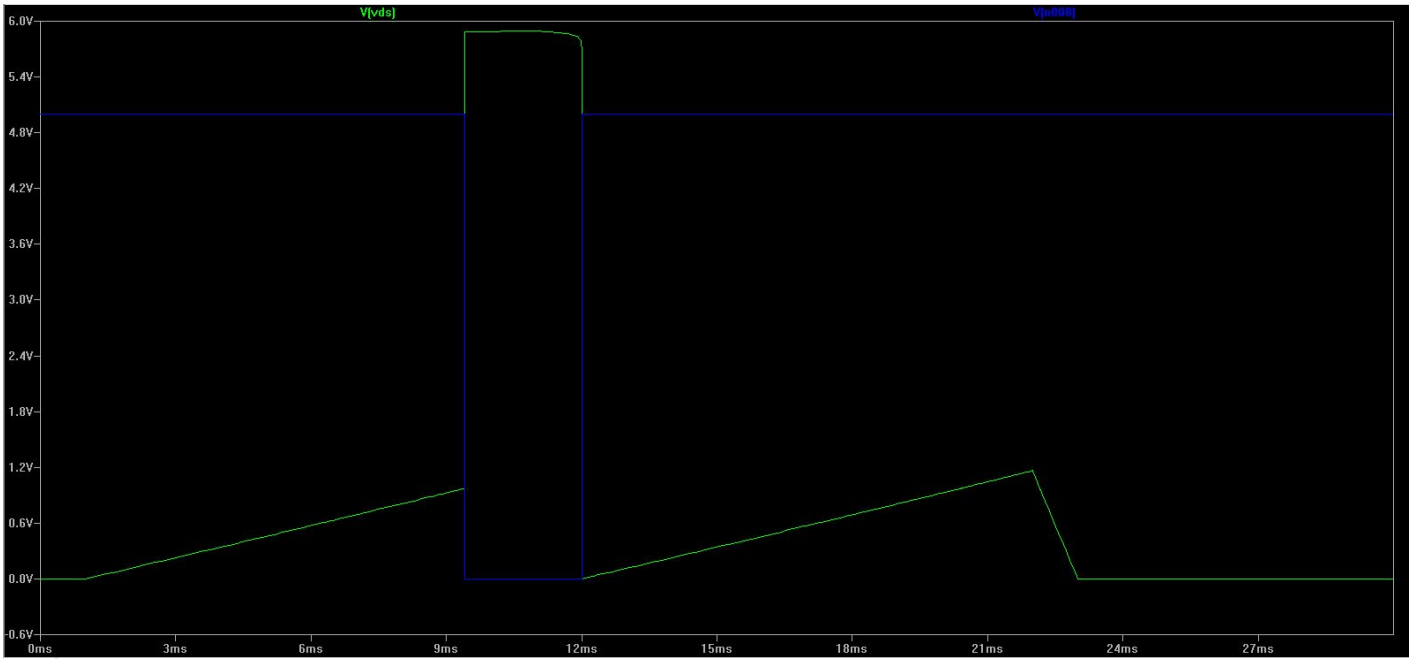


DAC Design:

We chose to redesign a DAC using a different architecture than was used in MP4. This is because our chip has no clock source, nor do we want to add one. Therefore, a switched DAC is non-ideal. This hierarchy is slightly larger because of the use of resistors, but operates in steady state.

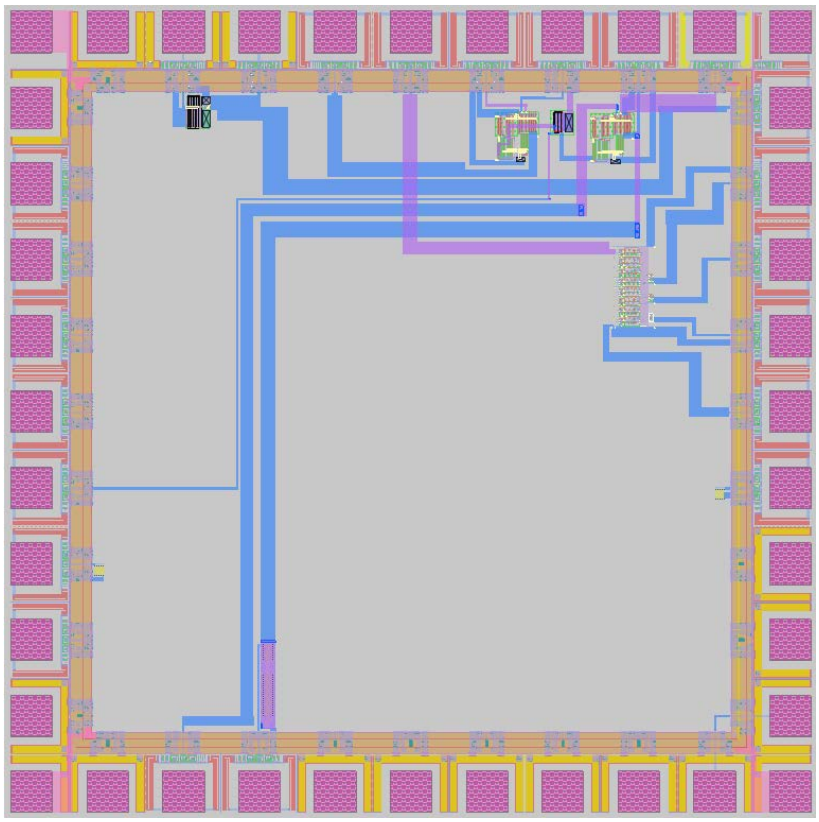


Simulation:



Explanation: As Vds (green) increases, eventually it hits the trip point. At this point, the gate driver output (blue) drops low to shut off the fet. Naturally, Vds then increases to the supply rail. After a short period of time, the reset pin is activated (manually) to reactivate the fet. The reset pin is held for the rest of the simulation, which explains why the breaker does not trip a second time.

Layout: See https://github.com/MattWis/MADVLSI-Final for all MAGIC layout files



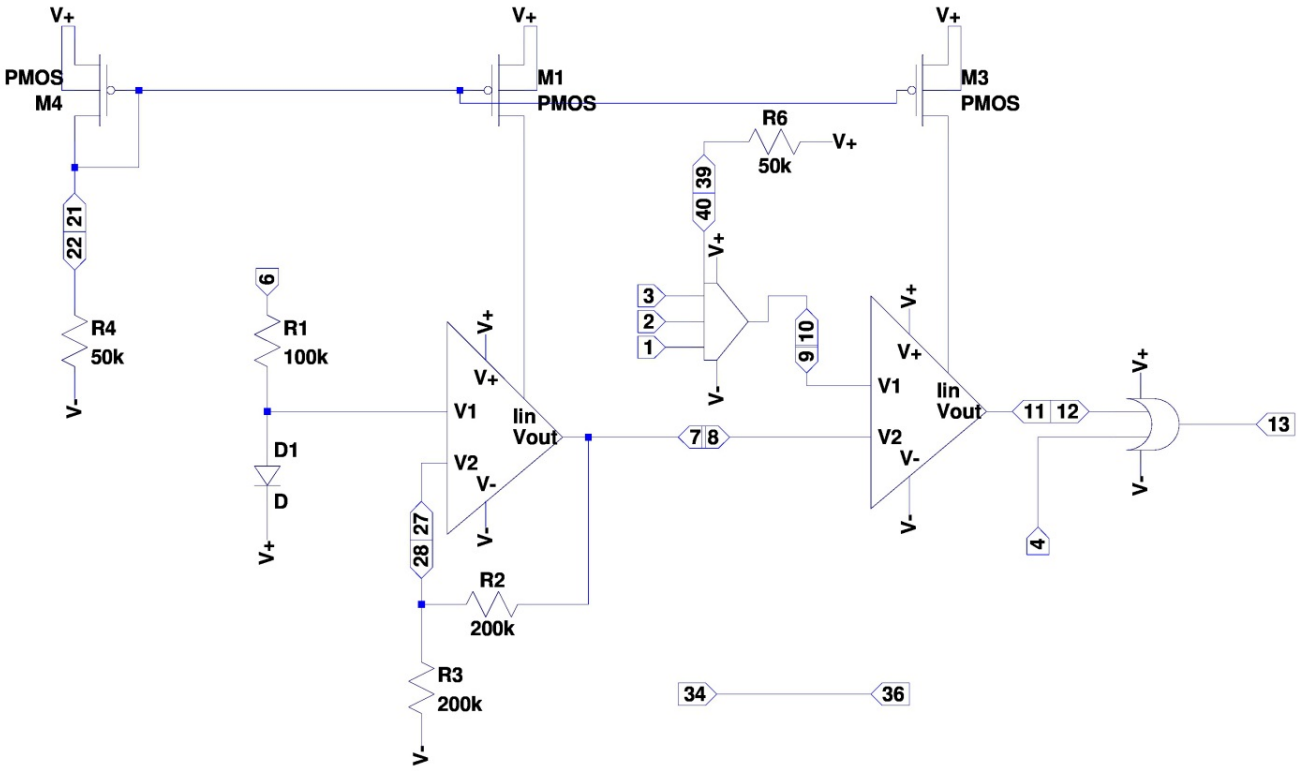
Matching:

All individual sub components were successfully matched with LVS comparison to their respective LTSpice models. The .net, .spice, and comp.out files for these comparisons can be found at https://github.com/MattWis/MADVLSI-Final. The full assembly could not be compared because the diodes, bjts, and resistors would not extract correctly, but connections were tested by selecting entire nets and verifying that all items were attached to the correct nets. Furthermore, basic error checking was done to ensure that ground and power were not shorted, that none of the inputs/outputs were shorted to power and ground, etc.

Testing procedure:

In order to maximize the chances of success, we have created a large number of internal break points. These are places where two elements are supposed to be connected, but are intentionally left disconnected. Instead, both elements are routed out to bonding pads. This means that for proper operation, these two pins will need to be jumpered together. Prior to inserting the jumpers though, each element can be tested individually, and if one doesn't work it can be bypassed by an off-the-shelf compatible component.

Schematic with all external pins and breakpoints labeled



As such, our testing procedure involves individually testing each component, then inserting jumpers, then one final test on the entire system. Each test assumes that all previous tests have passed, or that a suitable bypass has been found.

TEST 1: on chip resistor (DAC). Use a multimeter to measure the resistance between pin 39 and power. It should be ~50K. Assuming this passes, you may now jumper pins 39 to 40.

TEST 2: on chip resistor 2 (current source). Measure the resistance between pin 22 and ground. It should be ~ 50k.

TEST 3: on chip resistor 3 (amplifier). Measure the resistance between pin 28 and 7. It should be ~ 200k.

TEST 4: on chip resistor 3 (amplifier). Measure the resistance between pin 28 and gnd. It should be ~ 200k. You can now jumper 28 to 27

TEST 5: the DAC. Apply power to the chip. Use a microcontroller or digital logic generator to provide binary counting logic on pins 1, 2, and 3. Use an oscilloscope to measure the voltage on pin 10. It should count 8 discrete binary steps. They will not necessarily reach 5V. Upper voltage depends on the resistor value.

TEST 6: current source. Tie an external resistor (50k) from pin 21 to ground. Measure the current through this resistor. Current should be ~100 uA. Assuming both this test and test 2 pass, you may now Jumper pins 21 to pins 22.

TEST 7: Op amp. Apply a voltage to pin 9 (~2.5V). Sweep the voltage on pin 8 around the voltage on pin 9 and verify that the behavior of an op amp is seen (output is pin 11). Assuming both the op amp and DAC passed tests, you may now jumper pins 10 and 9.

TEST 8: OR gate. Apply a digital logic signal to pins 12 and 4. Read the voltage on pin13 and verify that the truth table of an OR gate is accurately represented. Jumper pins 11 and 12.

TEST 9: amp. Apply a smallish amplitude (1V pk-pk) sine wave on pin 6. Measure voltage on pin 7. Verify that the input waveform is amplified by a factor of 2. Note that for low voltages, the amplification factor may be slightly smaller. Assuming this test is passed, tie pins 7 and 8.

TEST 10: full system test. Apply a small voltage analog signal on pin 6. Apply a digital binary input on pins 1,2, and 3. Apply a digital low on pin 4. Read the digital state of pin 13. Increase the voltage on pin 6 until it 'trips' (digital state on pin 13 becomes high). Reset the state of pin 13 by raising pin 4 high, then returning pin 4 low. Repeat this test multiple times. The trip voltage should be consistent. It should also be linearly controllable via pins 1,2, and 3.

TEST 11: high voltage robustness. Apply a higher voltage (20-50V) on pin 6. Remove the voltage and repeat the previous test to verify that nothing has broken.

TEST 12: practical application. Set up a power mosfet as a low side switch with a variable load. Either drive the gate with pin 13 (if the gate can be driven by 5V), or use pin 13 as a logic signal for a gate

driver. Tie the drain to pin 6. Apply a digital signal on pins 1, 2, 3. See if you can increase the load to the point where the FET shuts off. Use pin 4 to turn it back on.

Final Notes: Easter Eggs (additional things on our chip worth testing for fun)

TEST 13: High voltage fet (maybe). There may be a high voltage fet that can be characterized.

TEST 14: Fuse. A short metal trace connects pins 34 and 36, designed to operate as a single use fuse. Put a current between pins 14 and 16. Increase current until the current stops (circuit becomes open). Record this current level. Feel free to test if any other components on the chip were fried by repeating above tests. (not required)

TEST 15: Inductor. A large spiral of metal3 was included because we had no other use for metal 3. Feel free to test the trace for both resistance (which may be considerable) and inductance (which is probably small, but hopefully measurable), as well as capacitance (hopefully not large enough to matter).