TPS745-Q1 500-mA LDO With Power-Good in a Small Wettable Flank WSON Package

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Device junction temperature: –40°C to 150°C
- Package:
  - 2-mm × 2-mm wettable flank WSON
- Input voltage range: 1.5 V to 6.0 V
- Output voltage range:
  - Fixed option: 0.65 V to 5.0 V
  - Adjustable option: 0.55 V to 5.5 V
- High PSRR: 45 dB at 100 kHz
- Output accuracy: 1% typical, 2% maximum
- Power-good output options:
  - Open-drain and push-pull
- Ultra-low dropout:
  - 225 mV (max) at 500 mA (3.3 V_{OUT})
- Stable with a 1-µF or larger capacitor
- Low I_Q: 25 µA (typical)
- Active output discharge

2 Applications

- Head units
- Clusters
- Telematics
- Radar
- Camera modules
- General post-regulation (for example, 5 V to 3.3 V)

3 Description

The TPS745-Q1 is a 500-mA ultra-low-dropout regulator (LDO) with power-good functionality. This device is available in a small 6-pin, 2-mm × 2-mm WSON package with wettable flanks to facilitate optical inspection. The TPS745-Q1 consumes low quiescent current and provides fast line and load transient performance.

The TPS745-Q1 is a flexible device for post-regulation by supporting an input voltage range from 1.5 V to 6.0 V and an externally adjustable output range of 0.65 V to 5.5 V. The device also features fixed output voltages for powering common voltage rails.

The TPS745-Q1 has a power-good (PG) output that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output can be used for sequencing multiple power sources in the system.

The TPS745-Q1 is stable with small ceramic output capacitors, allowing for a small overall solution size. A precision band-gap and error amplifier provides high accuracy of 1% (max) at 25°C and 2% (max) over temperature. This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. The TPS745-Q1 has an internal foldback current limit that helps reduce the thermal dissipation during short-circuit events.

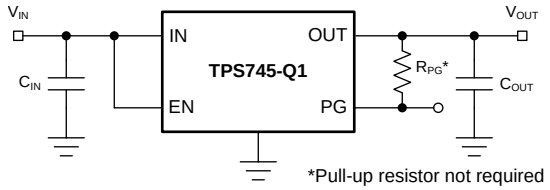
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS745-Q1	Wettable flank WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

Typical Application



*Pull-up resistor not required for push-pull option

Table of Contents

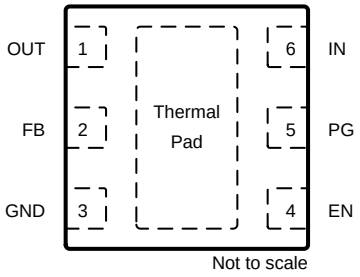
ADVANCE INFORMATION

4 Revision History

DATE	REVISION	NOTES
June 2019	*	Initial release.

5 Pin Configuration and Functions

DRV Package
6-Pin Adjustable WSON
Top View



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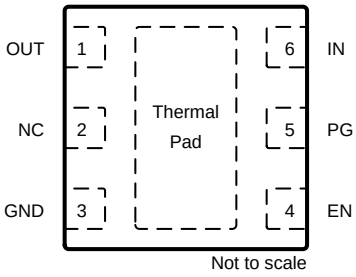
DRV Package
6-Pin Fixed WSON
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	FIXED	ADJUSTABLE		
EN	4	4	Input	Enable pin. Drive EN greater than V_{HI} to turn on the regulator. Drive EN less than V_{LO} to put the low-dropout regulator (LDO) into shutdown mode.
FB	—	2	—	This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO.
GND	3	3	—	Ground pin.
IN	6	6	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the input capacitor as close to the output of the device as possible.
NC	2	—	—	No internal connection. Ground this pin for better thermal performance.
OUT	1	1	Output	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the output capacitor as close to output of the device as possible.
PG	5	5	Output	Power-good output. Available in open-drain and push-pull topologies. For the open-drain version, if the power-good functionality is not being used, ground this pin or leave floating. For the push-pull version, if the power-good functionality is not being used, leave this pin floating.
Thermal Pad			—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_{IN}	–0.3	6.5	V
	Enable, V_{EN}	–0.3	6.5	
	Feedback, V_{FB}	–0.3	2	
	Power-good, V_{PG}	–0.3	6.5	
	Output, V_{OUT}	–0.3	V_{IN} + 0.3(2)	
Current	Output, I_{OUT}		Internally Limited	
	Power-good, I_{PG}		±10	mA
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 6.5 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	TBD	V
		Charged-device model (CDM), per AEC Q100-011	TBD	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
C_{IN}	Input capacitor		1			µF
C_{OUT}	Output capacitor		1		220	µF
V_{IN}	Input voltage		1.5		6.0	V
V_{OUT}	Output voltage	Adjustable only	0.55		5.5	V
		Fixed only	0.65		5.0	
I_{OUT}	Output current		0		500	mA
V_{EN}	Enable voltage(1)		0		6	V
V_{PG}	PG voltage		0		6	V
T_J	Junction operating temperature		–40		150	°C

(1) Maximum enable toggle frequency must be below 10 kHz.

6.4 Thermal Information

THERMAL METRIC(1)		TPS745-Q1 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	20.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

ADVANCE INFORMATION

6.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +150°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.5		6.0	V
V_{OUT}	Output voltage	Adjustable only		0.55		5.5	V
		Fixed only		0.65		5.0	
V_{FB}	Feedback voltage			0.542	0.55	0.558	V
	Output accuracy	T_J = 25°C		–0.7%		0.7%	
		V_{OUT} ≥ 1 V		–1.5%		1.5%	
		0.6 V ≤ V_{OUT} < 1 V		–25		25	mV
$(\Delta_{VOUT})_{\Delta VIN}/V_{OUT}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 6.0 V			2	10	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0.1 mA ≤ I_{OUT} ≤ 500 mA			0.050		V/A
I_{GND}	Ground current	T_J = 25°C , I_{OUT} = 0 mA			25	41	µA
		I_{OUT} = 0 mA				45	
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, 1.4 V ≤ V_{IN} ≤ 6.0 V, T_J = 25°C			0.1	1	µA
I_{FB}	Feedback pin current (adjustable only)				0.01	0.1	µA
I_{CL}	Output current limit	V_{IN} = V_{OUT} + $V_{DO(MAX)}$ + 0.1 V	V_{OUT} = V_{OUT} – 0.2 V, V_{OUT} ≤ 1 V	530	720	865	mA
			V_{OUT} = 0.9 × V_{OUT}, 1.0 V < V_{OUT} ≤ 5.5 V	530	720	865	
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V				990	mA
V_{DO}	Dropout voltage	I_{OUT} = 500 mA, V_{OUT} = 0.95 × $V_{OUT(NOM)}$	0.6 V ≤ V_{OUT} < 0.8 V			850	mV
			0.8 V ≤ V_{OUT} < 1.0 V			675	
			1.0 V ≤ V_{OUT} < 1.2 V			505	
			1.2 V ≤ V_{OUT} < 1.5 V			340	
			1.5 V ≤ V_{OUT} < 1.8 V			285	
			1.8 V ≤ V_{OUT} < 2.5 V			235	
			2.5 V ≤ V_{OUT} < 3.3 V			225	
			3.3 V ≤ V_{OUT} < 5.5 V		50		
PSRR	Power-supply rejection ratio	f = 1 kHz			45		dB
		f = 100 kHz			30		
		f = 1 MHz			30		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 0.6 V			53		μV_{RMS}
$V_{UVLO,r}$	Undervoltage lockout	V_{IN} rising		1.21	1.33	1.47	V
$V_{UVLO,f}$	Undervoltage lockout	V_{IN} falling		1.17	1.29	1.42	V
$V_{UVLO,HYST}$	Undervoltage lockout hysteresis	V_{IN} hysteresis			40		mV
t_{STR}	Startup time	From EN low-to-high transition to V_{OUT} = V_{OUT} × 95%			500		µs
V_{HI}	EN pin high voltage (enabled)			1.0			V
V_{LO}	EN pin low voltage (enabled)					0.3	V
I_{EN}	Enable pin current	V_{IN} = EN = 6.0 V			10		nA
$R_{PULLDOWN}$	Pulldown resistance	V_{IN} = 6.0 V			95		Ω
PG_{HTH}	PG high threshold	V_{OUT} increasing		89	94	95	$\%V_{OUT}$
PG_{LTH}	PG low threshold	V_{OUT} decreasing		87	92	93	$\%V_{OUT}$
$V_{OL(PG)}$	PG pin low-level output voltage	V_{IN} ≥ 1.5 V, I_{SINK} = 1 mA				300	mV
		V_{IN} ≥ 2.75 V, I_{SINK} = 2 mA				300	

ADVANCE INFORMATION

Electrical Characteristics (continued)

at operating temperature range (T_J = –40°C to +150°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(PG)}$	PG pin high-level output voltage (only for push-pull version)	V_{OUT} ≥ 1.0 V(1), I_{SINK} = 0.04 mA	0.8 × V_{OUT}			V
		V_{OUT} ≥ 1.4 V, I_{Source} = 0.2 mA	0.8 × V_{OUT}			
		V_{OUT} ≥ 2.5 V, I_{Source} = 0.5 mA	0.8 × V_{OUT}			
		V_{OUT} ≥ 4.5 V, I_{Source} = 1.0 mA	0.8 × V_{OUT}			
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > PG_{HTH}, V_{PG} = 6.0 V			300	nA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		155		

(1) The push-pull option is supported only for V_{OUT} ≥ 1.0 V.

6.6 Timing Requirements

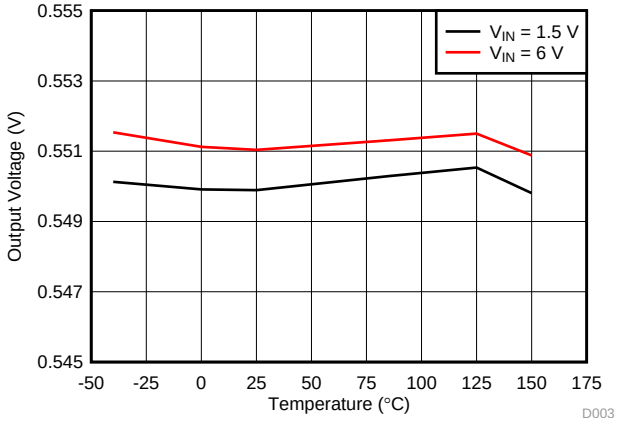
PARAMETER			MIN	NOM	MAX	UNIT
t_{PGDH}	PG delay time (rising) from 92% V_{OUT} to 20% of PG(1)		135	165	178	µs
		'B' version		5		ms
t_{PGDL}	PG delay time (falling) from 90% V_{OUT} to 80% of PG(1)		1.5	7	10	µs

(1) Output overdrive = 10%

ADVANCE INFORMATION

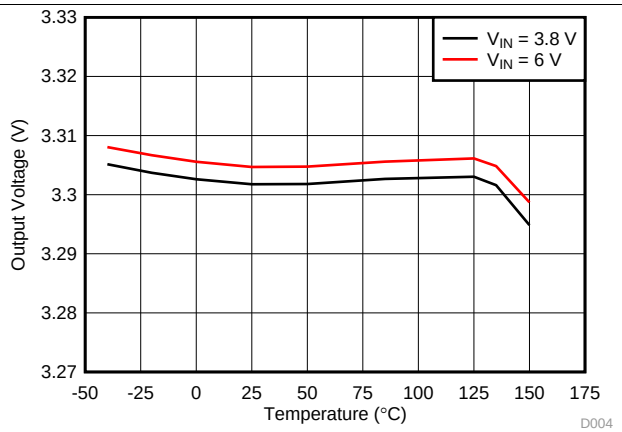
6.7 Typical Characteristics

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



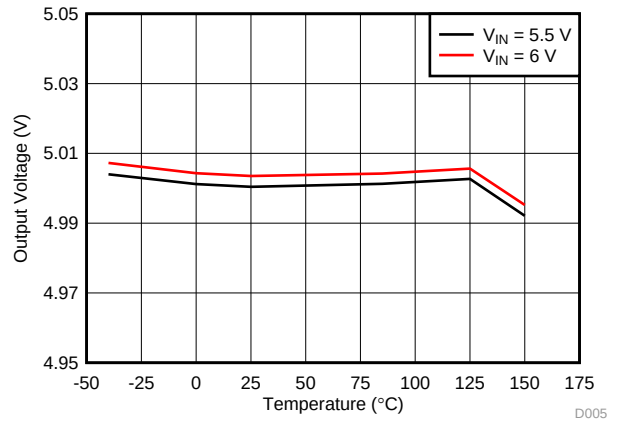
V_{OUT} = 0.55 V, I_{OUT} = 1 mA

Figure 1. Output Voltage vs Ambient Temperature



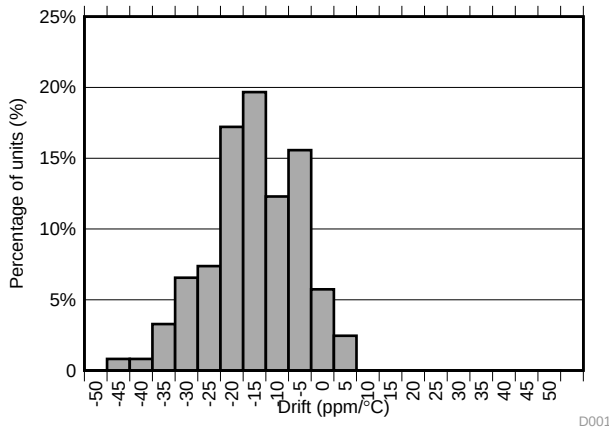
V_{OUT} = 3.3 V, I_{OUT} = 1 mA

Figure 2. Output Voltage vs Ambient Temperature



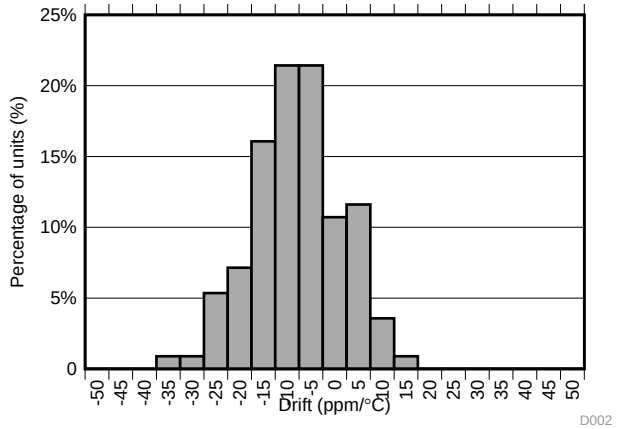
V_{OUT} = 5 V, I_{OUT} = 1 mA

Figure 3. Output Voltage vs Ambient Temperature



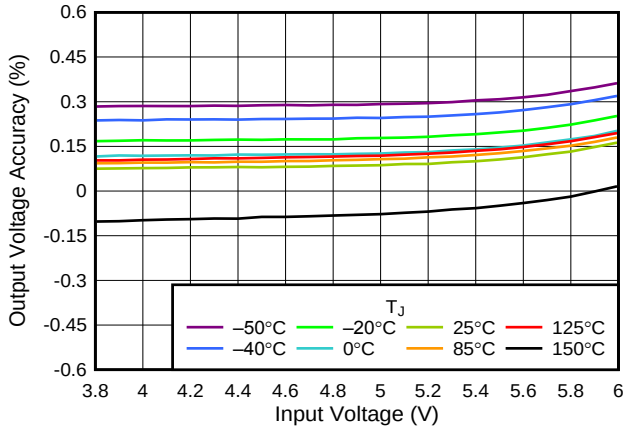
0.65-V, 3.3-V, and 5-V options, I_{OUT} = 1 mA

Figure 4. Temperature Drift Histogram (–40°C to +25°C)



0.65-V, 3.3-V, and 5-V options, I_{OUT} = 1 mA

Figure 5. Temperature Drift Histogram (25°C to 150°C)



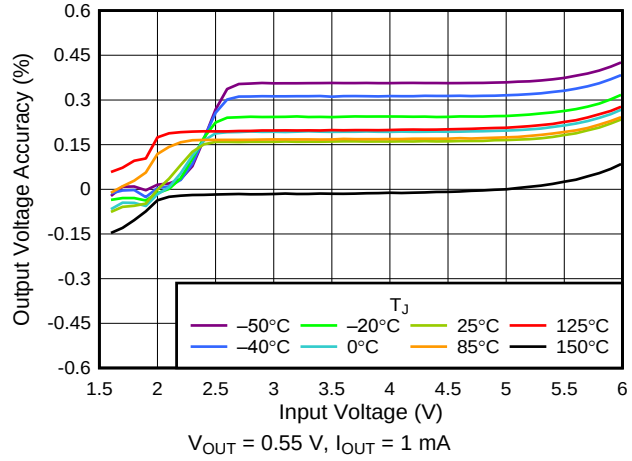
V_{OUT} = 3.3 V, I_{OUT} = 1 mA

Figure 6. 3.3-V Line Regulation vs V_{IN}

ADVANCE INFORMATION

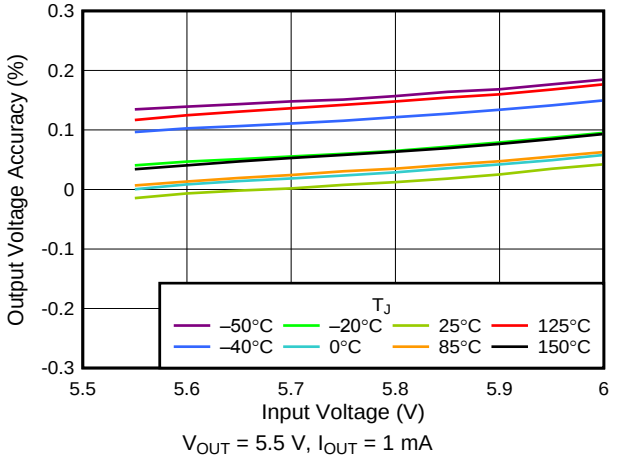
Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



V_{OUT} = 0.55 V, I_{OUT} = 1 mA

Figure 7. 0.55-V Line Regulation vs V_{IN}



V_{OUT} = 5.5 V, I_{OUT} = 1 mA

Figure 8. 5.5-V Line Regulation vs V_{IN}

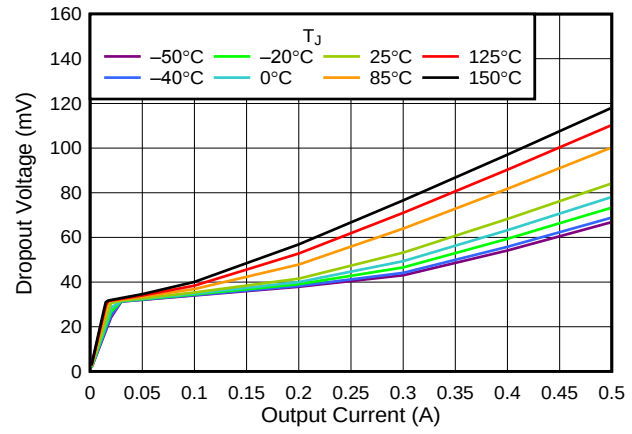


Figure 9. 3.3-V Dropout Voltage vs I_{OUT}

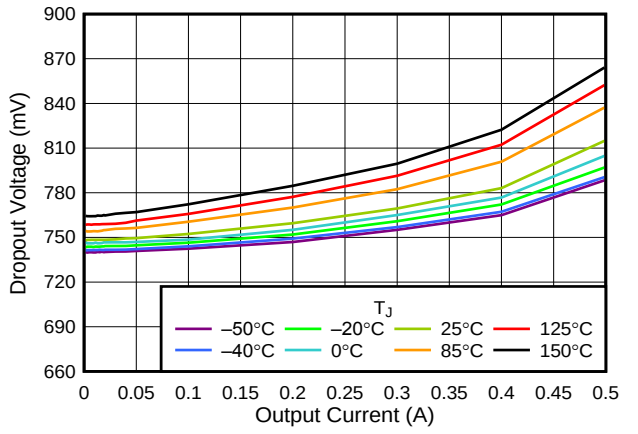


Figure 10. 0.55-V Dropout Voltage vs I_{OUT}

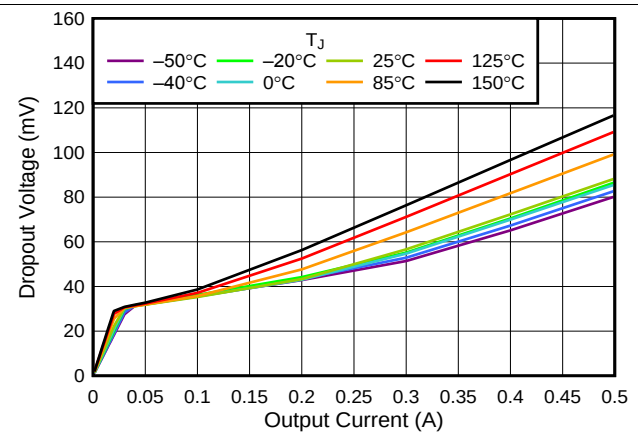
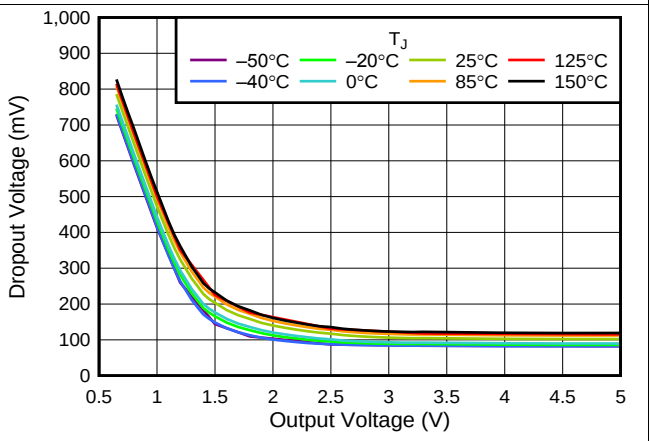


Figure 11. 5.5-V Dropout Voltage vs I_{OUT}



I_{OUT} = 500 mA

Figure 12. V_{DO} vs V_{OUT}

ADVANCE INFORMATION

Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

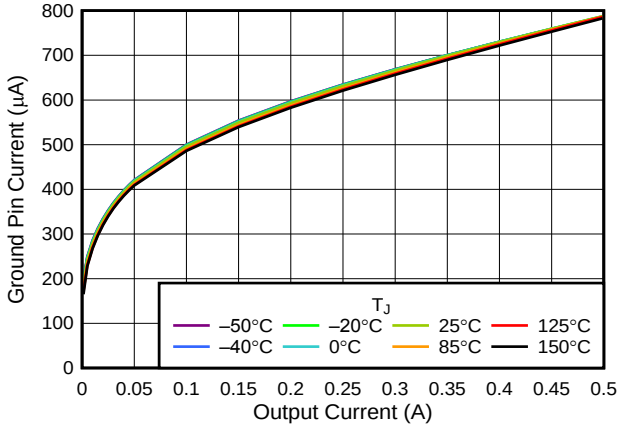


Figure 13. I_{GND} vs I_{OUT}

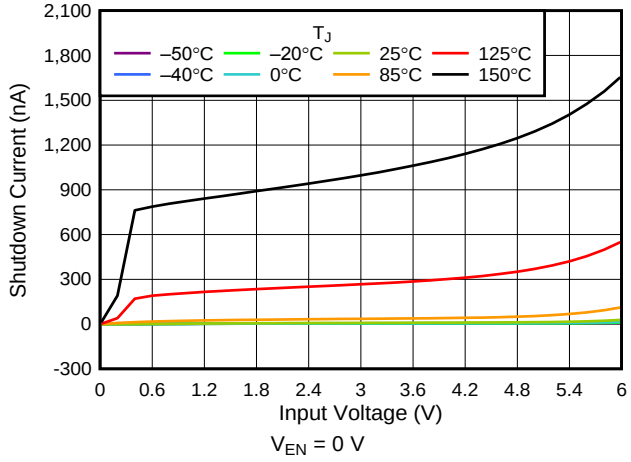


Figure 14. I_{SHDN} vs V_{IN}

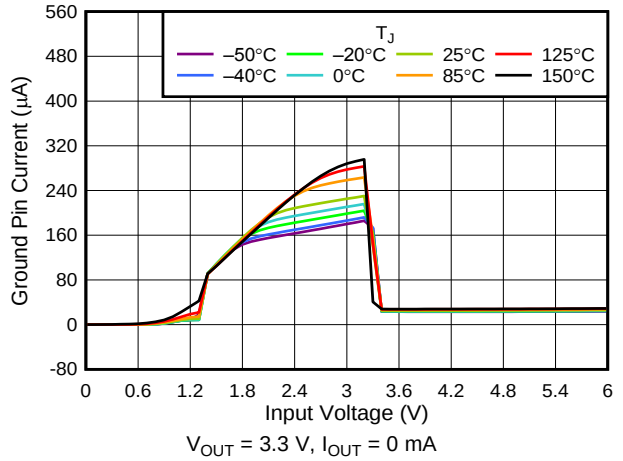


Figure 15. I_Q vs V_{IN}

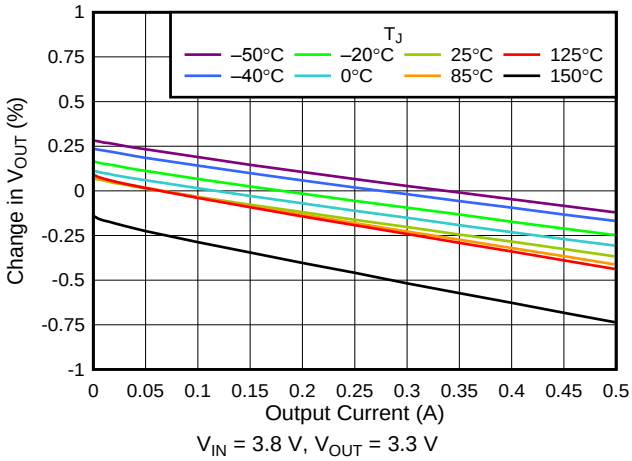


Figure 16. 3.3-V Load Regulation vs I_{OUT}

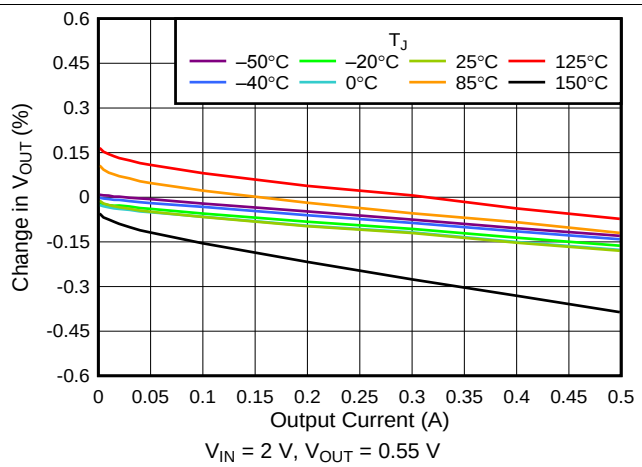


Figure 17. 0.55-V Load Regulation vs I_{OUT}

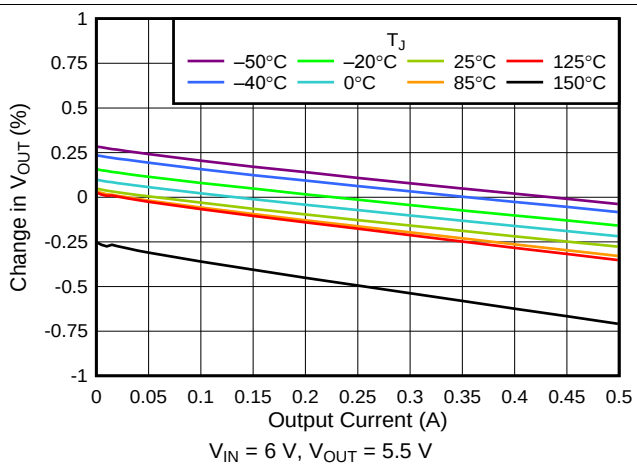


Figure 18. 5-V Load Regulation vs I_{OUT}

ADVANCE INFORMATION

Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

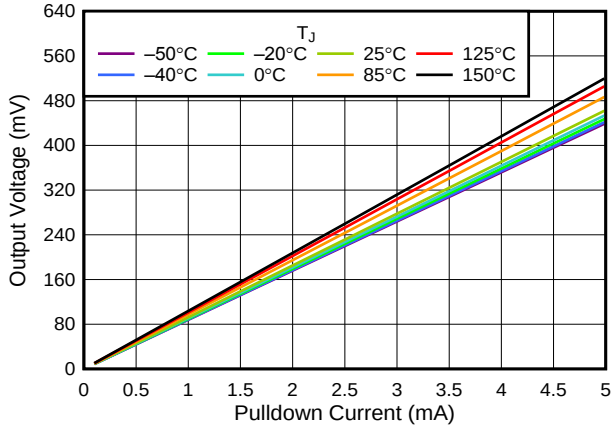


Figure 19. V_{OUT} vs I_{OUT} Pulldown Resistor

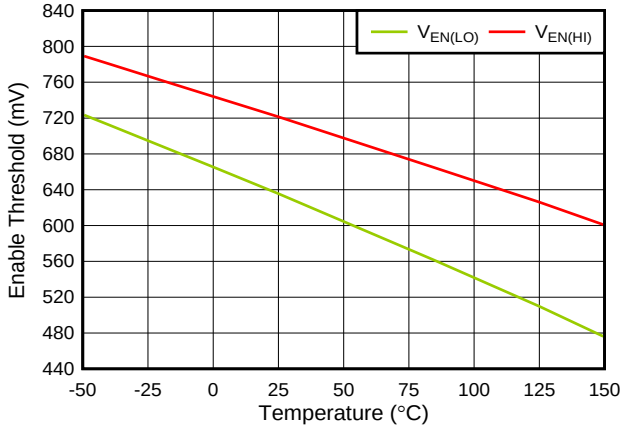


Figure 20. $V_{EN(HI)}$ and $V_{EN(LO)}$ vs Temperature

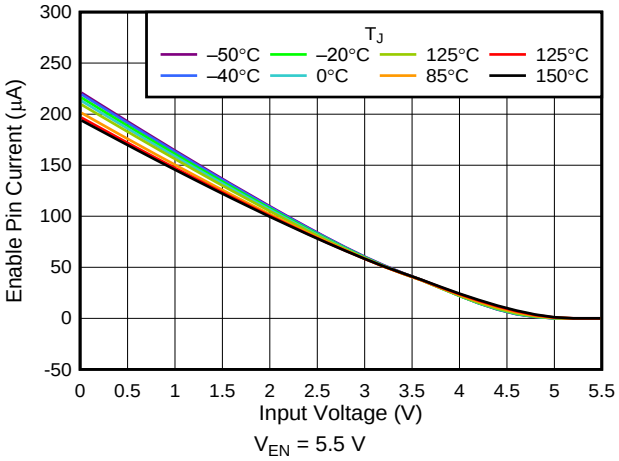


Figure 21. I_{EN} vs V_{IN}

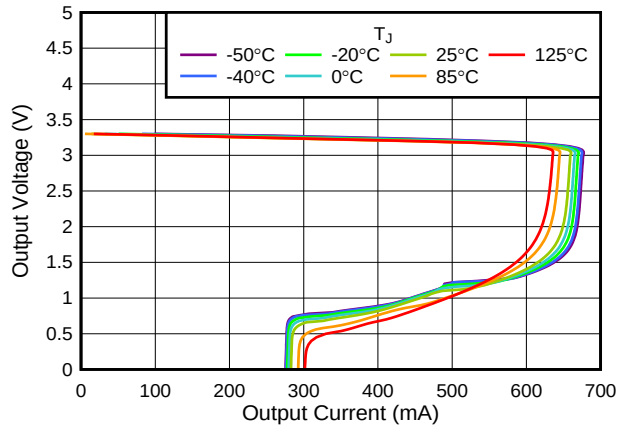


Figure 22. 3.3-V V_{OUT} vs I_{OUT}

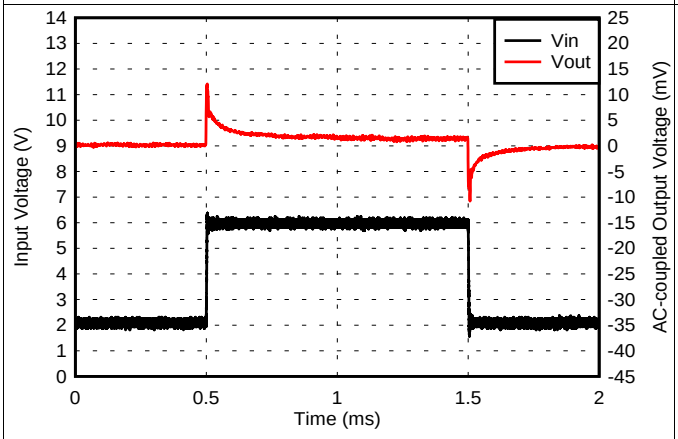


Figure 23. 0.55-V Line Transient

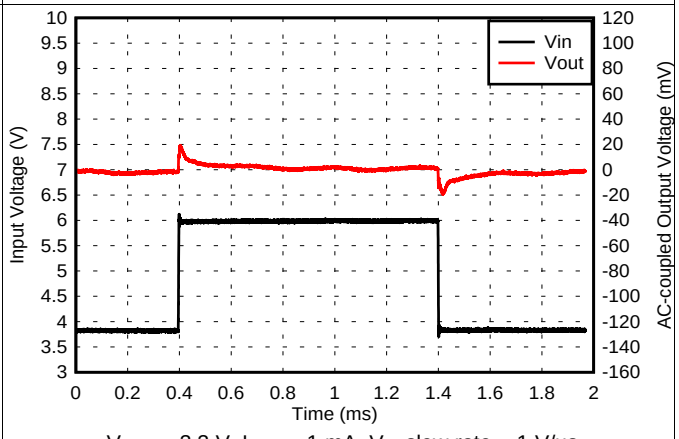
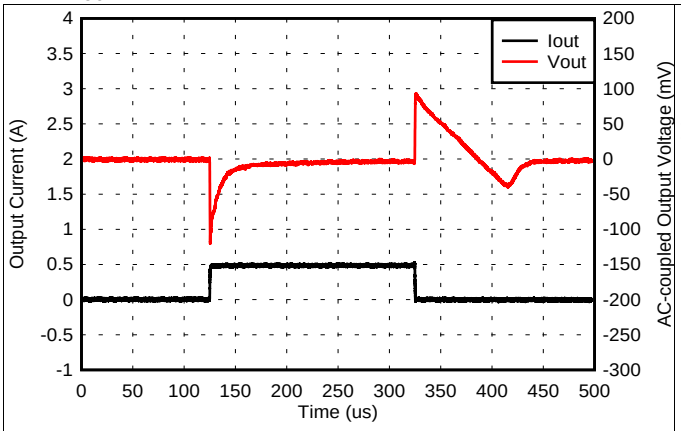


Figure 24. 3.3-V Line Transient

ADVANCE INFORMATION

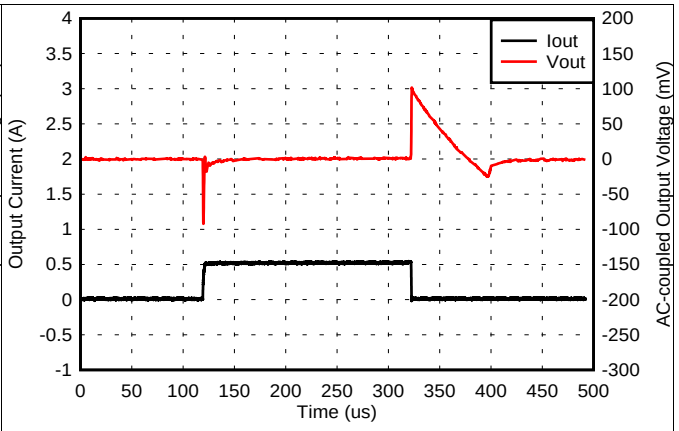
Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



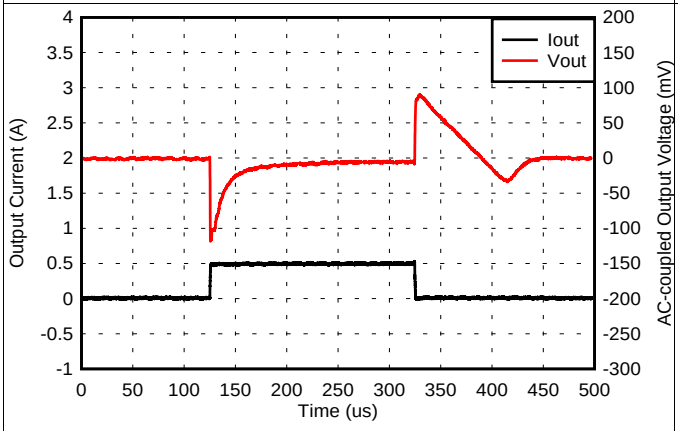
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} slew rate = 1 A/µs

Figure 25. 3.3-V, 1-mA to 500-mA Load Transient



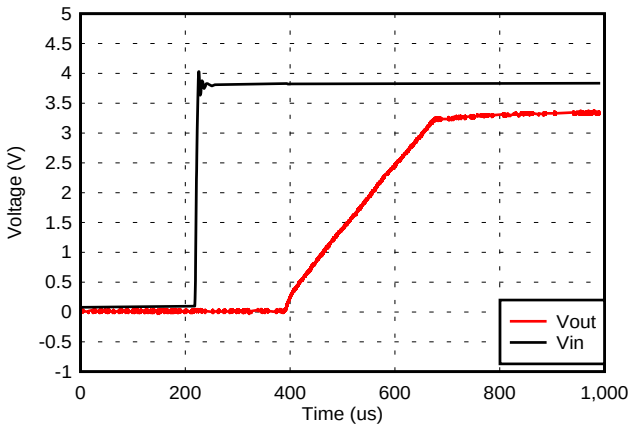
V_{IN} = 2 V, V_{OUT} = 0.55 V, I_{OUT} slew rate = 1 A/µs

Figure 26. 0.55-V, 1-mA to 500-mA Load Transient



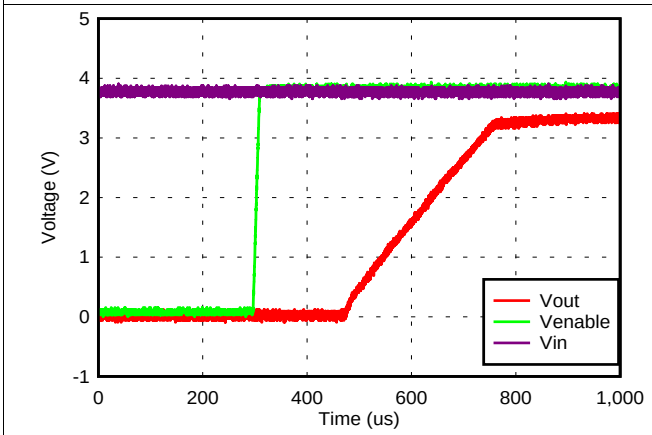
V_{IN} = 5.5 V, V_{OUT} = 5 V, I_{OUT} slew rate = 1 A/µs

Figure 27. 5-V, 1-mA to 500-mA Load Transient



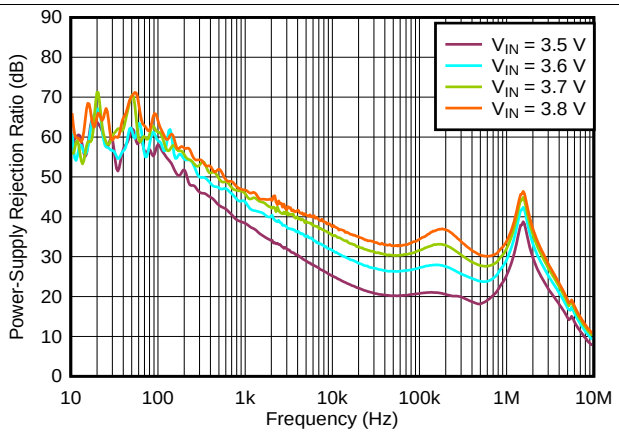
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA

Figure 28. V_{IN} Power-Up



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA

Figure 29. Startup With EN



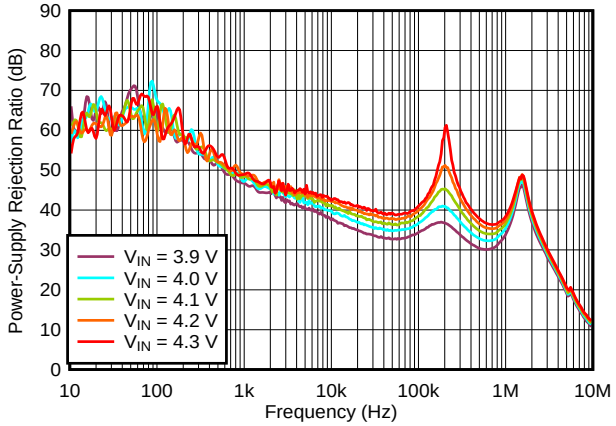
V_{OUT} = 3.3 V, I_{OUT} = 500 mA, C_{OUT} = 2.2 µF

Figure 30. PSRR vs Frequency and V_{IN}

ADVANCE INFORMATION

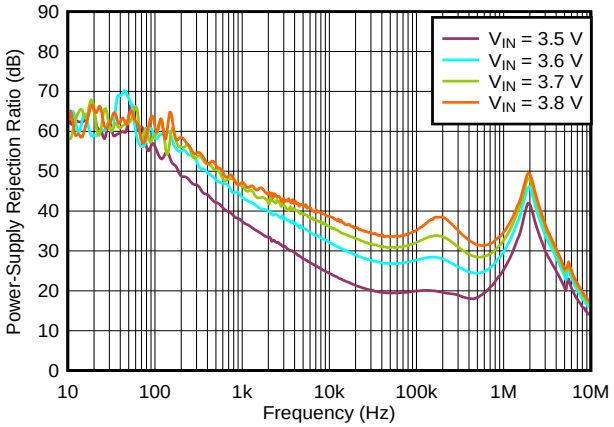
Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



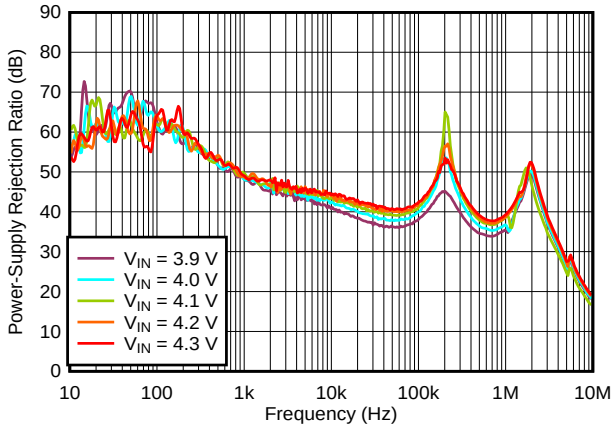
V_{OUT} = 3.3 V, I_{OUT} = 500 mA, C_{OUT} = 2.2 µF

Figure 31. PSRR vs Frequency and V_{IN}



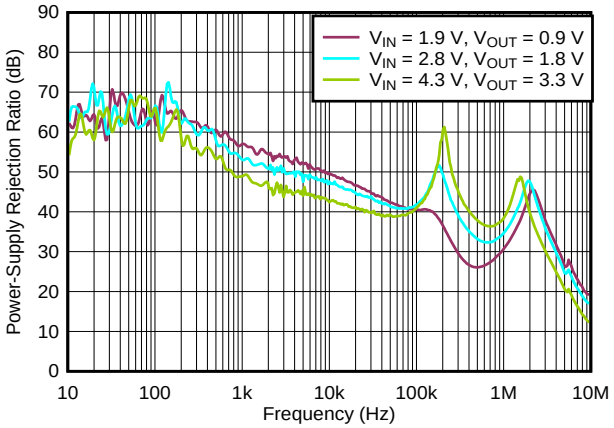
V_{OUT} = 3.3 V, I_{OUT} = 250 mA, C_{OUT} = 2.2 µF

Figure 32. PSRR vs Frequency and V_{IN}



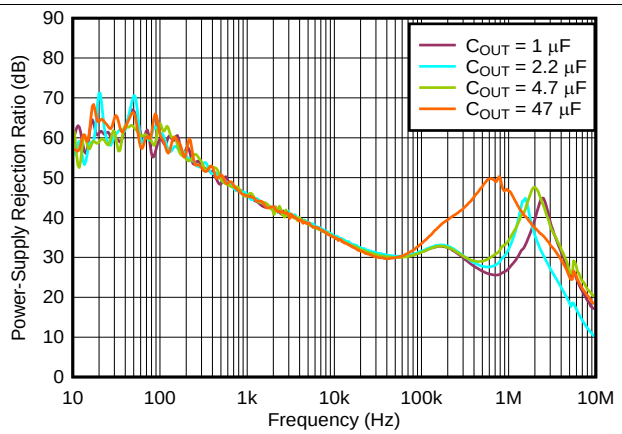
V_{OUT} = 3.3 V, I_{OUT} = 250 mA, C_{OUT} = 2.2 µF

Figure 33. PSRR vs Frequency and V_{IN}



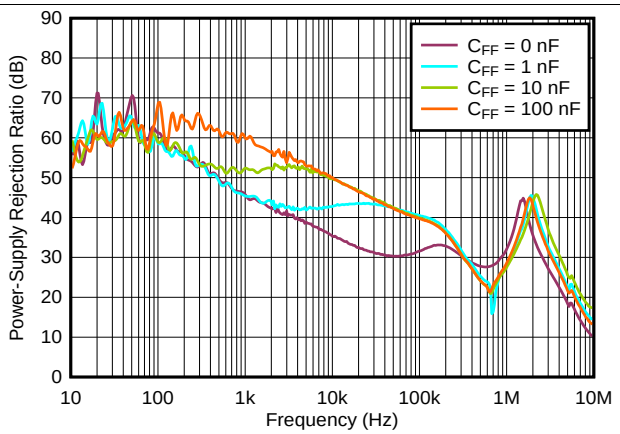
I_{OUT} = 500 mA, C_{OUT} = 2.2 µF

Figure 34. PSRR vs Frequency



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

Figure 35. PSRR vs Frequency and C_{OUT}



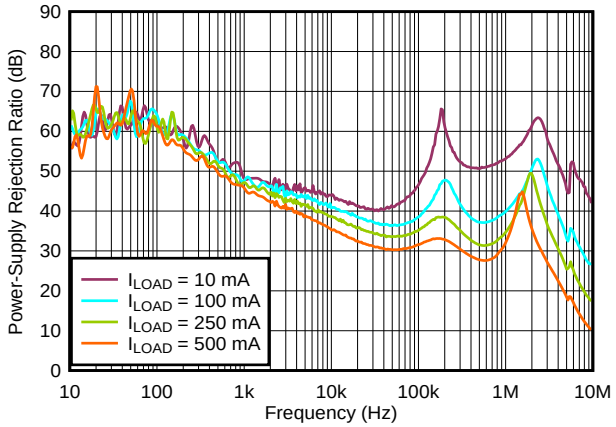
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

Figure 36. PSRR vs Frequency and C_{FF}

ADVANCE INFORMATION

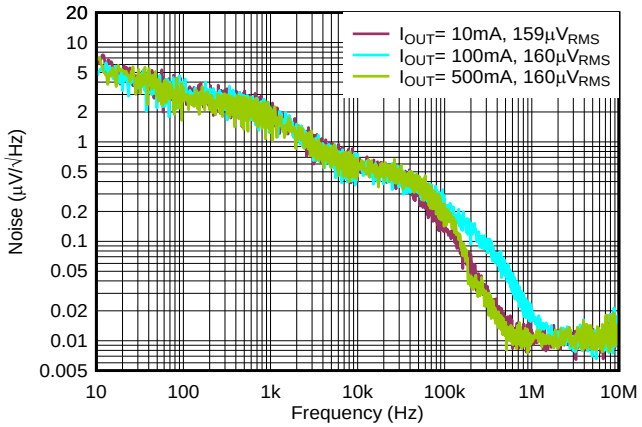
Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



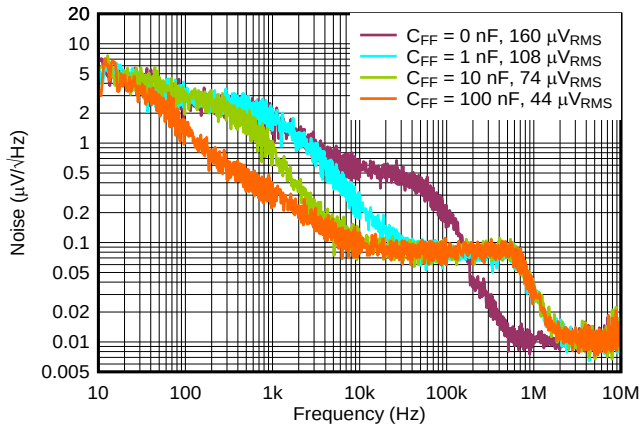
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF

Figure 37. PSRR vs Frequency and I_{LOAD}



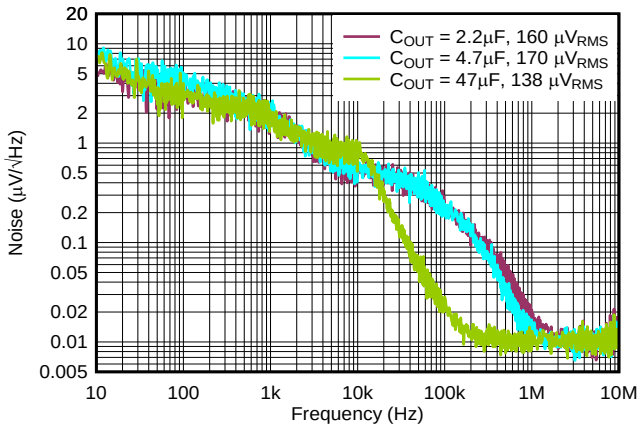
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF,
V_{RMS} BW = 10 Hz to 100 kHz

Figure 38. Output Spectral Noise Density vs Frequency and I_{OUT}



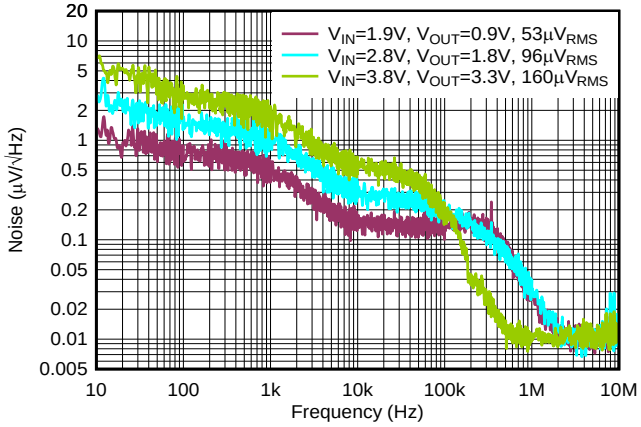
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA, C_{OUT} = 2.2 µF,
V_{RMS} BW = 10 Hz to 100 kHz

Figure 39. Output Spectral Noise Density vs Frequency and C_{FF}



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 100 mA, C_{FF} = 0 µF,
V_{RMS} BW = 10 Hz to 100 kHz

Figure 40. Output Spectral Noise Density vs Frequency and C_{OUT}



I_{OUT} = 500 mA, C_{OUT} = 2.2 µF, V_{RMS} BW = 10 Hz to 100 kHz

Figure 41. Output Spectral Noise Density vs Frequency

ADVANCE INFORMATION

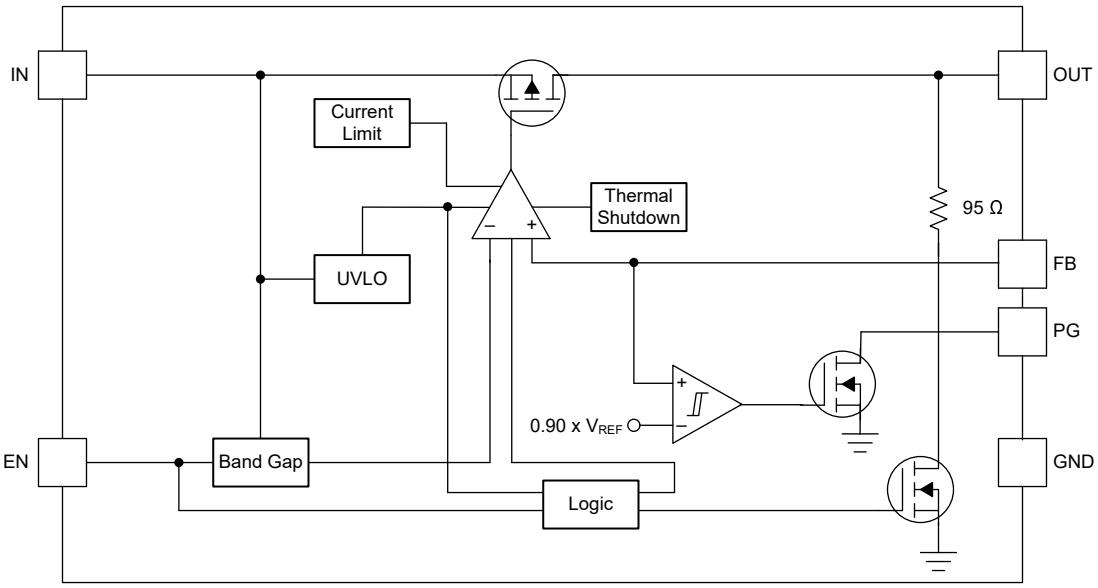
7 Detailed Description

7.1 Overview

The TPS745-Q1 is a low-dropout regulator (LDO) that consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, good PSRR with low dropout voltage, make this device ideal for automotive applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is –40°C to 150°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 TPS745-Q1 Comparison

Table 1 lists the three different power-good (PG) options for the TPS745-Q1.

Table 1. TPS745-Q1 Comparison Table

DEVICE	POWER-GOOD DELAY	POWER-GOOD TYPE
TPS745xxPQWDRVRQ1	150 µs	Open-drain
TPS745xxPBQWDRVRQ1	5 ms	Open-drain
TPS745xxPCQWDRVRQ1	150 µs	Push-pull

7.3.2 Undervoltage Lockout (UVLO)

The TPS745-Q1 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage (V_{UVLO}). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When V_{IN} is less than V_{UVLO}, the output is connected to ground with a 95-Ω pulldown resistor.

ADVANCE INFORMATION

7.3.3 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed V_{HI}. Turn off the device by forcing the EN pin to drop below V_{LO}. If shutdown capability is not required, connect EN to IN. The TPS745-Q1 has an internal pulldown MOSFET that connects a 95-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 95-Ω pulldown resistor. Equation 1calculates the time constant:

$$\tau = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \quad (1)$$

7.3.4 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4\ V \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 42 shows a diagram of the foldback current limit.

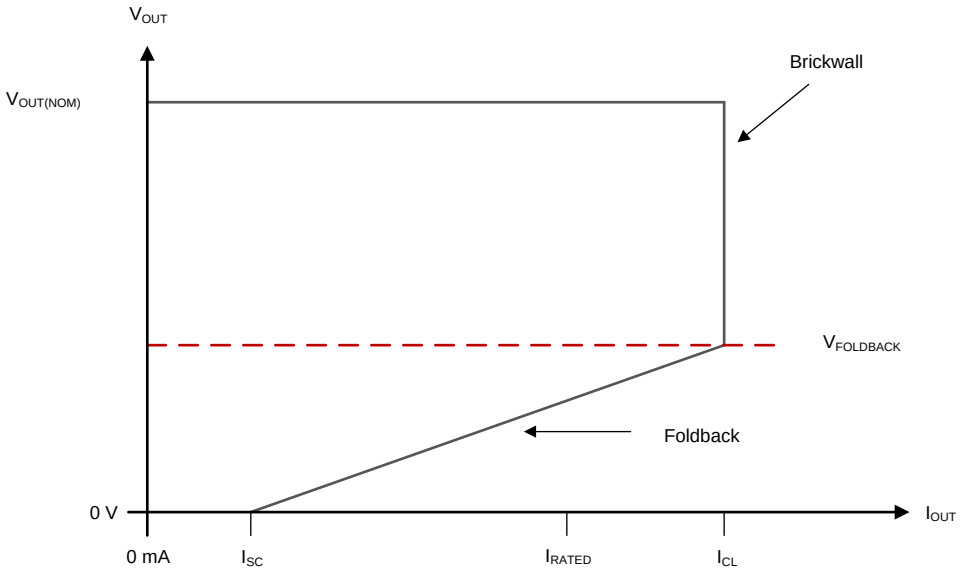


Figure 42. Foldback Current Limit

ADVANCE INFORMATION

7.3.5 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 175°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the regulator from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS745-Q1 internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TPS745-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 2. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

ADVANCE INFORMATION

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Selection

The TPS745-Q1 needs an output capacitance of 1 µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application be sure to look at the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 100 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

ADVANCE INFORMATION

Application Information (continued)

8.1.2 Dropout Voltage

The TPS745-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation.

8.1.3 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in Figure 43, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

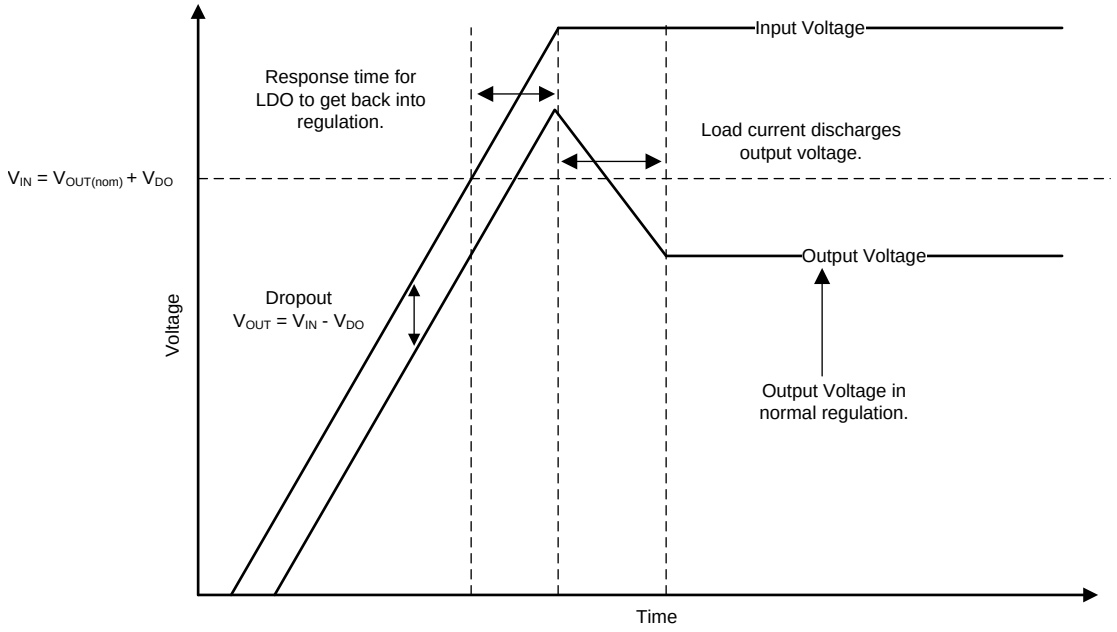


Figure 43. Startup Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. Figure 44 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

ADVANCE INFORMATION

Application Information (continued)

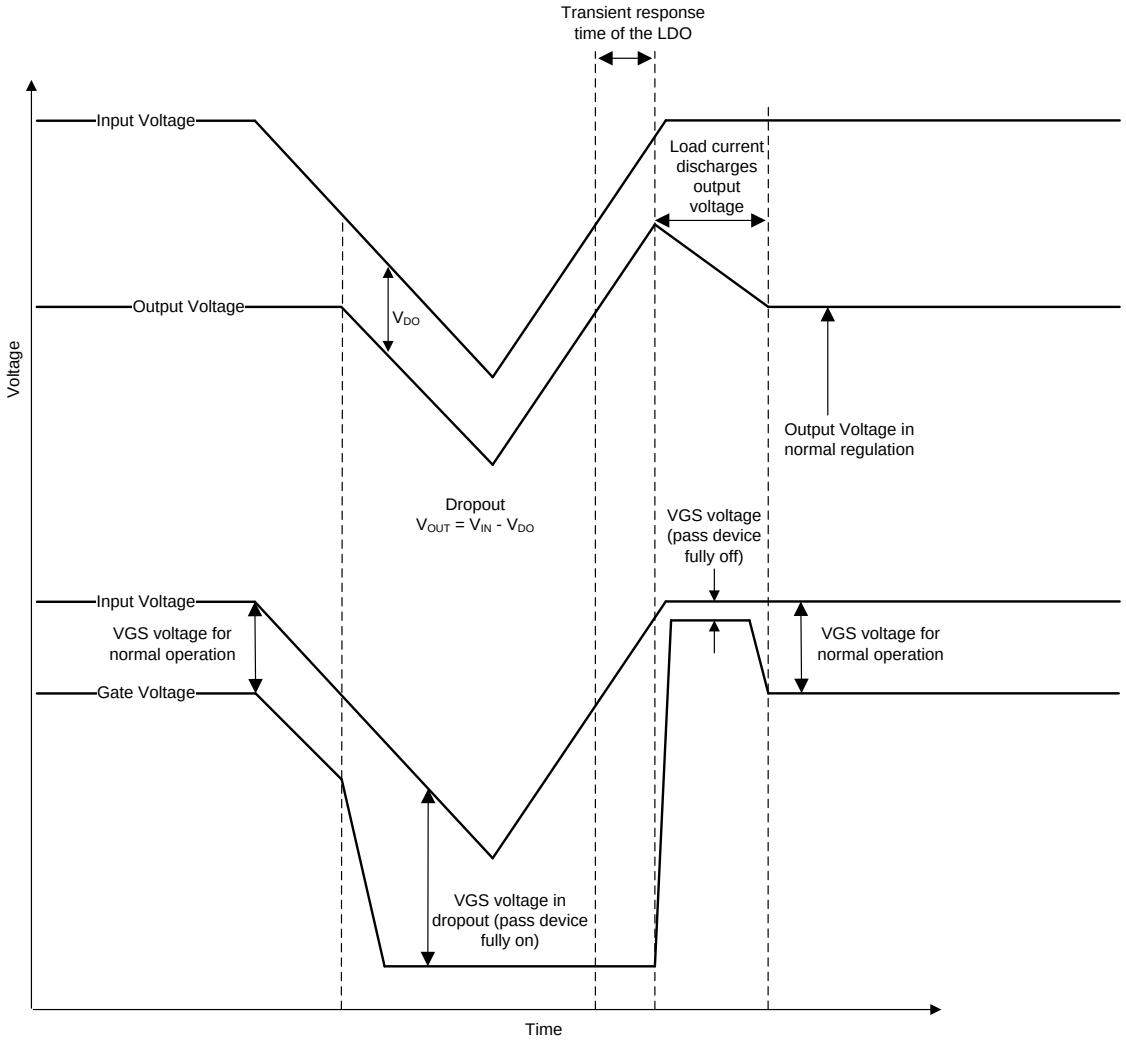


Figure 44. Line Transients From Dropout

8.1.4 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

ADVANCE INFORMATION

Application Information (continued)

If reverse current flow is expected in the application, external protection must be used to protect the device. Figure 45 shows one approach of protecting the device.

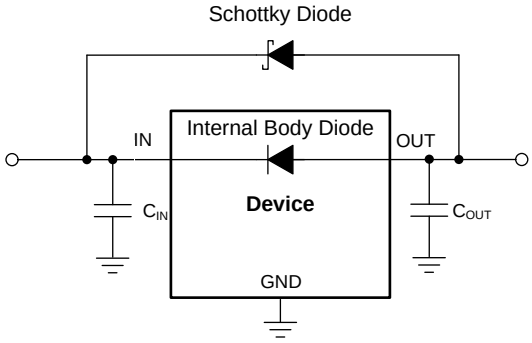


Figure 45. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.5 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 2 calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

NOTE

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

For a more comprehensive study of how thermal resistance varies with copper area and thickness, see the *An empirical analysis of the impact of board layout on LDO thermal performance* application report. As described in Figure 46, modifying board layout to be more thermally enhanced can lower the $R_{\theta JA}$ value from 80.3°C/W to 46.8°C/W or better.

ADVANCE INFORMATION

Application Information (continued)

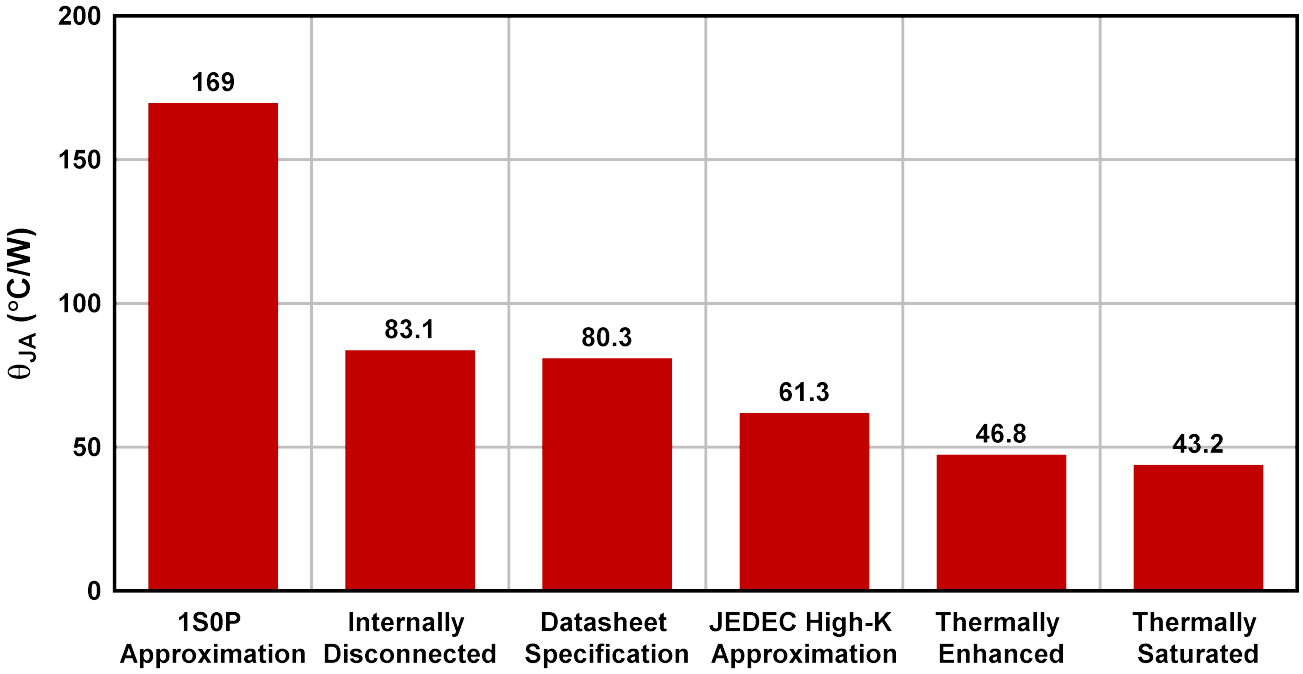


Figure 46. TPS745-Q1 (WSON) $R_{\theta JA}$ vs Board Layout

8.1.6 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the output voltage falls below the PG threshold voltage (PG_{LTH}), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds PG_{HTH}, the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device. Using a pullup resistor from 10 kΩ to 100 kΩ is recommended.

When using a feed-forward capacitor (C_{FF}), the time constant for the LDO startup is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue, and to receive a valid PG output, make sure that the time constant of both the LDO startup and the power-good output match, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

The state of PG is only valid when the TPS745-Q1 operates above the minimum input voltage of the device and power-good is asserted, regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. When the input voltage falls below approximately 0.8 V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

8.1.7 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the startup time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

ADVANCE INFORMATION

Application Information (continued)

8.1.8 Startup sequencing

If V_{EN} is greater than V_{UVLO} rising (min), the input pin (IN) must sink 1 mA of current to avoid the device being turn on with a floating input pin.

8.2 Typical Application

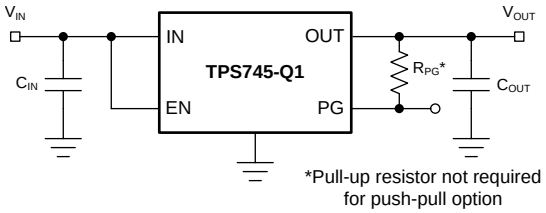


Figure 47. TPS745-Q1 Typical Application

8.2.1 Design Requirements

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3 V
Output voltage	1.8 V, ±1%
Input current	300 mA, maximum
Output load	300-mA DC
Maximum ambient temperature	105°C

8.2.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 2.2 µF are selected to give the maximum output capacitance in a small, low-cost package; see the *Input and Output Capacitor Selection* section for details.

Figure 47 illustrates the output voltage of the ; set the output voltage using the resistor divider.

8.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During startup, the input current is higher as a result of the inrush current charging the output capacitor. Use Equation 4 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (4)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

ADVANCE INFORMATION

8.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use Equation 5 to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ as Equation 6 shows and add the ambient temperature (T_A) to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (5)$$

$$T_J = R_{\theta JA} \times P_D + T_A \quad (6)$$

Calculate the maximum ambient temperature as Equation 7 shows if the ($T_{J(MAX)}$) value does not exceed 150°C. Equation 8 calculates the maximum ambient temperature with a value of 113.86°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (7)$$

$$T_{A(MAX)} = 150°C - 80.3°C/W \times (3.3\ V - 1.8\ V) \times (0.3\ A) = 113.86°C \quad (8)$$

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TPS745-Q1.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Example

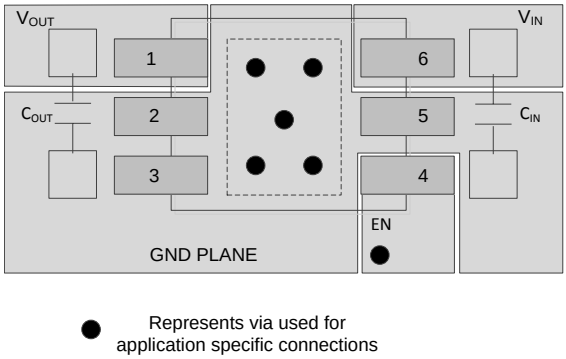


Figure 48. Layout Example for the DRV Package

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Table 4. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TPS745**xx(x)PvQWyyyzQ1**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **P** indicates an active output discharge feature. All members of the TPS745-Q1 family actively discharge the output when the device is disabled. **v** indicates the topology of the power-good output and the timing associated with the power-good delay. • If unused, indicates an open-drain power-good output with a 150-µs delay. • If **B**, indicates a open-drain power-good output with a 5-ms delay. • If **C**, indicates a push-pull power-good output with a 150-µs delay. **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **W** indicates the package has wettable flanks. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces). **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.6 V to 5.0 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *An empirical analysis of the impact of board layout on LDO thermal performance* application report
- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report
-

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

ADVANCE INFORMATION

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PPS74501PCQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	P1ZF	Samples
PPS74501PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	PS26	Samples
PPS74511PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	PS76	Samples
PPS74512PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	PS86	Samples
PPS74518PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	PSA6	Samples
PPS74525PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	PSC6	Samples
PPS74528PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	PSD6	Samples
PPS74533PCQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	P1ZE	Samples
PPS74533PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	PSF6	Samples
TPS74501PBQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74501PCQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74501PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS745105PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74510PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74511PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74512PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74515PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74518PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74522PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74525PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74528PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74529PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74533PCQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74533PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74550PQWDRVRQ1	PREVIEW	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS745-Q1 :

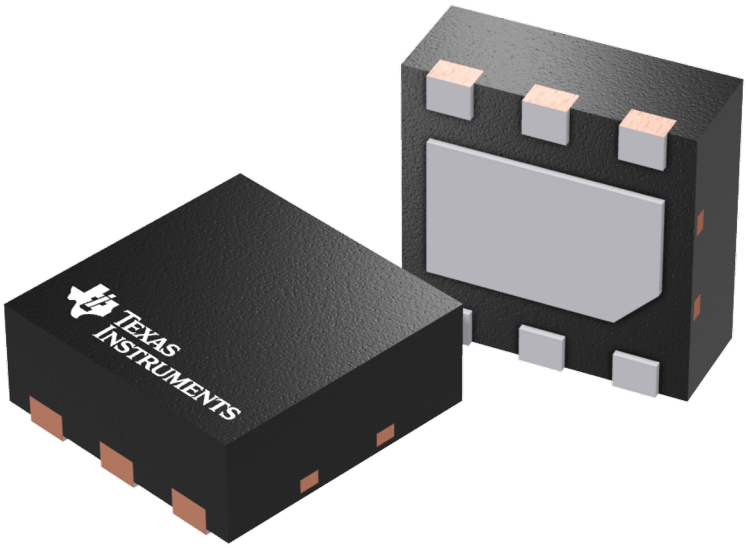
- Catalog: TPS745

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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