State diagram:

- RESET: self-loop i_rst=1; i_rst=0 → READY
- READY: self-loop i_start=0; i_start=1 → INIT
- INIT → FINISH
- FINISH: o_done=0 → FETCH; o_done=1 → WAIT_START
- FETCH → READ_VAL
- READ_VAL → WRITE1
- WRITE1 → WRITE2
- WRITE2 → FINISH
- WAIT_START: self-loop i_start=1; i_start=0 → READY

	load1	sel1	load2	sel2	sel3	en_reg	sel5	o_mem_en	o_mem_we
RESET	0	1	0	1	0	0	0	0	0
READY	0	1	0	1	0	0	0	0	0
INIT	1	0	1	0	0	0	0	0	0
FETCH	0	1	0	1	0	0	0	1	0
READ_VAL	0	1	0	1	0	1	0	1	0
WRITE1	1	1	0	1	0	0	0	1	1
WRITE2	1	1	1	1	0	0	1	1	1
FINISH	0	1	0	1	1	0	0	0	0
WAIT_START	0	1	0	1	1	0	0	0	0