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TESTING AND FAULT TOLERANCE

Laboratory Session 7: “Boundary Scan Testing”

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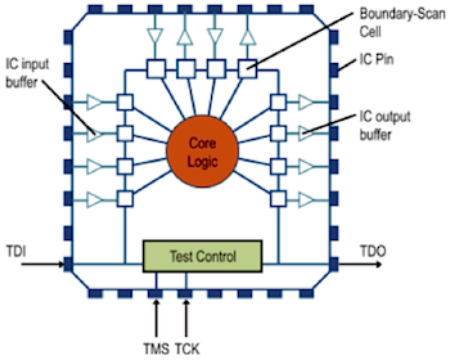

exercises of this lab are provided by Artur Jutman and testonica.

[A] TAP Controller & TAP State Diagram

After running Trainer 1149! and selecting your board (your board number is the last digit of your student ID code, 10 if your digit is 0) (“Board_#.nl”) file from the Netlists folder (where # is the assignment number) do the following:

[A.1] Tasks:

Using the TAP state diagram, TMS, TDI, TDO:

1. Fill the first table with appropriate instruction names used with D# component.
2. Read IDCODE and USERCODE contents from D# IC and record them on the second table.
3. What is the minimum number of clock cycles that is enough to return to the Test-Logic-Reset state from any random state when keeping the TMS signal high? 5

Instruction Code:	000	001	010	011	100	101	110	111
Instruction Name:	USERCODE	BYPASS	EXTEST	SAMPLE	CLAMP	HIGHZ	IDCODE	BYPASS

IDCODE (32-bits)	Binary	10011101100111011000000000011
	Hexadecimal	09D9D803
USERCODE (32-bits)	Binary	10011101100111011000000000011
	Hexadecimal	09D9D803

- Use the BSDL file of the selected IC to find the Instruction names, if the name is missing simulate the instruction code using the TAP state diagram, TMS, TDI, TDO and TCK. The D#.BSD files are located in the “Components” folder.
- You can compare the obtained binary code with the values in the .BSD file of the IC and the hexadecimal

code with the value displayed in the chip graphical view.

[B] Cluster Test

Switch to debug mode. Then, using BS registers apply stimuli to the cluster inputs and measure the cluster output responses in order to determine the functionality of the cluster. Use the following sequence of instructions:

- Define the first test stimulus and apply SAMPLE/PRELOAD, BYPASS, SAMPLE/PRELOAD instructions to chips SN74BCT8244A, D# and SN74BCT8244A, respectively.
- Define the second test stimulus and apply EXTEST, BYPASS, EXTEST instructions.
- Repeat with EXTEST, BYPASS, EXTEST instructions until you identify the Boolean function implemented by the cluster. Remember that the output responses for current data are available at the next test clock cycle.

[B.1] Tasks:

1. Fill in the following truth table of the cluster
2. Draw the schematic of the cluster

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

[C] Interconnect Test & Diagnosis

Using the debug mode do the following:

- Select the “TwoChips” board configuration
- Go to “Diagnostics” → Insert Fault → Random Fault
- Generate test patterns bot for stuck-at faults
- Apply your patterns one by one and record the responses (remember, the data are captured in the next clock cycle)
- Complete the diagnosis

Interconnect nets	Test Patterns	Output Responses	Pass/Fail
Net 0	0,1	0,1	Y
Net 1	0,1	0,1	Y
Net 2	0,1	0,0	N
Net 3	0,1	0,1	Y
Net 4	0,1	0,1	Y
Net 5	0,1	0,1	Y
Net 6	0,1	0,1	Y
Net 7	0,1	0,1	Y
Pass/Fail			

Fault diagnosis: Net 2 s/0

Appendix A: Boundary Scan Coach Software

You can find the Boundary Scan Coach in the course material (setupcoach.exe). The tool is only available for Windows OS. Once installed, you can run the tool to access 3 basic tutorials on JTAG. With this tool, you can only run the tutorials, while you should use “Trainer 1149!” or other tools to practice with virtual boards.

Appendix B: Trainer 1149!

You can find install/setup instructions here. The software is multiplatform but **Java JRE** is required. Once installed, run the tool and complete the exercises. The file is released with the software, but you can also find it in the course material.

As “Assigment no. (1-10)”, use the last digit of your student ID (**if 0, use 10**). For example with s210506 use Assigment no. 6.